

# NCP1523

## 3 MHz, 600 mA, High-Efficiency, Adjustable Output Voltage Step-down Converter

The NCP1523 step-down PWM DC-DC converter is optimized for portable applications powered from 1-cell Li-ion or 3 cell Alkaline/NiCd/NiMH batteries. The device is available in an adjustable output voltage from 0.9 V to 3.3 V. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built-in 3 MHz (nominal) oscillator which reduces component size by allowing use of a small inductor and capacitors. NCP1523 is available in automatic switching PWM/PFM (NCP1523FCT2G) improving system efficiency and in PWM mode only (NCP1523BFCT2G) offering a very efficient load transient solution.

Additional features include integrated soft-start, cycle-by-cycle current limiting and thermal shutdown protection. The NCP1523 is available in a space saving, 8 pin chip scale package.

### Features

- Sources up to 600 mA
- 3 MHz Switching Frequency
- Up to 93% Efficiency
- Synchronous rectification for higher efficiency
- Thermal limit protection
- Shutdown current consumption of 0.3  $\mu$ A
- These are Pb-Free Devices

### Special Features for NCP1523FCT2G

- Auto PFM/PWM mode solution
- High efficiency at light load

### Special Features for NCP1523BFCT2G

- Load Transient Highly Efficient Solution
- Very small Output Voltage Ripple
- Adjustable Output Voltage from 0.9 V to 3.3 V

### Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment



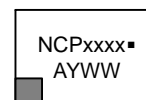
ON Semiconductor®

<http://onsemi.com>



FLIP-CHIP-8  
CASE 766AE

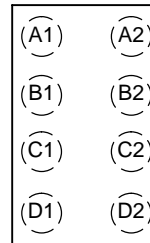
### MARKING DIAGRAM



A1

NCPxxxx = Device Code  
xxxx = 1523 or 523B  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



PIN: A1 - GND  
A2 -  $V_{IN}$   
B1 - SW  
B2 - EN  
C1 - GND  
C2 - ADJ  
D1 -  $V_{OUT}$   
D2 - FB

Top View  
(Bumps Below)

### ORDERING INFORMATION

Device	Package	Shipping†
NCP1523FCT2G (NCP1523)	FLIP-CHIP-8 (Pb-Free)	3000 / Tape & Reel
NCP1523BFCT2G (NCP1523B)	FLIP-CHIP-8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP1523

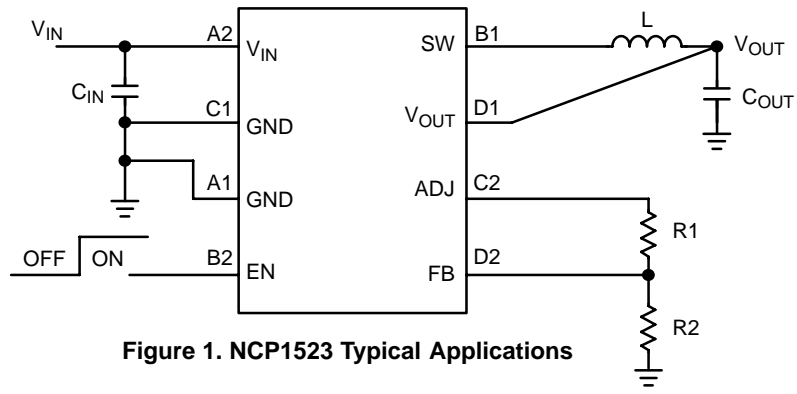


Figure 1. NCP1523 Typical Applications

## TYPICAL APPLICATIONS

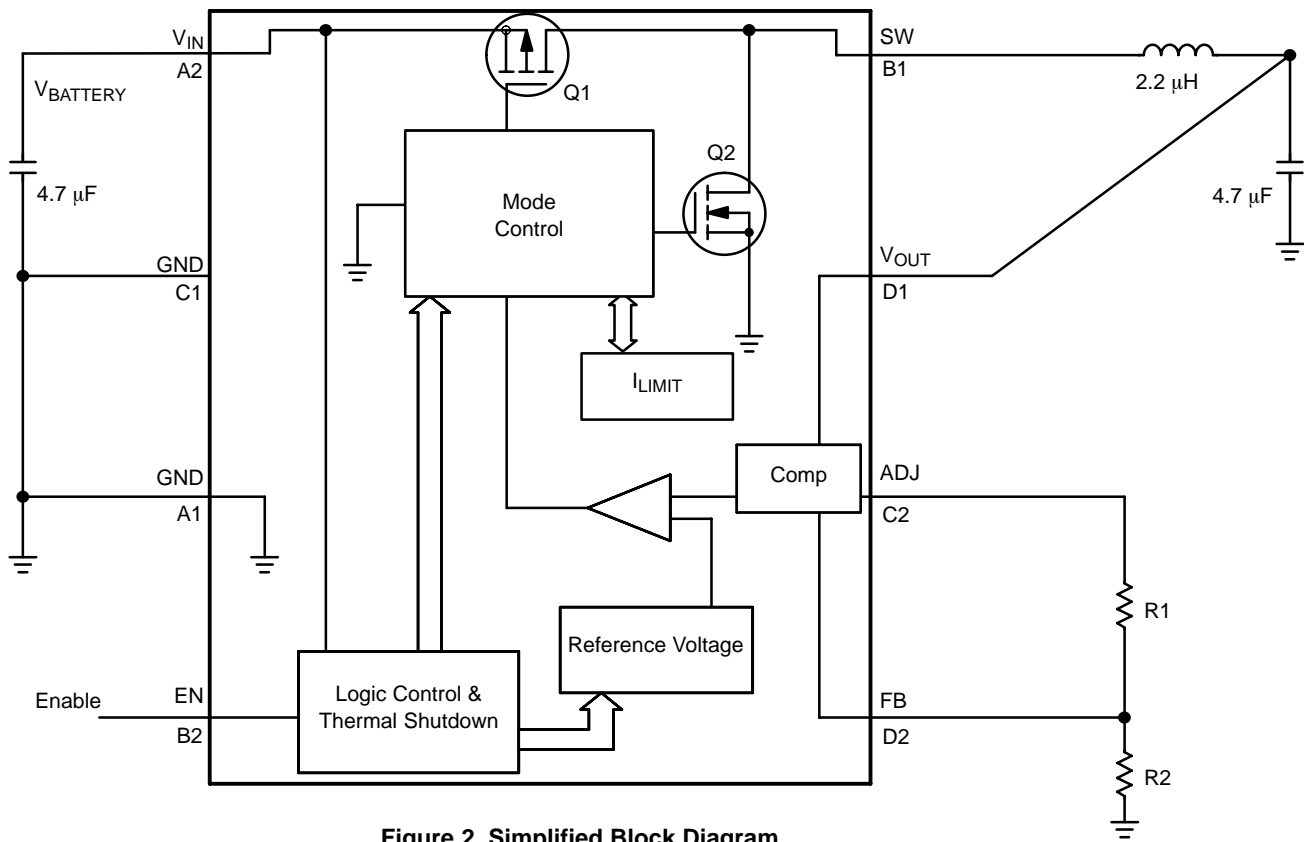


Figure 2. Simplified Block Diagram

# NCP1523

## PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	GND	Power Ground	Ground connection for the NFET Power Stage and the analog sections.
A2	V <sub>IN</sub>	Power Input	Power Supply Input for the PFET Power Stage and the Analog Sections of the IC.
B1	SW	Analog Output	Connection from Power MOSFETs to the Inductor.
B2	EN	Digital Input	Enable for Switching Regulator. This pin is active high. This pin contains an internal pulldown resistor.
C1	GND	Power Ground	Ground connection for the NFET Power Stage and the analog sections.
C2	ADJ	Analog Input	This pin is the compensation input. R1 is connected to this pin.
D1	V <sub>OUT</sub>	Analog Input	This pin is connected of the converter's output. This is the sense of the output voltage.
D2	FB	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V <sub>MIN</sub>	-0.3	V
Maximum Voltage All Pins (Note 1)	V <sub>MAX</sub>	7	V
Maximum Voltage Enable, FB, SW	V <sub>MAX</sub>	V <sub>IN</sub> + 0.3	V
Thermal Resistance, Junction-to-Air (Note 2)	R <sub>θJA</sub>	159	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to 85	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to 150	°C
Junction Operating Temperature	T <sub>J</sub>	-40 to 125	°C
Latch-up Current Maximum Rating T <sub>A</sub> = 85°C (Note 4)	I <sub>LU</sub>	± 100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V <sub>ESD</sub>	2.0 200	kV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22-A108B
2. For the 8-Pin Chip Scale Package, the R<sub>θJA</sub> is highly dependent of the PCB heatsink area. R<sub>θJA</sub> = 159°C/W with 50 mm<sup>2</sup> PCB heatsink area.
3. This device series contains ESD protection and exceeds the following tests:  
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114  
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115
4. Latchup current maximum rating per JEDEC standard: JESD78.

# NCP1523

## ELECTRICAL CHARACTERISTICS FOR NCP1523

(Typical values are referenced to  $T_A = +25^\circ\text{C}$ , Minimum and Maximum values are referenced  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  ambient temperature, unless otherwise noted, operating conditions  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$  unless otherwise noted)

Symbol	Rating	Min	Typ	Max	Unit
$V_{IN}$	Input Voltage Range	2.7		5.5	V
$V_{UVLO}$	Under Voltage Lockout ( $V_{IN}$ Falling)		2.4		V
$I_q$	Quiescent Current (Light Load Mode)		60	95	$\mu\text{A}$
$I_{STB}$	Standby Current, EN Low		0.3	1.2	$\mu\text{A}$
$F_{OSC}$	Oscillator Frequency	2.400	3	3.600	MHz
$I_{LIM}$	Peak Inductor Current		1200		mA
$V_{REF}$	Feedback Reference Voltage		0.6		V
$V_{FBtol}$	FB Pin Tolerance Overtemperature	-3		3	%
$\Delta V_{FB}$	Reference Voltage Line Regulation		0.1		%
$V_{OUT}$	Output Voltage Accuracy (Note 5)	-3%	$V_{nom}$	+3%	V
$V_{OUT}$	Minimum Output Voltage		0.9		V
$V_{OUT}$	Maximum Output Voltage		2.3		V
$\Delta V_{OUT}$	Output Voltage Line Regulation ( $V_{IN}$ from 2.7 to 5.5) $I_O = 100\text{ mA}$		0.1		%
$V_{LOADREG}$	Voltage Load Regulation ( $I_O = 150\text{ mA}$ to $600\text{ mA}$ )		0.001		%/mA
	Duty Cycle			100	%
$R_{SWH}$	P-Channel On-Resistance		300		$\text{m}\Omega$
$R_{SWL}$	N-Channel On-Resistance		300		$\text{m}\Omega$
$I_{LeakH}$	P-Channel Leakage Current		0.05		$\mu\text{A}$
$I_{LeakL}$	N-Channel Leakage Current		0.01		$\mu\text{A}$
$V_{ENH}$	Enable Pin High	1.2			V
$V_{ENL}$	Enable Pin Low			0.4	V
$T_{START}$	Soft Start Time		350	450	$\mu\text{s}$

5. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1, R2).

# NCP1523

## ELECTRICAL CHARACTERISTICS FOR NCP1523B

(Typical values are referenced to  $T_A = +25^\circ\text{C}$ , Minimum and Maximum values are referenced  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  ambient temperature, unless otherwise noted, operating conditions  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$  unless otherwise noted)

Symbol	Rating	Min	Typ	Max	Unit
$V_{IN}$	Input Voltage Range	2.7		5.2	V
$V_{UVLO}$	Under voltage Lockout ( $V_{IN}$ Falling)		2.4		V
$I_q$	Quiescent Current – No Switching – Oscillator Running		250 2.5	350	$\mu\text{A}$ mA
$I_{STB}$	Standby Current, EN Low		0.3	1.2	$\mu\text{A}$
$F_{OSC}$	Oscillator Frequency	2.400	3	3.600	MHz
$I_{LIM}$	Peak Inductor Current		1200		mA
$V_{REF}$	Feedback Reference Voltage		0.6		V
$V_{FBtol}$	FB Pin Tolerance Overtemperature	-3		3	%
$\Delta V_{FB}$	Reference Voltage Line Regulation		0.1		%
$V_{OUT}$	Output Voltage Accuracy (Note 6)	-3%	$V_{nom}$	+3%	V
$V_{OUT}$	Minimum Output Voltage (Note 7)		0.9		V
$V_{OUT}$	Maximum Output Voltage		3.3		V
$\Delta V_{OUT}$	Output Voltage Line Regulation ( $V_{IN} = 2.7 - 5.2$ ) $I_O = 100\text{ mA}$ (Note 7)		0.1		%
$V_{LOADREG}$	Voltage Load Regulation ( $I_O = 1\text{ mA}$ to $600\text{ mA}$ ) (Note 7)		0.001		%/mA
	Duty Cycle			100	%
$R_{SWH}$	P-Channel On-Resistance		300		$\text{m}\Omega$
$R_{SWL}$	N-Channel On-Resistance		300		$\text{m}\Omega$
$I_{LeakH}$	P-Channel Leakage Current		0.05		$\mu\text{A}$
$I_{LeakL}$	N-Channel Leakage Current		0.01		$\mu\text{A}$
$V_{ENH}$	Enable Pin High	1.2			V
$V_{ENL}$	Enable Pin Low			0.4	V
$T_{START}$	Soft-Start Time		350	450	$\mu\text{s}$

6. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1, R2).

7. Electrical values are guaranteed for drop between input and output voltages less than 4.0 V (Page 13).

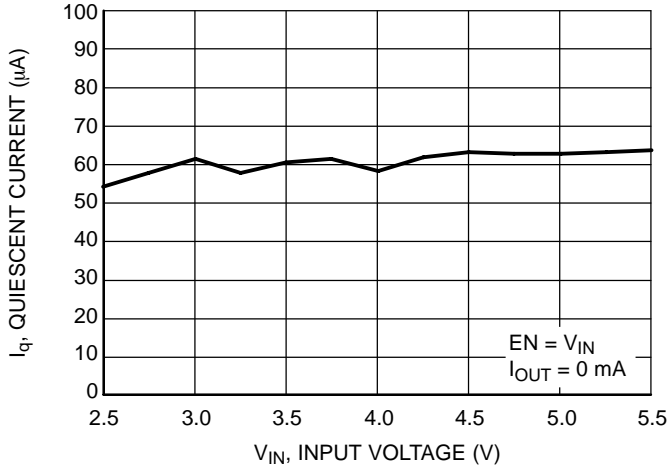
# NCP1523

## TABLE OF GRAPHS

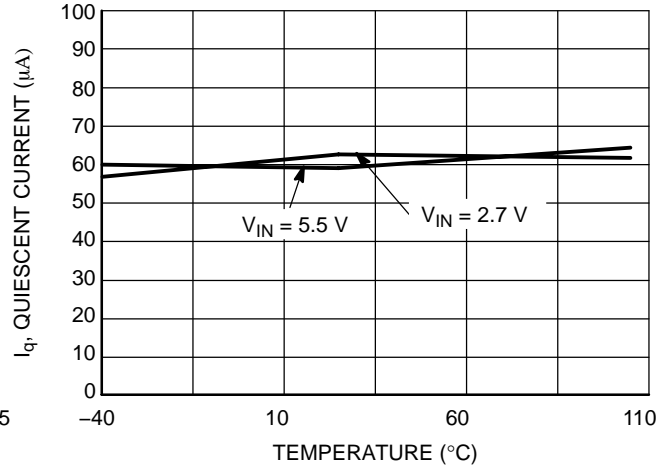
TYPICAL CHARACTERISTICS			NCP1523FCT2G	NCP1523BFCT2G
$\eta$	Efficiency	vs. Load Current	6, 7, 8	20, 21, 22
		vs. Input Voltage		23
$V_{OUT}$	Output Voltage	vs. Temperature		
$F_{OSC}$	Frequency Variation	vs. Input Voltage	9, 10	19
$V_{OUT}$	Load Regulation	vs. Load Current	11	24
		vs. Temperature		25
$V_{OUT}$	Line Regulation	vs. Output Current		26
		vs. Temperature		27
$V_{OUT}$	Load Transient Response		15, 16	32, 33
$V_{OUT}$	Line Transient Response			31
$I_{stb}$	Shutdown Current	vs. Input Voltage	5	
		vs. Temperature	3	28
$I_q$	Quiescent Current	vs. Temperature	4	29
	PWM Mode Operation		13	18
	PFM Mode Operation		14	
	PFM/PWM Threshold	vs. Input Voltage	12	
$T_{start}$	Soft Start		17	30

# NCP1523

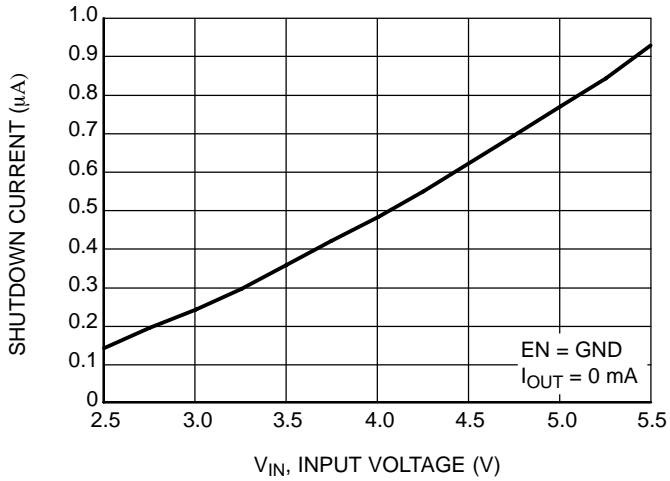
## NCP1523 CHARACTERISTICS



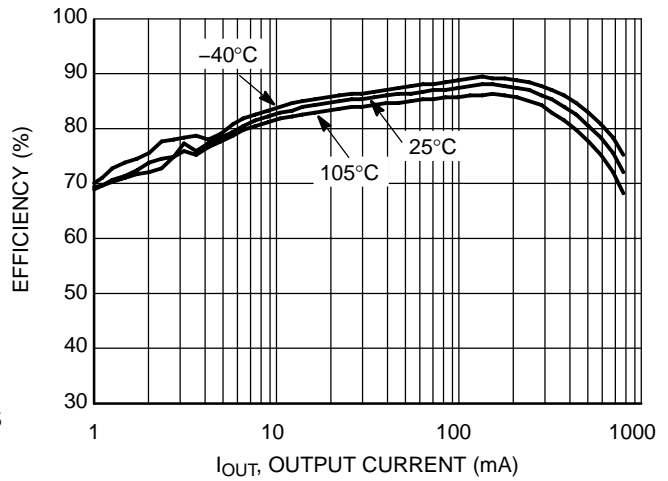
**Figure 3. Quiescent Current vs. Supply Voltage**



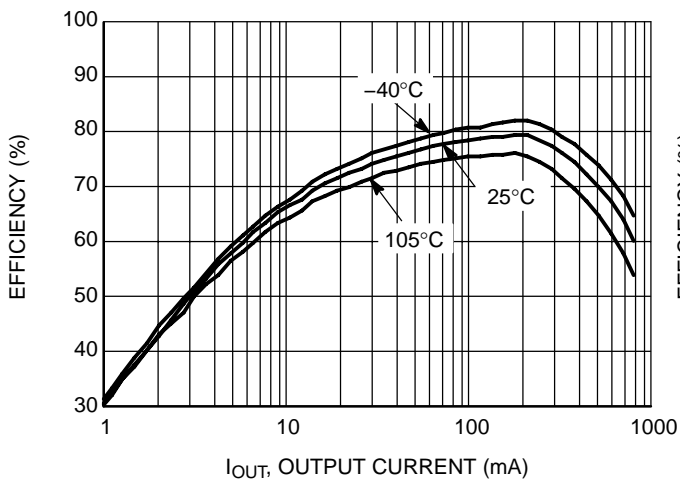
**Figure 4. Quiescent Current vs. Temperature**



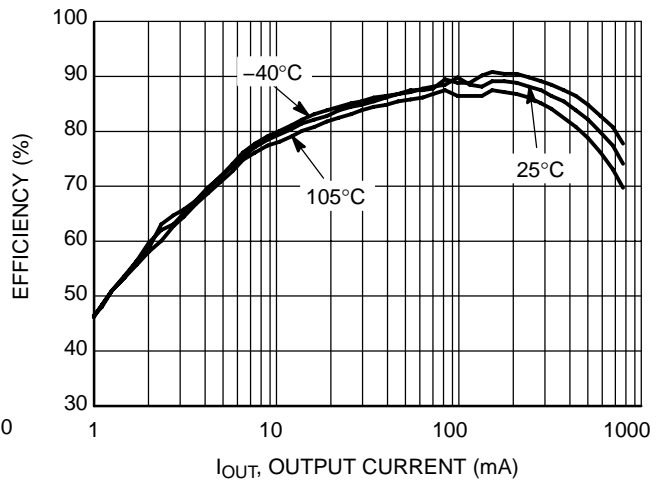
**Figure 5. Shutdown Current vs. Supply Voltage**



**Figure 6. Efficiency vs. Output Current ( $V_{OUT} = 1.8 \text{ V}$ ,  $V_{IN} = 3.6 \text{ V}$ )**



**Figure 7. Efficiency vs. Output Current ( $V_{OUT} = 0.9 \text{ V}$ ,  $V_{IN} = 3.6 \text{ V}$ )**



**Figure 8. Efficiency vs. Output Current ( $V_{OUT} = 2.0 \text{ V}$ ,  $V_{IN} = 3.6 \text{ V}$ )**

# NCP1523

## NCP1523 CHARACTERISTICS

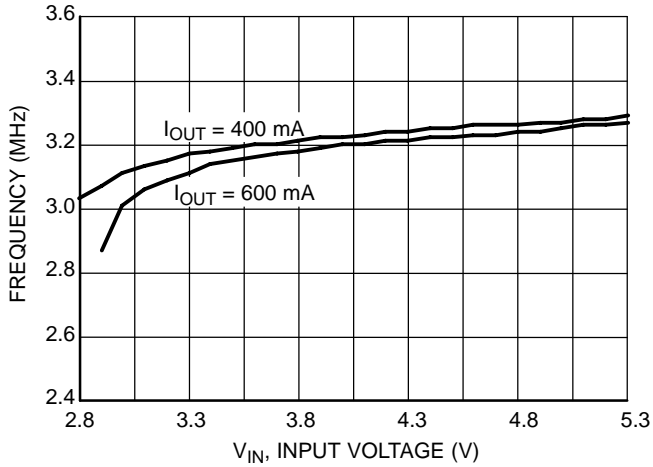


Figure 9. Frequency vs. Input Voltage

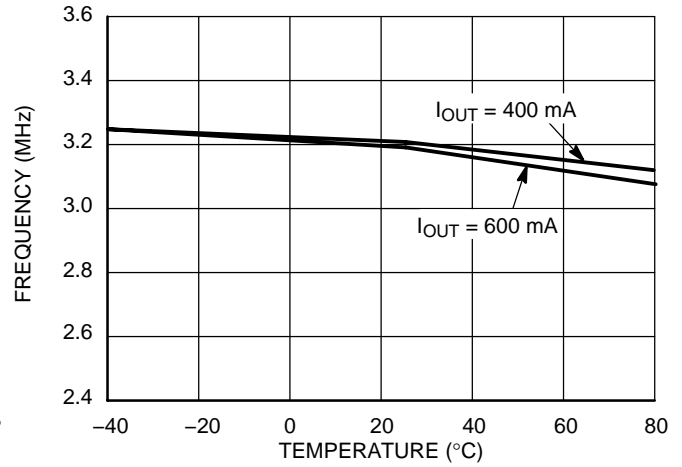


Figure 10. Frequency vs. Temperature

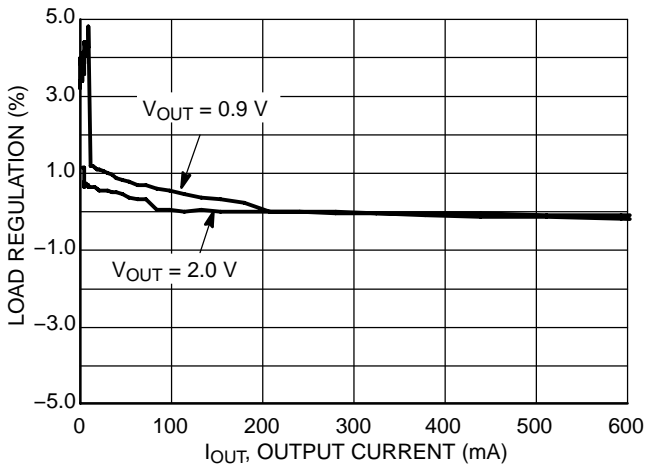


Figure 11. Load Regulation

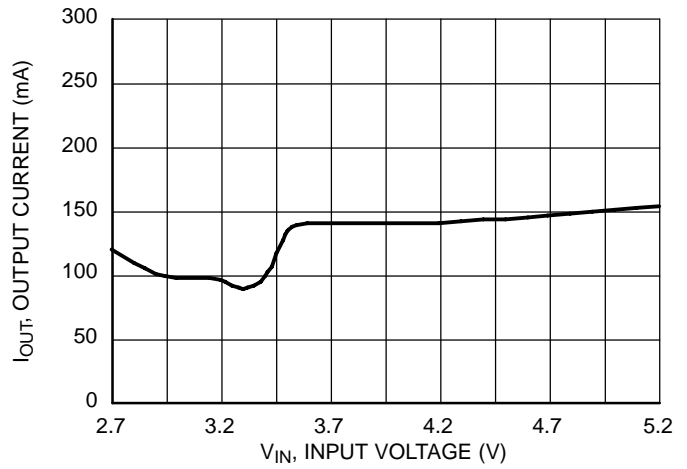


Figure 12. PFM/PWM Threshold vs. Input Voltage

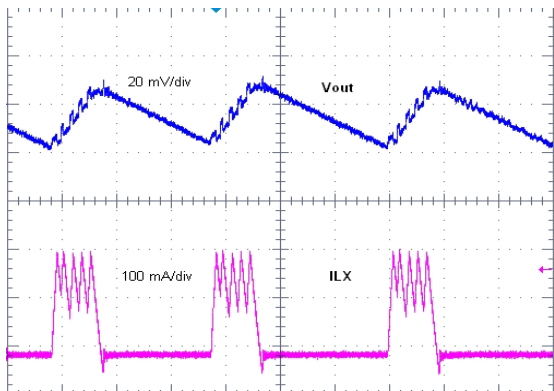


Figure 13. Step Down Converter PFM Mode Operation

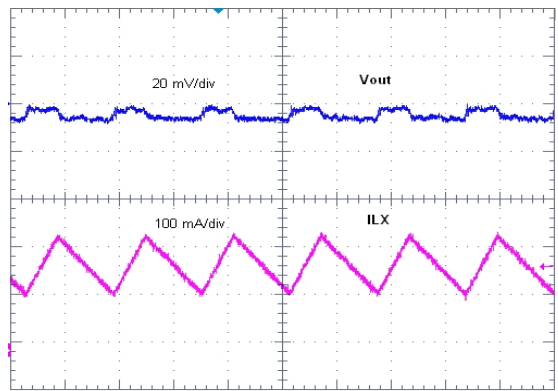


Figure 14. Step Down Converter PWM Mode Operation



# NCP1523

## NCP1523 CHARACTERISTICS

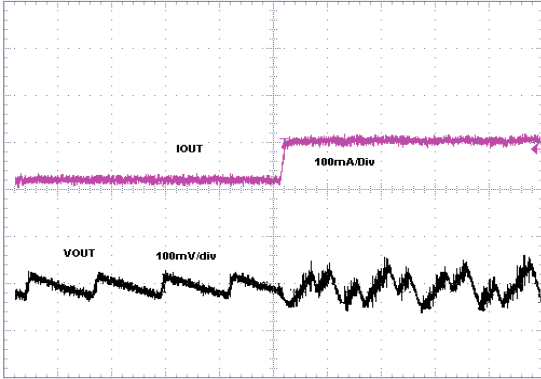


Figure 15. Load Transient Response in PFM Operation (10 mA to 100 mA)

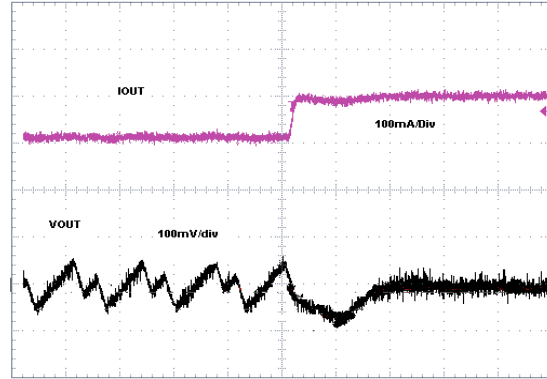


Figure 16. Load Transient Response Between PFM and PWM Operation (100 mA to 200 mA)

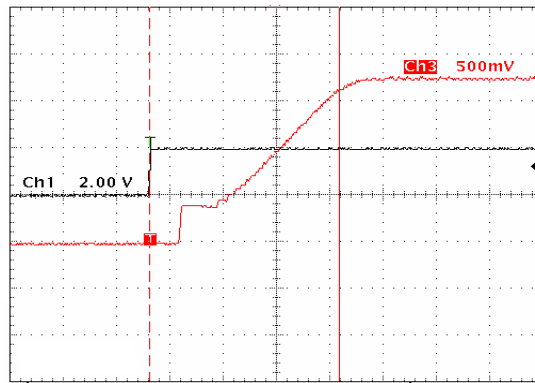


Figure 17. Soft Start Time ( $V_{IN} = 3.6 \text{ V}$ )

NCP1523B CHARACTERISTICS

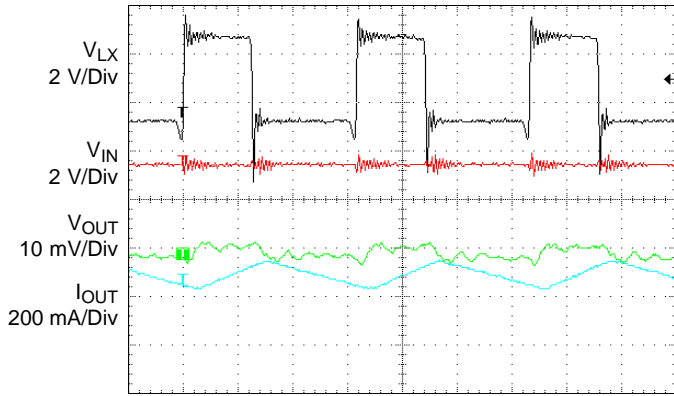


Figure 18. PWM Mode of Operation  
( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$ ,  $25^\circ\text{C}$ )

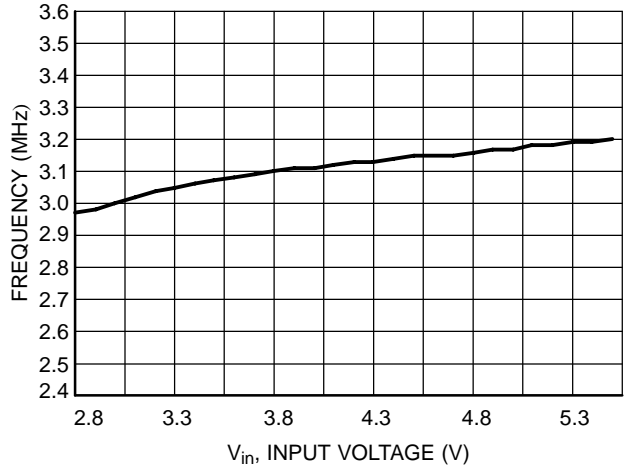


Figure 19. Switching Frequency vs. Input Voltage  
( $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 300\text{ mA}$ ,  $25^\circ\text{C}$ )

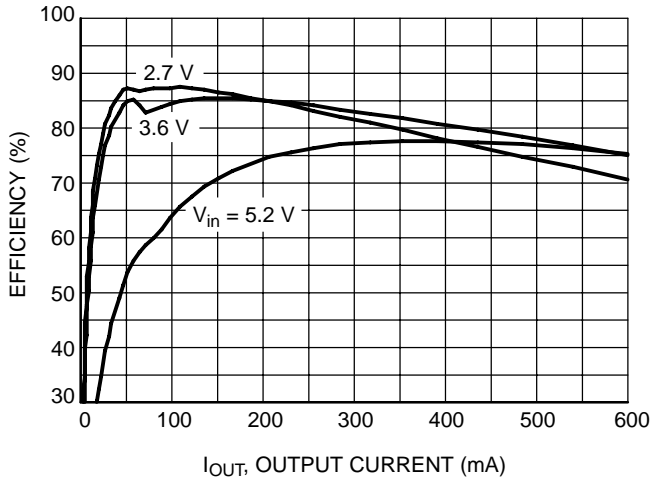


Figure 20. Efficiency vs. Output Current  
( $V_{OUT} = 1.2\text{ V}$ ,  $25^\circ\text{C}$ )

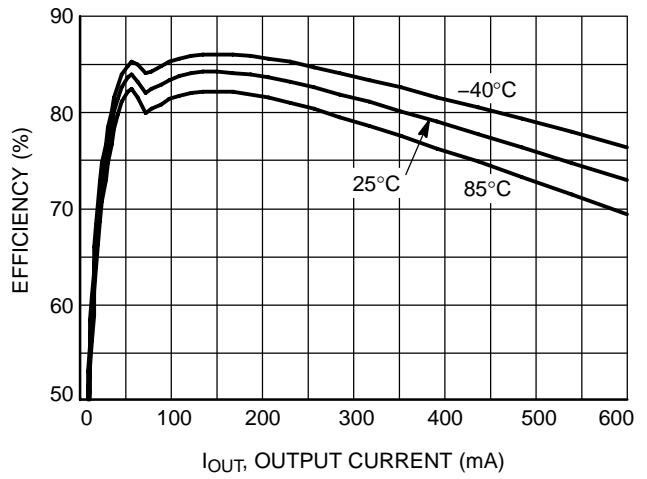


Figure 21. Efficiency vs. Output Current  
( $V_{OUT} = 1.2\text{ V}$ ,  $V_{IN} = 3.6\text{ V}$ )

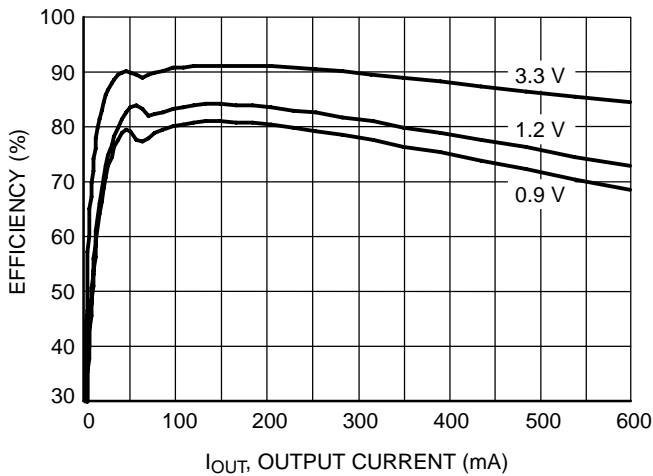


Figure 22. Efficiency vs. Output Current  
( $V_{IN} = 3.6\text{ V}$ ,  $25^\circ\text{C}$ )

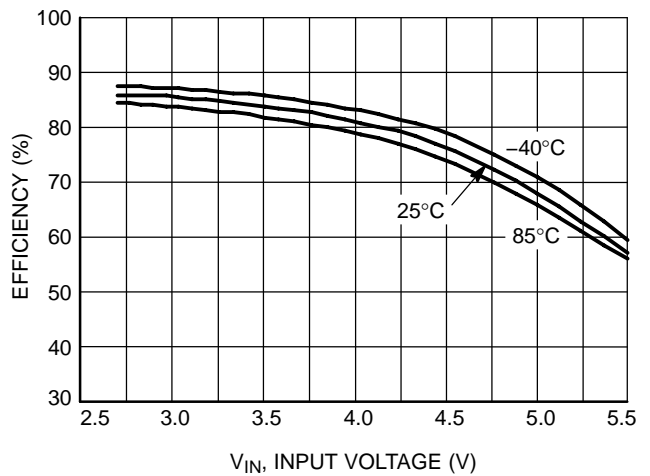


Figure 23. Efficiency vs. Input Current  
( $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ )

# NCP1523

## NCP1523B CHARACTERISTICS

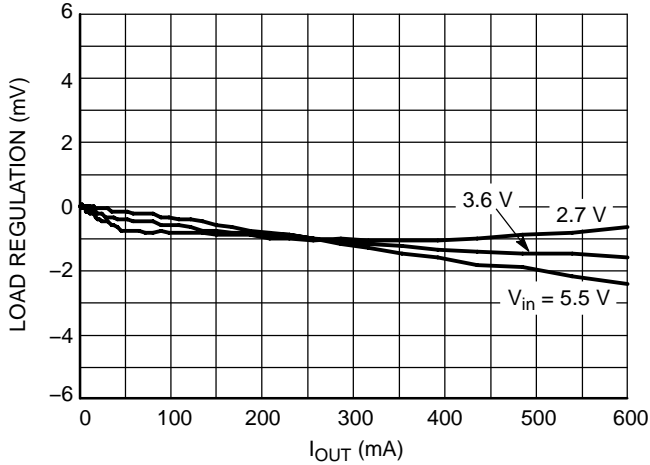


Figure 24. Load Regulation vs. Input Voltage  
( $V_{OUT} = 1.2\text{ V}$ ,  $25^\circ\text{C}$ )

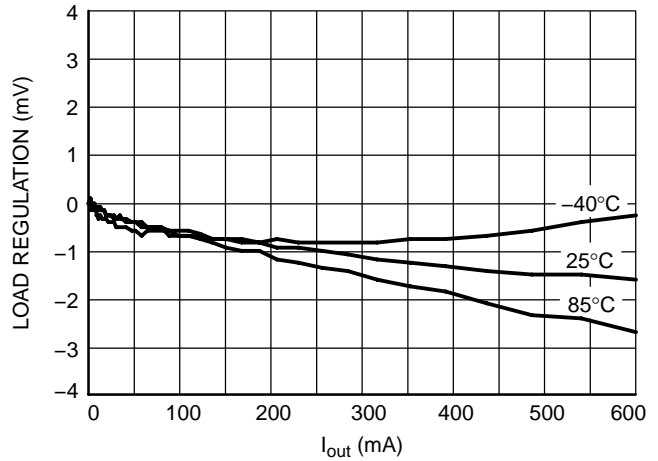


Figure 25. Load Regulation vs. Temperature  
( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ )

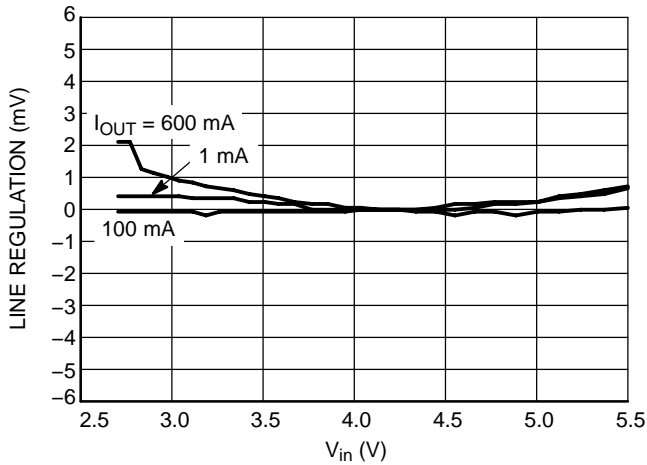


Figure 26. Line Regulation vs. Output Current  
( $V_{OUT} = 1.2\text{ V}$ ,  $25^\circ\text{C}$ )

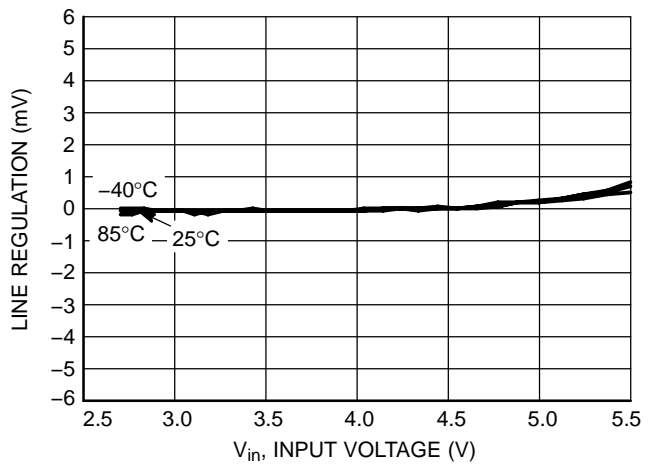


Figure 27. Line Regulation vs. Temperature  
( $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ )

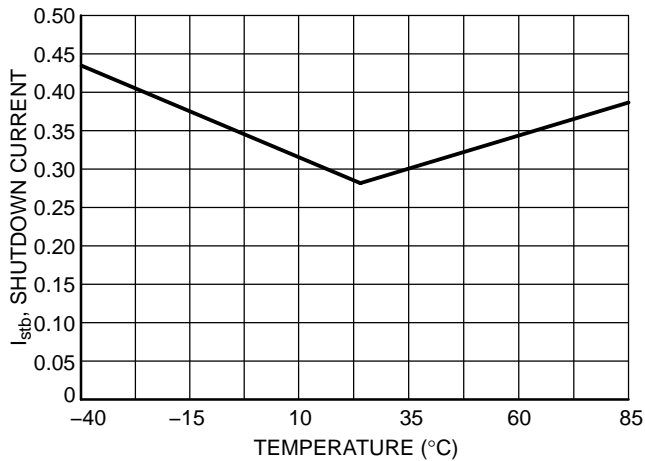


Figure 28. Shutdown Current vs. Temperature  
( $V_{OUT} = 3.6\text{ V}$ )

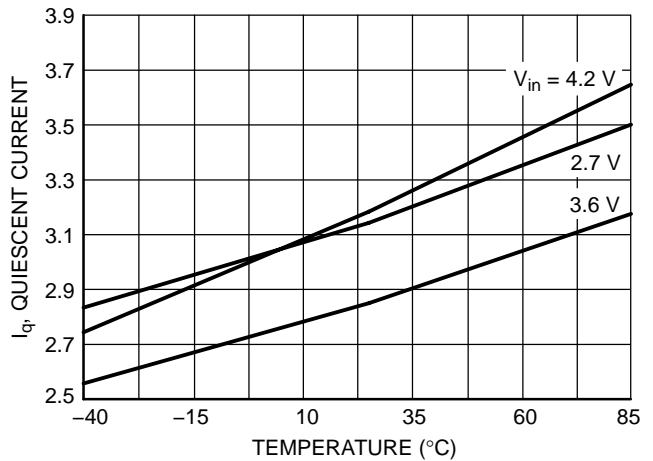


Figure 29. Quiescent Current vs. Temperature

NCP1523B CHARACTERISTICS

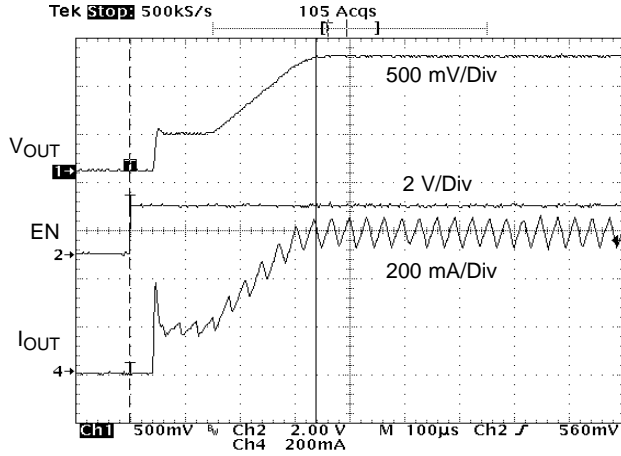


Figure 30. Soft Start Time  
 ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 600\text{ mA}$ )

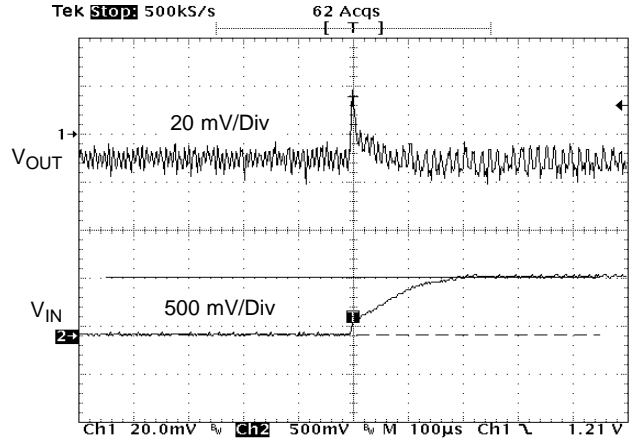


Figure 31. Line Transient Response  
 ( $V_{IN}$  step =  $600\text{ mV}$ ,  $V_{OUT} = 1.2\text{ V}$ )

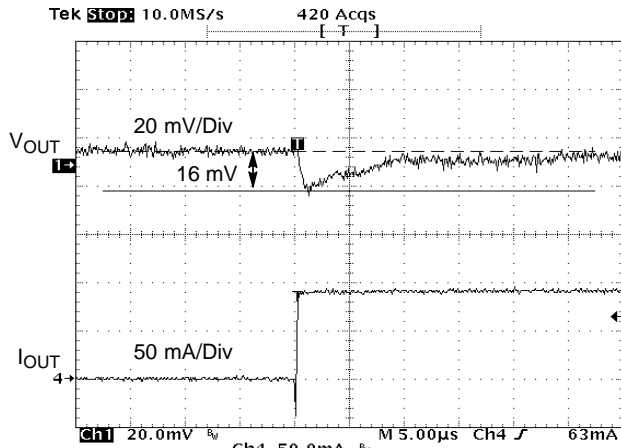


Figure 32. Load Transient Response  
 ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $0\text{ mA}$  to  $95\text{ mA}$  step)

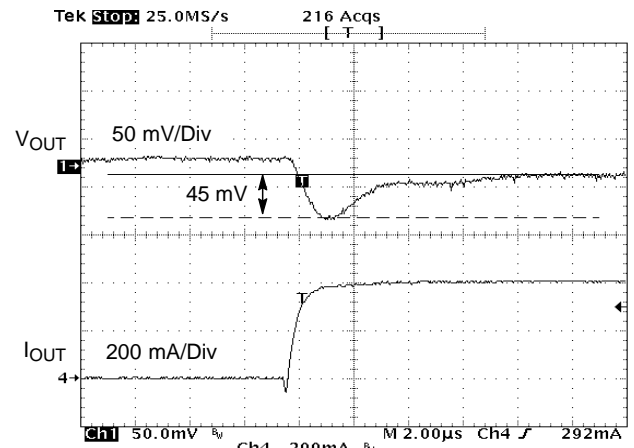


Figure 33. Load Transient Response  
 ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $0\text{ mA}$  to  $400\text{ mA}$  step)

## OPERATION DESCRIPTION

**Overview**

The NCP1523 uses a constant frequency, voltage mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal.

It delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDA. The output voltage is set by external resistor divider and has a voltage tolerance of  $\pm 3\%$  with 90% efficiency or better. The NCP1523 sources up to 600 mA depending on external components chosen.

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only six external components are required for implementation. The part uses an internal reference voltage of 0.6 V. It is recommended to keep the part in shutdown until the input voltage is 2.7 V or higher.

**PWM Operating Mode: NCP1523 & NCP1523B**

In this mode, the output voltage of the NCP1523 is regulated by modulating the on-time pulse width of the main switch Q1 at a fixed frequency of 3 MHz. The switching of the PMOS Q1 is controlled by a flip-flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the PWM ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the amplifier's error voltage. Once this has occurred, the PWM comparator resets the flip-flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

**PFM Operating Mode at Light Load: NCP1523 Only**

The NCP1523FCT2G works with two mode of operation PWM/PFM depending on the current required. Under light load conditions, the NCP1523FCT2G enters in low current PFM mode of operation to reduce power consumption ( $I_Q = 60 \mu\text{A typ}$ ). The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically  $V_{\text{nom}} - 2\%$ ), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until the peak inductor current reaches 200 mA (nom). Then  $I_{\text{LIM}}$  comparator goes high to switch OFF Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The Negative current detector (NCD) will detect when the inductor current drops below zero and the output voltage decreases through discharging the output capacitor. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

**PWM Operating Mode at Light Load: NCP1523B Only**

At low light conditions, NCP1523BFCT2G works also in PWM mode offering very good load transient results from light load to full charge. When there is no load on the output, the PMOS Q1 remains ON during a small pulse according to the flip-flop driven by the internal oscillator and the error comparator. If the drop between input and output voltage is higher than 4.0 V, the structure reaches the minimum ON time ( $T_{\text{ONmin}}$ ). In this particular case, the part can not supply correctly the desired output voltage and shows a small output voltage deregulation. For an output voltage configured to 0.9 V, 4.9 V is the maximum input voltage which guarantees the correct output value; for an output set to 1.5 V, the maximum input is 5.5 V.

**Cycle-by-Cycle Current Limitation**

From the block diagram (Figure 3), an  $I_{\text{LIM}}$  comparator is used to realize cycle-by-cycle current limit protection. The comparator compares the SW pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the  $I_{\text{LIM}}$  comparator detects the SW voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle-by-cycle current limit is set at 1200 mA (nom).

**Soft Start**

The NCP1523 uses soft-start to limit the inrush current when the device is initially powered up or enabled. Soft-start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft-start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

**Shutdown Mode**

When a voltage less than 0.4 V is applied on the EN pin, the NCP1523 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3  $\mu\text{A}$  (typical value). Applying a voltage above 1.2 V to EN pin will enable the device for normal operation. The device will go through soft-start to normal operation. EN pin should be activated after the input voltage is applied.

**Thermal Shutdown**

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction Temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating.

APPLICATION INFORMATION

**Output Voltage Selection**

The output voltage is programmed through an external resistor divider connected from ADJ to FB then to GND. For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100 kΩ – 600 kΩ] range. If R2 is 200 kΩ given the V<sub>FB</sub> is 0.6 V, the current through the divider will be 3 μA.

The formula below gives the value of V<sub>OUT</sub>, given the desired R1 and the R1 value,

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

- V<sub>OUT</sub>: output voltage (volts)
- V<sub>FB</sub>: feedback voltage = 0.6 V
- R1: feedback resistor from V<sub>OUT</sub> to FB
- R2: feedback resistor from FB to GND

**Input Capacitor Selection**

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is I<sub>O</sub>, max/2.

For NCP1523, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V<sub>IN</sub> Pin.

**Table 1. LIST OF INPUT CAPACITOR**

Murata	GRM188R60J475KE
	GRM21BR71C475KA
Taiyo Yuden	JMK212BY475MG
TDK	C2012X5R0J475KT
	C1608X5R0J475KT

**Output L–C Filter Design Considerations:**

The NCP1523 is built in 3 MHz frequency and uses voltage mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L–C filter must be selected to work with internal compensation. For NCP1523, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C<sub>OUT</sub> = 4.7 μF

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu\text{H} \times 4.7\ \mu\text{F}}} = 49.5\ \text{KHz}$$

The device operates with inductance value between 1 μH and maximum of 4.7 μH.

If the corner frequency is moved, it is recommended to check the loop stability depending of the output ripple voltage accepted and output current required. For lower frequency, the stability will be increase; a larger output capacitor value could be chosen without critical effect on the system. On the other hand, a smaller capacitor value increases the corner frequency and it should be critical for the system stability. Take care to check the loop stability. The phase margin is usually higher than 45°.

**Table 2. L–C FILTER EXAMPLE**

Inductance (L)	Output Capacitor (C <sub>OUT</sub> )
1 μH	10 μF
2.2 μH	4.7 μF
4.7 μH	2.2 μF

**Inductor Selection**

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI<sub>L</sub>) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

ΔI<sub>L</sub> = peak to peak inductor ripple current

L = inductor value

f<sub>SW</sub> = Switching frequency

The Saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

I<sub>L(MAX)</sub> Maximum inductor current

I<sub>O(MAX)</sub> Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

**Table 3. LIST OF INDUCTOR**

FDK	MIPW3226 Series
TDK	VLF3010AT Series
	TFC252005 Series
Taiyo Yuden	LQ CBL2012
Coil Craft	DO1605–T Series
	LPO3010

## Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left( \frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR \right)$$

In PFM mode (at light load), the output voltage is regulated by pulse frequency modulation. The output voltage ripple is independent of the output capacitor value. It is set by the threshold of PM comparator.

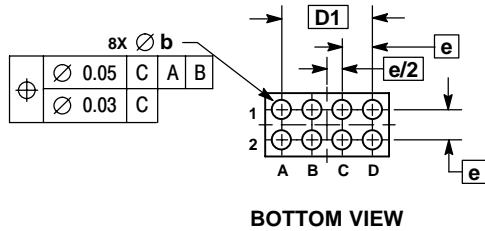
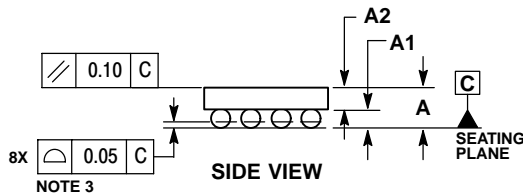
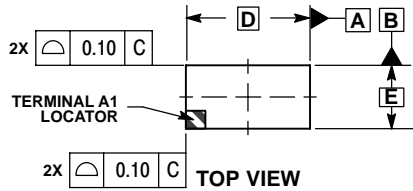
**Table 4. LIST OF OUTPUT CAPACITOR ROHS**

Murata	GRM188R60J475KE	4.7 $\mu$ F
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 $\mu$ F
Taiyo Yuden	JMK212BY475MG	4.7 $\mu$ F
	JMK212BJ106MG	10 $\mu$ F
TDK	C2012X5R0J475KT	4.7 $\mu$ F
	C1608X5R0J475KT	
	C2012X5R0J106KT	10 $\mu$ F

# NCP1523

## PACKAGE DIMENSIONS

### 8 PIN FLIP-CHIP, 2.05x1.05, 0.5P CASE 766AE-01 ISSUE C



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.655
A1	0.210	0.270
A2	0.335	0.385
b	0.290	0.340
D	2.050 BSC	
D1	1.500 BSC	
E	1.050 BSC	
e	0.500 BSC	

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative