MOTOROLA

SN54/74LS569A

FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

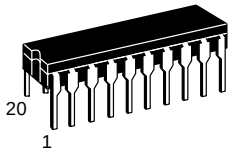
The SN54/74LS569A is designed as programmable up/down BCD and Binary counters respectively. These devices have 3-state outputs for use in bus organized systems. With the exception of output enable (OE) and asynchronous clear (ACLR), all functions occur on the positive edge of the clock pulse (CP).

When the LOAD input is LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Enabling of the counters occurs only when CEP and CET are LOW and LOAD is HIGH. Direction of the count is controlled by the up-down input (U/D), HIGH counts up and LOW counts down. High-speed counting and cascading is implemented by internal look-ahead carry logic and an active LOW ripple carry output (RCO). On the LS569A, the RCO is LOW at binary 15 during up-count and during down-count it is also LOW at binary 0. During normal cascading operation RCO connected to the succeeding block at CET is the only requisite. When counting and when RCO is LOW, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset asynchronous clear (ACLR) and a synchronous clear (SCLR). When in a HIGH state, the output control (OE) input forces the counter output into a HIGH impedance state and when LOW, the counter outputs are enabled.

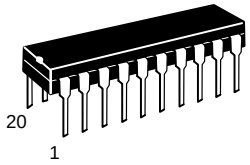
- ESD > 3500 Volts

FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

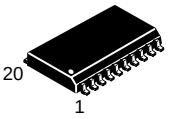
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

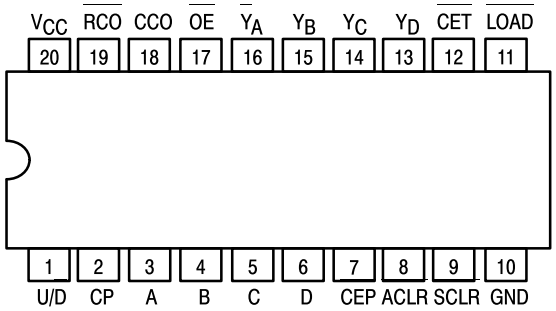


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

CONNECTION DIAGRAM (TOP VIEW)



V_{CC} = PIN 20
GND = PIN 10

Note: Pin 1 is marked for orientation.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High Except $\overline{RCO}$, CCO	54 74			−1.0 −2.6	mA
I_{OH}	Output Current — High $\overline{RCO}$, CCO	54, 74			−0.44	mA
I_{OL}	Output Current — Low Except $\overline{RCO}$, CCO	54 74			12 24	mA
I_{OL}	Output Current — Low, $\overline{RCO}$, CCO	54 74			4.0 8.0	mA

FUNCTION TABLE

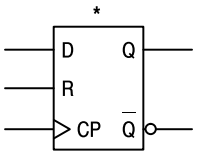
INPUTS											OUTPUTS						
CP	D	C	B	A	$\overline{LOAD}$	$\overline{CET}$	$\overline{CEP}$	$\overline{U/D}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{OE}$	$\overline{RCO}$	CCO	Y_D	Y_C	Y_B	Y_A	
↑	X	X	X	X	H	L	L	H	H	H	L	A/R	A/R	$(Q_T - CP) + 1$				Count Up
↑	X	X	X	X	H	L	L	L	H	H	L	A/R	A/R	$(Q_T - CP) - 1$				Count Down
↑	X	X	X	X	H	H	X	X	H	H	L	H	H	NC	NC	NC	NC	Count Inhibit
↑	X	X	X	X	H	L	H	X	H	H	L	A/R	H	NC	NC	NC	NC	Count Inhibit
Ω	X	X	X	X	X	L	L	H	H	H	L	L	⊓	H	H	H	H	Overflow
↑	X	X	X	X	X	L	H	H	H	H	L	L	H	H	H	H	H	Overflow
↑	X	X	X	X	X	H	X	H	H	H	L	H	H	H	H	H	H	Overflow Inhibit
⊓	X	X	X	X	X	L	L	L	H	H	L	L	⊓	L	L	L	L	Underflow
↑	X	X	X	X	X	L	H	L	H	H	L	L	H	L	L	L	L	Underflow
↑	X	X	X	X	X	H	X	L	H	H	L	H	H	L	L	L	L	Underflow Inhibit
↑	L	H	L	H	L	X	X	X	H	H	L	H	H	L	H	L	H	Load Example
↑	X	X	X	X	X	H	X	H	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
⊓	X	X	X	X	X	L	L	L	H	L	L	L	⊓	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	L	H	L	H	L	L	L	H	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	H	X	L	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
X	X	X	X	X	X	X	X	H	L	X	L	H	H	L	L	L	L	Asynchronous Clear
⊓	X	X	X	X	X	L	L	L	L	X	L	L	⊓	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	L	H	L	L	X	L	L	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	H	X	L	L	X	L	H	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	X	X	X	X	X	H	X	X	Hi-Z				Output Disabled

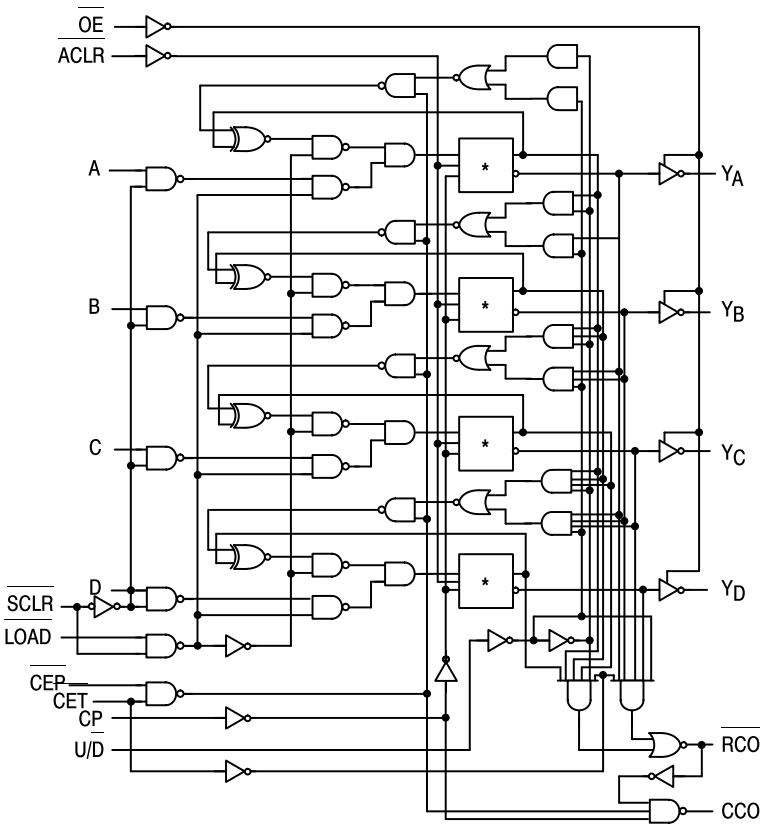
(Q_T — CP) = Output state prior to clock edge
NC = No change

A/R = Assumes required output state; High except during Overflow and Underflow

X = Don't care

LOGIC DIAGRAM

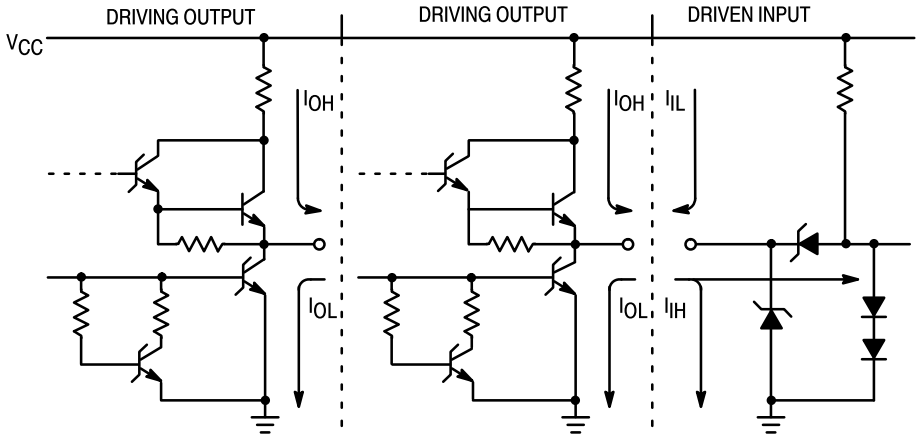




DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.
$\overline{CEP}$	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. CEP must be LOW to count.
$\overline{CET}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
$\overline{LOAD}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
U/$\overline{D}$	Up/Down Count Control. HIGH counts up and LOW counts down.
$\overline{ACLR}$	Asynchronous Clear. Master reset of counters to zero when ACLR is LOW, independent of the clock.
$\overline{SCLR}$	Synchronous clear of counters to zero on the next clock edge when SCLR is LOW.
$\overline{OE}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
Y_A, Y_B, Y_C, Y_D	The four counter outputs.
$\overline{RCO}$	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, RCO is LOW at 0000.
CCO	Clock Carry Output. While counting and RCO is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter			Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage		54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
			74			0.8			
V_{IK}	Input Clamp Diode Voltage				–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	YA–YD	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
			74	2.4	3.1		V		
		RCO, CCO	54	2.5	3.5		V		
			74	2.7	3.5		V		
V_{OL}	Output LOW Voltage		54, 74		0.25	0.4	V	I_{OL} = I_{OL} MAX	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			74		0.35	0.5	V		
I_{OZH}	Output Off Current HIGH					20	μA	V_{CC} = MAX, V_O = 2.7 V	
I_{OZL}	Output Off Current LOW					–20	μA	V_{CC} = MAX, V_O = 0.4 V	
I_{IH}	Input HIGH Current					20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
						0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	Others				–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		$\overline{CET}$				–0.8	mA		
I_{OS}	Short Circuit Current (Note 1)	RCO, CCO		–20		–100	mA	V_{CC} = MAX	
		Others		–30		–130	mA		
I_{CC}	Power Supply Current, 3-State					43	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

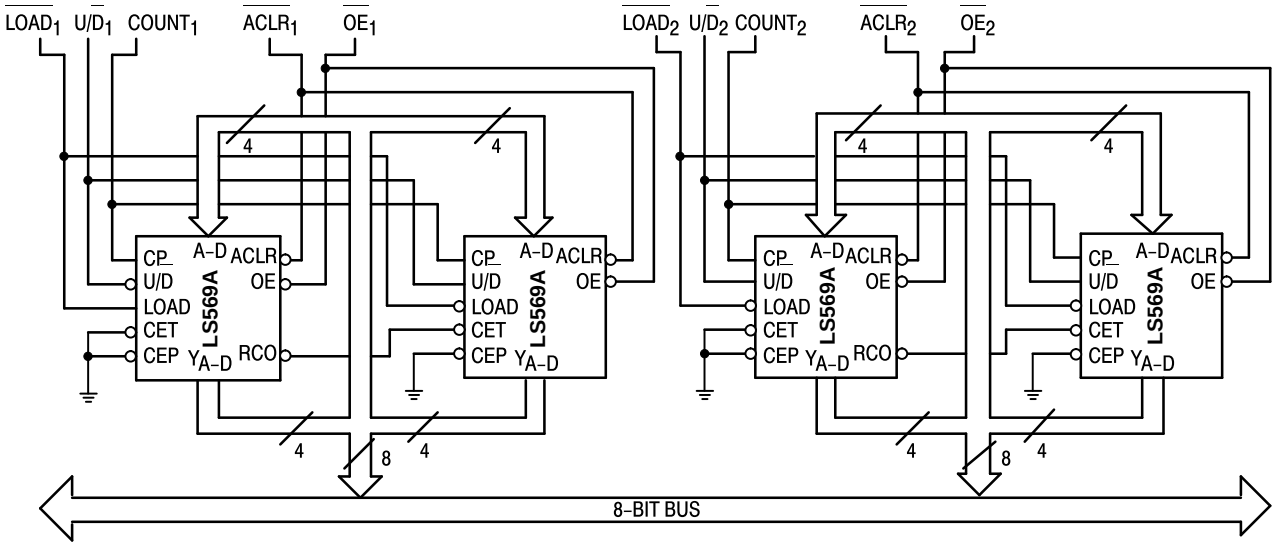
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions

f_{MAX}	Maximum Toggle Frequency	35			MHz	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay Clock to Q			15 20	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to RCO			14 15	ns	
t_{PLH} t_{PHL}	Propagation Delay U/D to RCO			20 24	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to RCO			20 25	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to CCO			16 28	ns	
t_{PLH} t_{PHL}	Propagation Delay CEP to CCO			16 26	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to CCO			15 17	ns	
t_{PLH} t_{PHL}	Propagation Delay ACLR to Q			22 32	ns	
t_{PZH} t_{PZL}	Output Enable Time			15 20	ns	
t_{PHZ} t_{PLZ}	Output Disable Time			20 27	ns	C_L = 5.0 pF

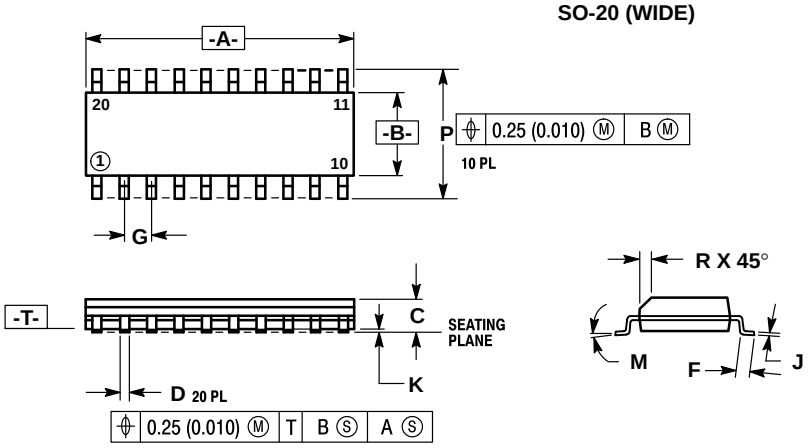
AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width (Low)	20			ns	V_{CC} = 5.0 V
t_s	Setup Time, A, B, C, D	20			ns	
t_s	Setup Time, $\overline{SCLR}$	20			ns	
t_s	Setup Time, $\overline{LOAD}$	25			ns	
t_s	Setup Time, U/$\overline{D}$	30			ns	
t_s	Setup Time, CET, $\overline{CEP}$	20			ns	
t_h	Hold Time, Any Inputs	0			ns	
t_{rec}	ACLR	15			ns	

MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS



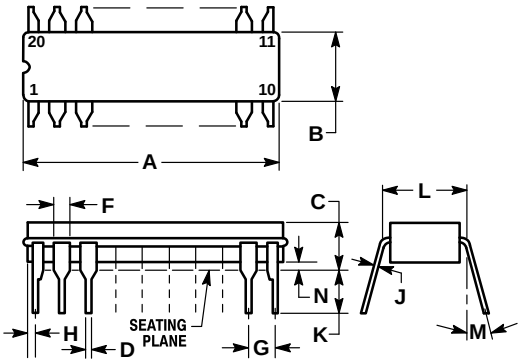
Case 751D-03 DW Suffix
20-Pin Plastic
SO-20 (WIDE)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

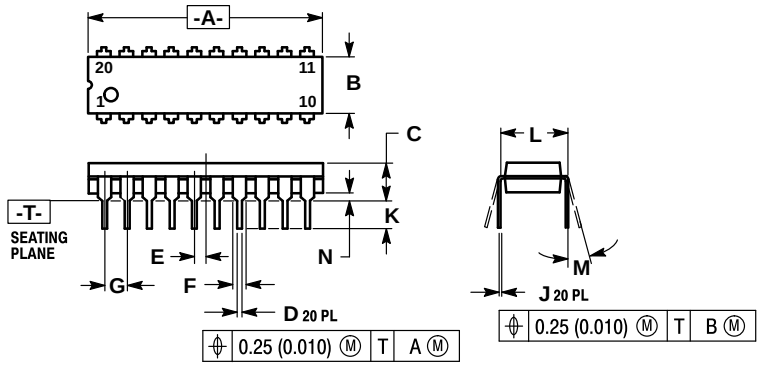
Case 732-03 J Suffix
20-Pin Ceramic Dual In-Line



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

Case 738-03 N Suffix
20-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

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ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed