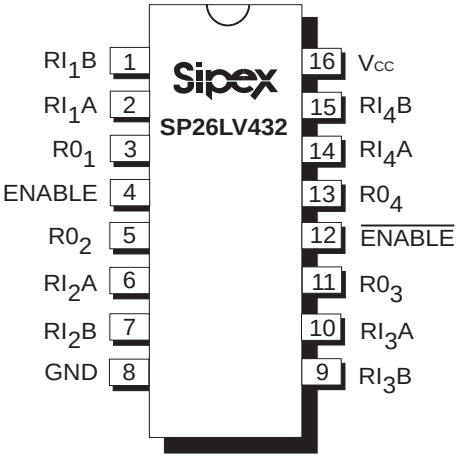
High Speed, Low Power Quad RS-422 Differential Line Receiver

- Quad Differential Line Receivers
- Compatible with the EIA standard for RS-422 serial protocol
- High-Z Output Control
- 14ns Typical Receiver Propagation Delays
- 60mV Typical Input Hysteresis
- Single +3.3V Supply Operation
- Common Receiver Enable Control
- Compatibility with the industry standard 26LV32
- -7.0V to +7.0V Common-Mode Input Voltage Range
- Switching Rates Up to 50Mbps
- Ideal for use with SP26LV431 Quad Drivers

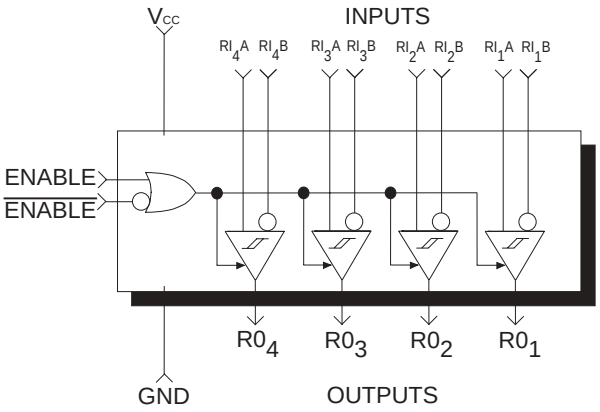


DESCRIPTION

The **SP26LV432** is a quad differential line receiver with 3-State outputs designed to meet the specifications of RS-422. The **SP26LV432** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol over 50Mbps under load. The RS-422 protocol allows up to 10 receivers to be connected to a multipoint bus transmission line. The **SP26LV432** features a receiver enable control common to all four receivers and a high-Z output with 6mA source and sink capability. Since the cabling can be as long as 4,000 feet, the RS-422 receivers of the **SP26LV432** are equipped with a wide (-7.0V to +7.0V) common-mode input voltage range to accommodate ground potential differences.

TYPICAL APPLICATION CIRCUIT

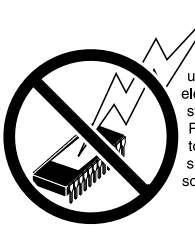
ENABLE	ENABLE	Input	Output
LOW	HIGH	don't care	high-Z
HIGH	don't care	$V_{ID} \geq V_{TH}$ (max)	HIGH
HIGH	don't care	$V_{ID} \leq V_{TH}$ (min)	LOW
don't care	LOW	$V_{ID} \geq V_{TH}$ (max)	HIGH
don't care	LOW	$V_{ID} \leq V_{TH}$ (min)	LOW
HIGH	don't care	open	HIGH
don't care	LOW	open	HIGH



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC} (Supply Voltage) ..... +7.0V
V_{CM} (Common Mode Range) ..... ±14V
V_{DIFF} (Differential Input Voltage) ..... ±14V
V_{IN} (Enable Input Voltage) ..... V_{CC} + 1.5V
T_{STG} (Storage Temperature Range) ..... -65°C to +150°C
Lead Temperature (4sec) ..... +260°C
Maximum Current Per Output ..... ±25mA
Storage Temperature ..... -65°C to +150°C
Power Dissipation Per Package
16-pin PDIP (derate 14.3mW/°C above +70°C) 1150mW
16-pin NSOIC (derate 8.95mW/°C above +70°C) 725mW



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

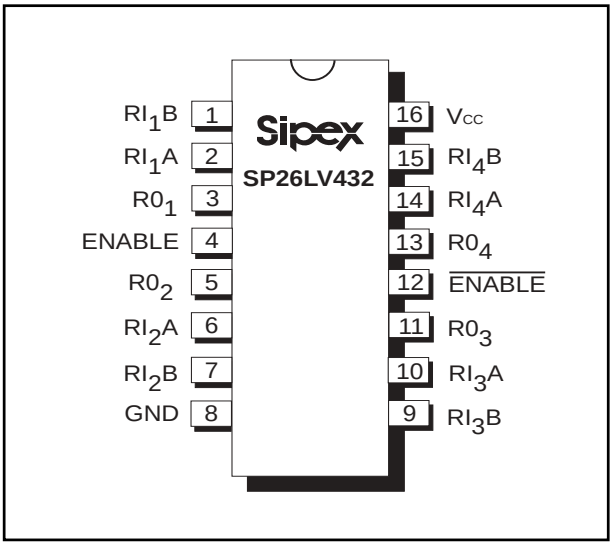
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +3.6V with T_{amb} = 25°C and all MIN and MAX limits apply across the recommended operating temperature range.

DC PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage, V_{CC}	3.0		3.6	V	
Enable Input Rise or Fall Times		3		ns	
Input Electrical Characteristics					
Minimum Differential Input Voltage, V_{TH}	-200	50	+200	mV	$V_{OUT} = V_{OH}$ or V_{OL}, $-7V < V_{CM} < +7V$
Input Resistance, R_{IN}	5.0			KΩ	V_{IN} = -7V, +7V, +10V other input = GND
Input Current					
I_{IN}		+1.25	+1.5	mA	V_{IN} = +10V, other input = GND
I_{IN}		-1.5	-2.5	mA	V_{IN} = -10V, other input = GND
Minimum Enable HIGH Input Level Voltage, $V_{IH(EN)}$	2.0			V	
Maximum Enable LOW Input Level Voltage, $V_{IL(EN)}$			0.8	V	
Maximum Enable Input Current, I_{EN}		±1.0		µA	$V_{IN} = V_{CC}$ or GND
Input Hysteresis, V_{HYST}		60		mV	V_{CM} = 0V
Quiescent Supply Current, I_{CC}		5	15	mA	V_{CC} = +3.3V, V_{DIF} = +1V
Output Electrical Characteristics					
Minimum High Level Output Voltage, V_{OH}	2.4	2.8		V	V_{CC} = +3.0V, V_{DIFF} = +1V, I_{OUT} = -6mA
Maximum Low Level Output Voltage, V_{OL}		0.2	0.5	V	V_{CC} = +3.0V, V_{DIFF} = -1V, I_{OUT} = +6mA
Maximum Tri-state Output Leakage Current, I_{OZQ}		±0.5	±5.0	µA	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL}, ENABLE = V_{IH}

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +3.6V, T_{amb} = 25°C, $t_r \leq 6$ns, $t_f \leq 6$ns, and all MIN and MAX limits apply across the recommended operating temperature range.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SWITCHING CHARACTERISTICS					
Propagation Delays, t_{PLHD}, t_{PHLD}		11	18	ns	Figure 3
Skew		0.8	2	ns	Figure 3, Note 4
Differential Ouput Rise and Fall Times, t_{TLH}, t_{PHL}		4	10	ns	Figure 3
Output Enable Time, t_{PZH}			40	ns	Figure 5
Output Enable Time, t_{PZL}			40	ns	Figure 5
Output Disable Time, t_{PHZ}			35	ns	Figure 5, Note 5
Output Disable Time, t_{PLZ}			35	ns	Figure 5, Note 5
Power dissipation Capacitance, C_{PD}		50		pF	Note 6
Input Capacitance, C_{IN}		6		pF	



PINOUT

PIN DESCRIPTION

PIN NUMBER	PIN NAME	DESCRIPTION
1	RI_1B	Inverted RS-422 receiver input.
2	RI_1A	Non-inverted RS-422 receiver input.
3	$R0_1$	TTL receiver output.
4	ENABLE	Receiver input enable, active HIGH.
5	$R0_2$	TTL receiver output.
6	RI_2A	Non-inverted RS-422 receiver input.
7	RI_2B	Inverted RS-422 receiver input.
8	GND	Ground.
9	RI_3B	Inverted RS-422 receiver input.
10	RI_3A	Non-inverted RS-422 receiver input.
11	$R0_3$	TTL receiver output.
12	$\overline{ENABLE}$	Receiver input enable, active LOW.
13	$R0_4$	TTL receiver output.
14	RI_4A	Non-inverted RS-422 receiver input.
15	RI_4B	Inverted RS-422 receiver input.
16	V_{CC}	+3.0V to +3.6V power supply.

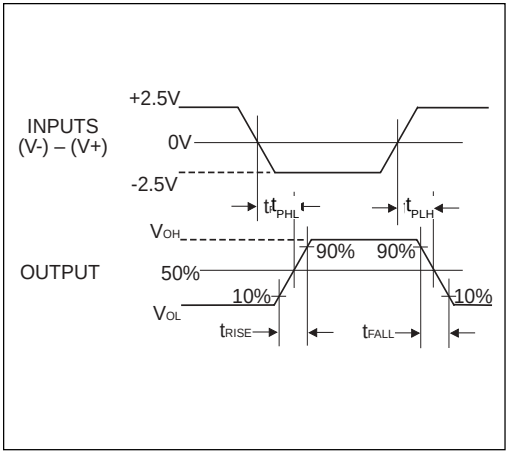


Figure 2. Propagation Delay

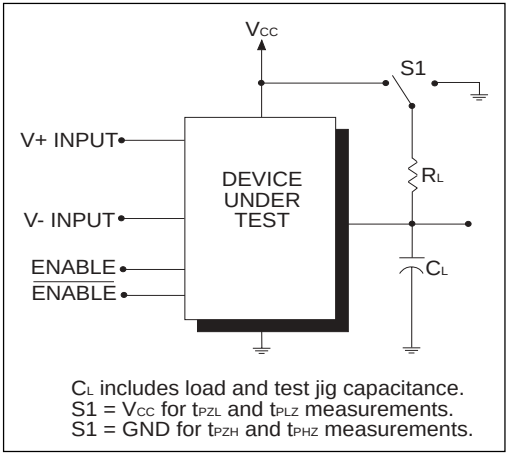


Figure 3. Test Circuit for high-Z Output Timing

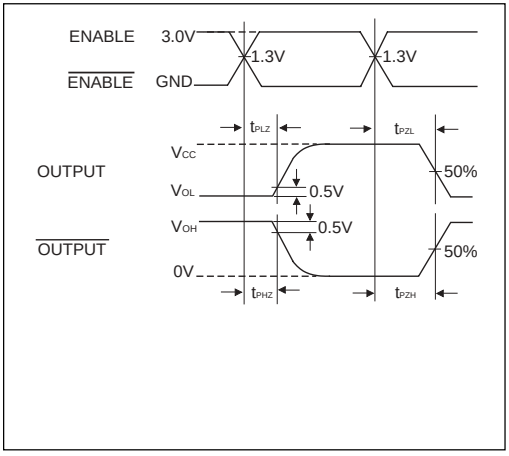


Figure 4. High Impedance Output Enable and Disable Waveforms

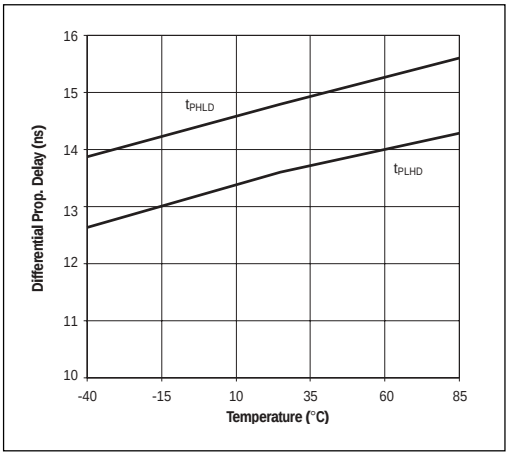


Figure 5. Differential Propagation Delay vs Temperature

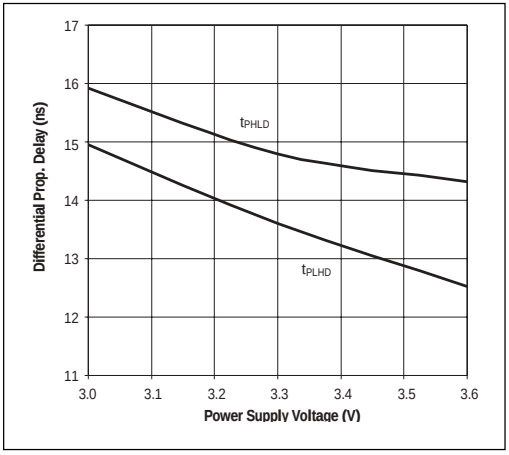


Figure 6. Differential Propagation Delay vs Supply Voltage

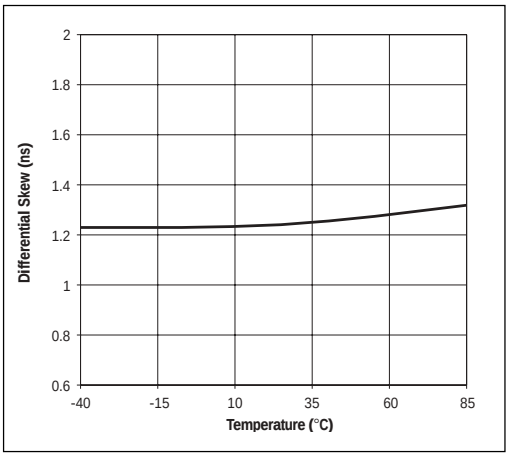


Figure 7. Differential Skew vs Temperature

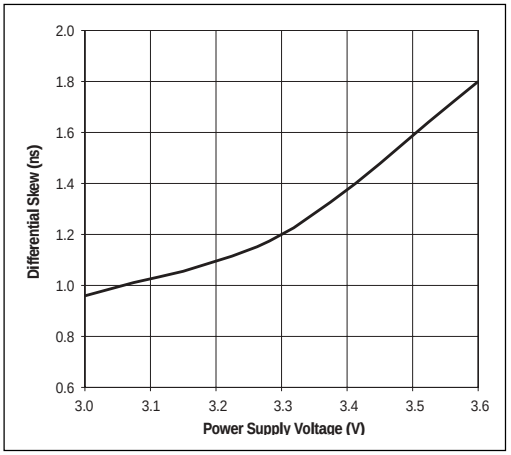


Figure 8. Differntial Skew vs Supply Voltage

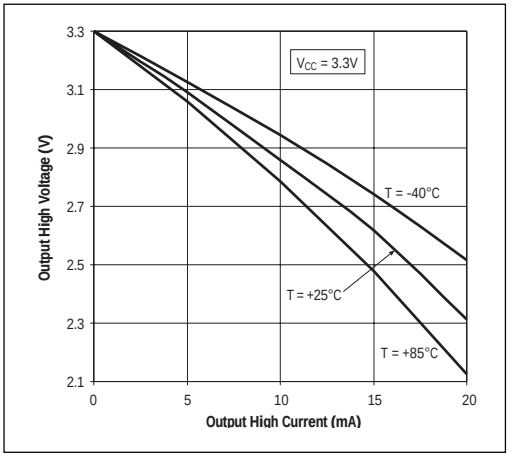


Figure 9. High Output Voltage vs Current over Temperature

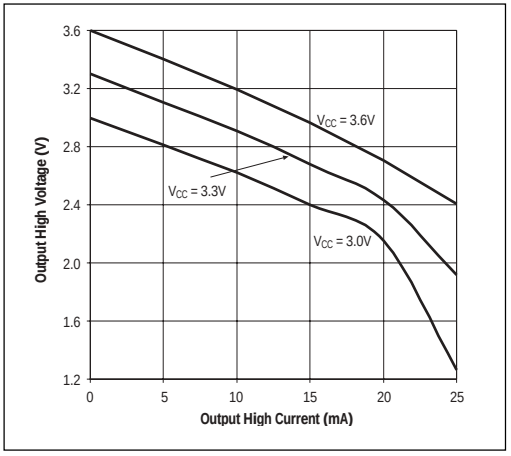


Figure 10. High Output Voltage vs Current over Supply Voltage

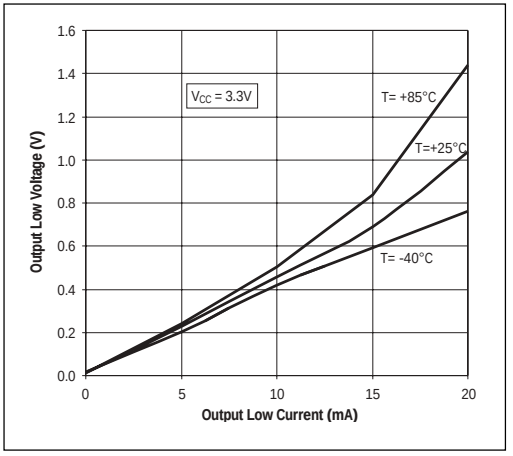


Figure 11. Low Output Voltage vs Current over Temperature

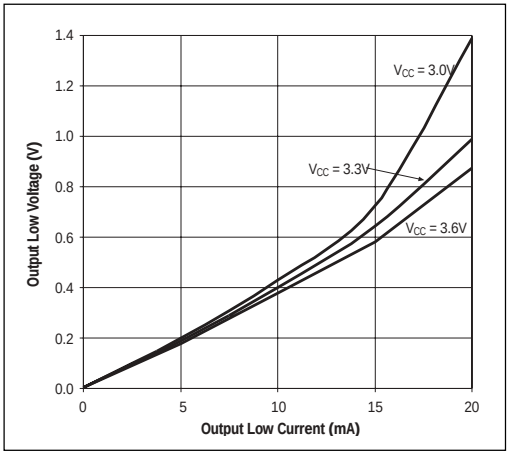


Figure 12. Low Output Voltage vs Current over Supply Voltage

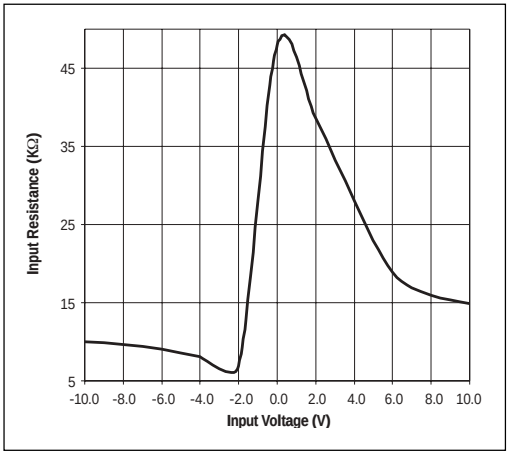


Figure 13. Input Resistance vs Input Voltage

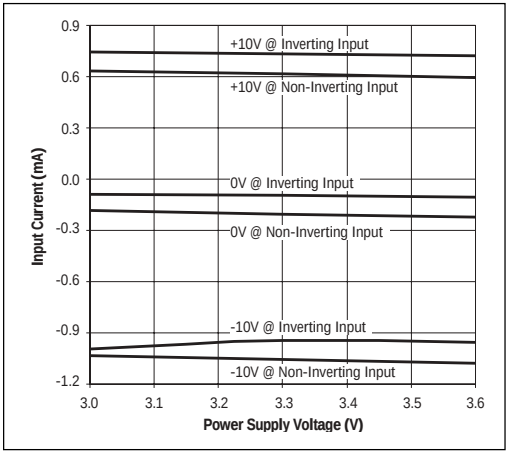


Figure 14. Input Current vs Supply Voltage

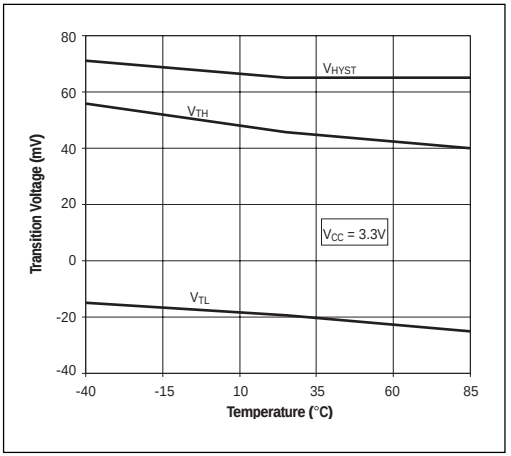


Figure 15. Transition Voltage vs Temperature

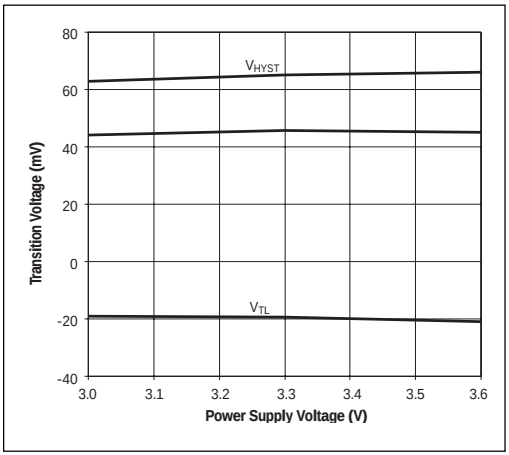


Figure 16. Transition Voltage vs Supply Voltage

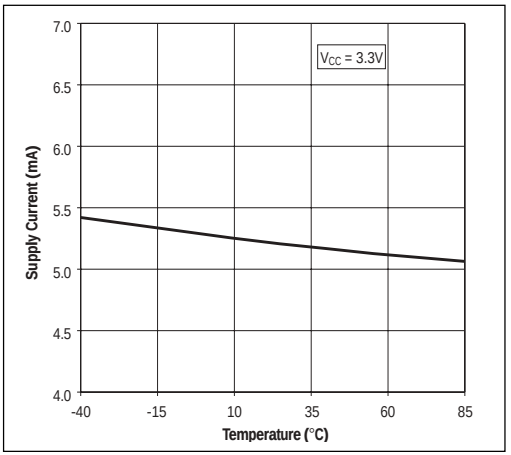


Figure 17. Supply Current vs Temperature

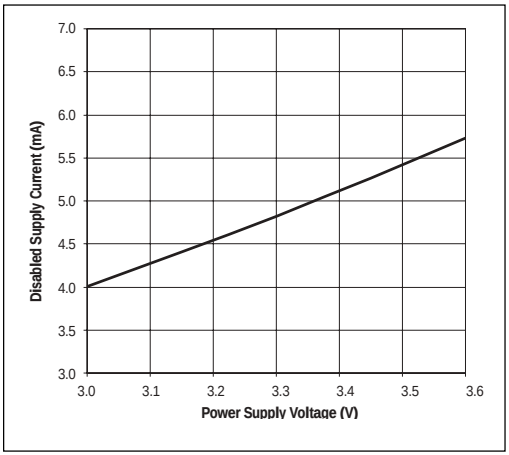


Figure 18. Disabled Supply Current vs Supply Voltage

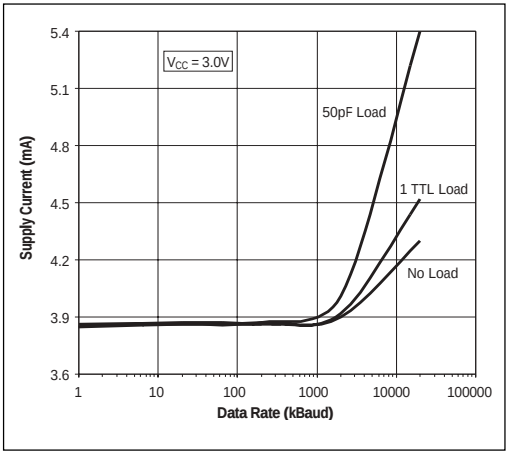


Figure 19. Supply Current vs Data Rate

The **SP26LV432** is a low-power quad differential line receiver designed for digital data transmission meeting specifications of the EIA standard RS-422 protocol. The **SP26LV432** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol to at least 50Mbps under load in harsh environments.

The RS-422 standard is ideal for multi-drop applications and for long-distance communication. The RS-422 protocol allows up to 10 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, the RS-422 receivers have an input sensitivity of 200mV over the wide (-7.0V to +7.0V) common mode range to accommodate ground potential differences. Internal pull-up and pull-down resistors prevent output oscillation on unused channels. Because the RS-422 is a differential interface, data is virtually immune to noise in the transmission line.

The **SP26LV432** accepts RS-422 levels and translates these into TTL or CMOS input levels. The **SP26LV432** features active HIGH and active LOW receiver enable controls common to all four receiver channels. A logic HIGH on the ENABLE pin (pin 4) or a logic LOW on the $\overline{\text{ENABLE}}$ pin (pin 12) will enable the differential receiver outputs. A logic LOW on the ENABLE pin (pin 4) and a logic HIGH on the $\overline{\text{ENABLE}}$ pin (pin 12) will force the receiver outputs into high impedance (high-Z). Refer to the truth table in *Figure 20*.

The RS-422 line receivers feature high source and sink current capability. All receivers are internally protected against short circuits on their inputs. The receivers feature tri-state outputs with 6mA source and sink capability. The typical receiver propagation delay is 14ns (35ns max).

To minimize reflections, the multipoint bus transmission line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
LOW	HIGH	don't care	high-Z
HIGH	don't care	$V_{ID} \geq V_{TH}$ (max)	HIGH
HIGH	don't care	$V_{ID} \leq V_{TH}$ (min)	LOW
don't care	LOW	$V_{ID} \geq V_{TH}$ (max)	HIGH
don't care	LOW	$V_{ID} \leq V_{TH}$ (min)	LOW
HIGH	don't care	open	HIGH
don't care	LOW	open	HIGH

Figure 20. Truth Table, Enable/Disable Function Common to all Four RS-422 Receivers

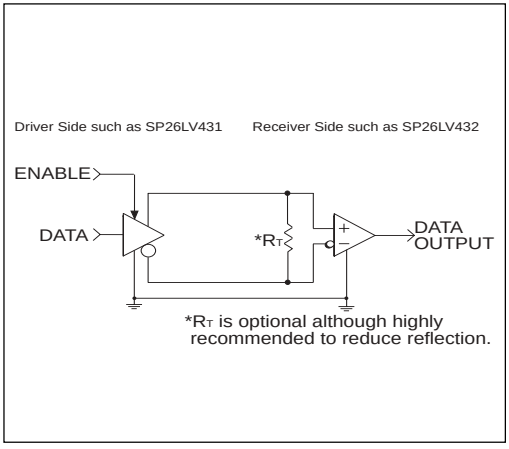
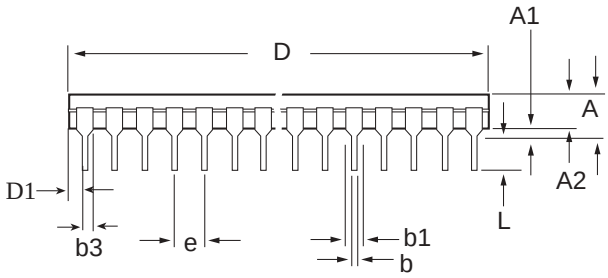
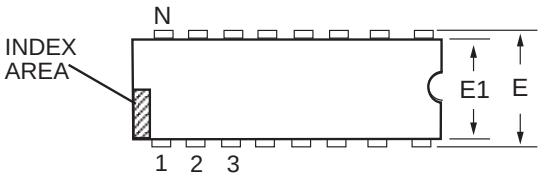
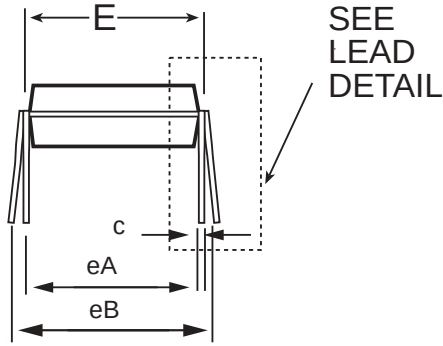


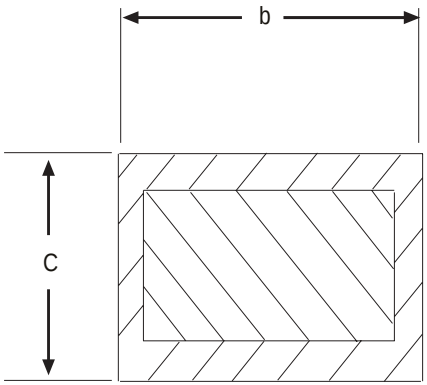
Figure 21. Two-Wire Balanced Systems, RS-422



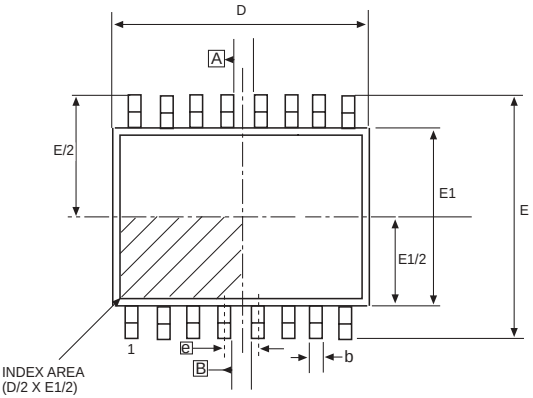


Dimensions in (mm)	16 PIN PDIP JEDEC MS-001 (BB) Variation		
	MIN	NOM	MAX
A	-	-	.210
A1	.015	-	-
A2	.115	.130	.195
b	.014	.018	.022
b2	.045	.060	.070
b3	.030	.039	.045
c	.008	.010	.014
D	.735	.755	.775
D1	.005	-	-
E	.300	.310	.325
E1	.240	.250	.280
e	.100 BSC		
eA	.300 BSC		
eB	-	-	.430
L	.115	.130	.150

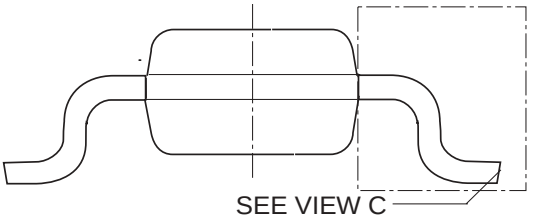


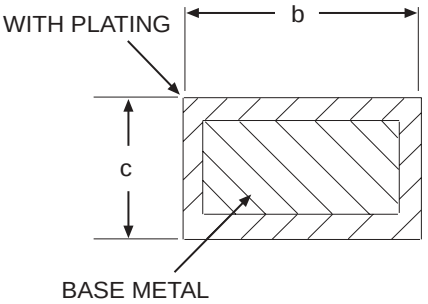


16 pin PDIP

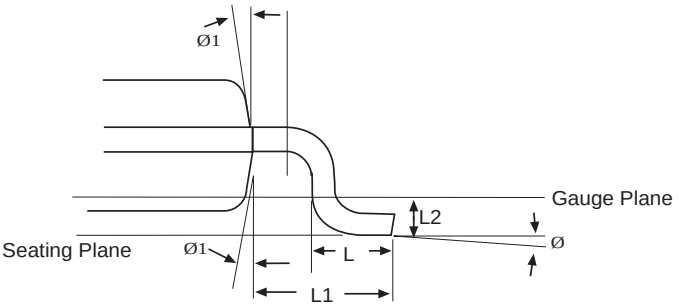


TOP VIEW

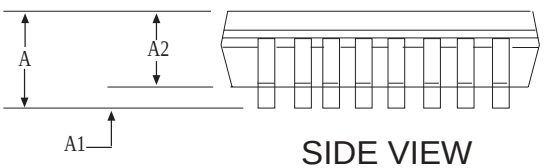




CONTACT AREA



VIEW C



SIDE VIEW

DIMENSIONS Minimum/Maximum (mm)	16 Pin NSOIC (JEDEC MS-012, AC - VARIATION)		
COMMON HEIGHT DIMENSION			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
Ø	0º	-	8º
Ø1	5º	-	15º

16 PIN NSOIC

ORDERING INFORMATION

Model	Temperature Range	Package
SP26LV432CP	0°C to +70°C	16–pin PDIP
SP26LV432CN	0°C to +70°C	16–pin NSOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
3/08/04	A	Production Release.

ANALOG EXCELLENCE

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