

QUINT DIFFERENTIAL LINE RECEIVER

FEATURES

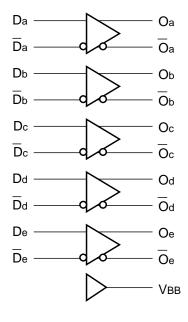
- Max. propagation delay of 900ps
- **■** Differential outputs
- IEE min. of -60mA
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- More than twice as fast as Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S314 offers five differential line receivers with emitter follower outputs, designed for use in high-performance ECL systems. For single-ended operation, the VBB reference voltage is available. In the single-ended mode, the apparent input threshold of the true inputs is 30mV higher than the threshold of the complementary inputs.

Common mode rejection of +1.0V is achieved through the use of active current sources. If both the true and complement inputs are at the same potential between VEE and VCC, then the complementary outputs will take on a logic HIGH state. Unlike the other members of the Synergy 300K family, the inputs on this device do not have pull-down resistors.

BLOCK DIAGRAM

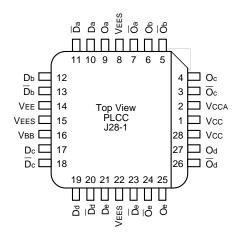


PIN NAMES

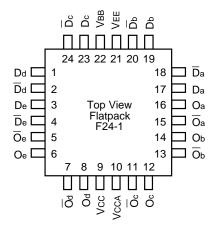
Pin	Function
Da – De	Data Inputs
D̄a − D̄e	Inverting Data Inputs
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

Micrel, Inc. SY100S314

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S314FC	F24-1	Commercial	SY100S314FC	Sn-Pb
SY100S314FCTR ⁽¹⁾	F24-1	Commercial	SY100S314FC	Sn-Pb
SY100S314JC	J28-1	Commercial	SY100S314JC	Sn-Pb
SY100S314JCTR ⁽¹⁾	J28-1	Commercial	SY100S314JC	Sn-Pb
SY100S314JZ ⁽²⁾	J28-1	Commercial	SY100S314JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S314JZTR ^(1, 2)	J28-1	Commercial	SY100S314JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

O = D

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
VDIFF	Input Voltage Differential	150	_	_	mV	Required for Full Output Swing
Vсм	Common Mode Voltage	_	_	1.0	V	Permissible ±VcM with Respect to VBB
Іін	Input HIGH Current	_	_	50	μΑ	VIN = VIH (Max.), Da - De = VBB, \overline{D} a - \overline{D} e = VIL (Min.)
Ісво	Input Leakage Current	-10	_	_	μА	$VIN = VEE$, $Da - De = VBB$, $\overline{Da} - \overline{De} = VIL$ (Min.)
lee	Power Supply Current	-60	-45	-30	mA	Da - De = VBB, Da - De = VIL (Min.)

AC ELECTRICAL CHARACTERISTICS

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

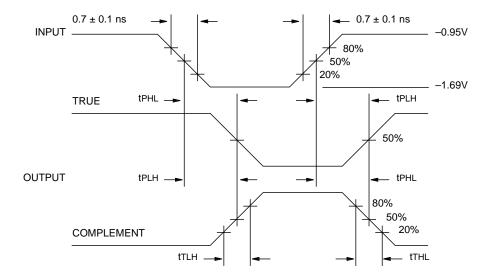
		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = 0°C		TA = +25°C		Ta = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



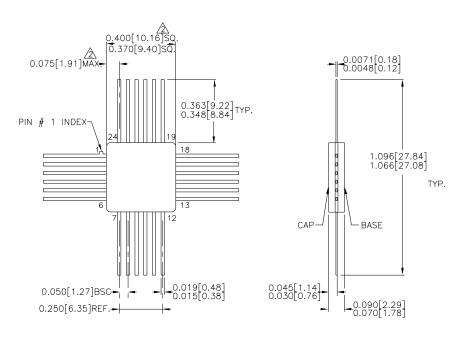
Propagation Delay and Transition Times

Note:

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Micrel, Inc. SY100S314

24-PIN CERPACK (F24-1)



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].

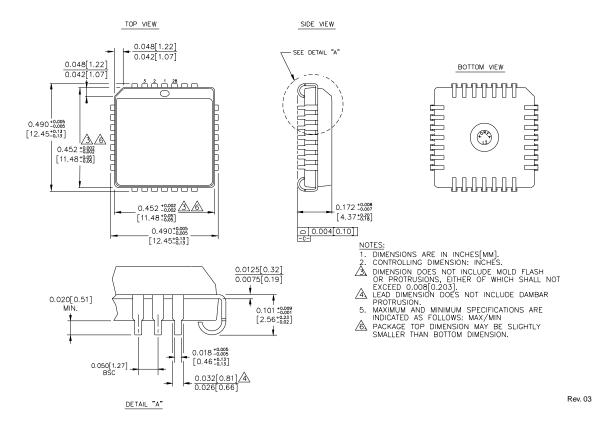
ATHIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

Micrel, Inc. SY100S314

28-PIN PLCC (J28-1)



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