LOW POWER HEX TTL-to-ECL TRANSLATOR

SY100S324

FEATURES

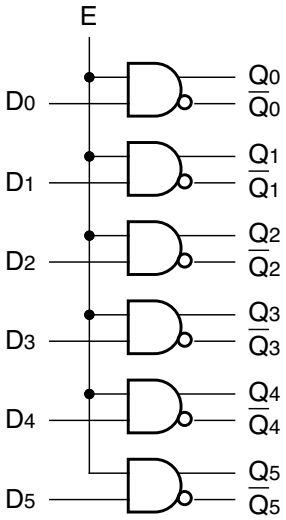
- **Max. propagation delay of 1.4ns**
- **I_{EE} min. of –70mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Differential outputs**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **Twice as fast as Fairchild's 324**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

DESCRIPTION

The SY100S324 is a hex translator designed to convert TTL logic levels to 100K ECL levels. The inputs are TTL compatible with differential outputs that can either be used as an inverting/non-inverting translator or as differential line drivers. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all non-inverting outputs LOW.

When used in the differential mode, due to its high common mode rejection, it overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

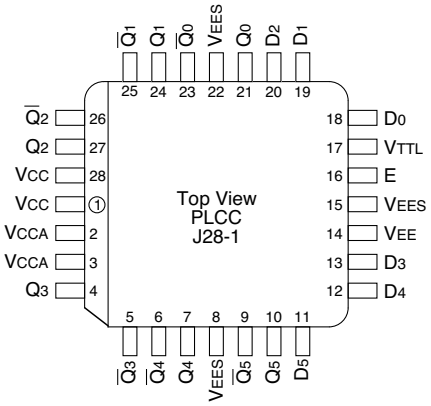
BLOCK DIAGRAM



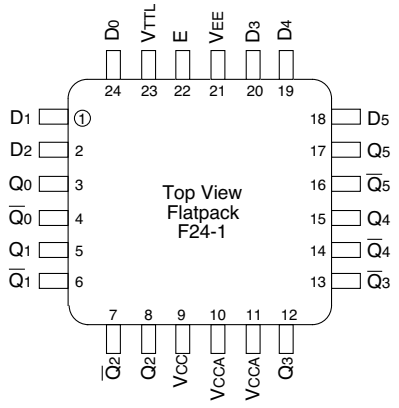
PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
E	Enable Inputs
Q_0–Q_5	Data Outputs
$\overline{Q_0}$–$\overline{Q_5}$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{TTL}	TTL V_{CC} Power Supply
V_{CCA}	V_{CCO} for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S324FC	F24-1	Commercial	SY100S324FC	Sn-Pb
SY100S324FCTR[1]	F24-1	Commercial	SY100S324FC	Sn-Pb
SY100S324JC	J28-1	Commercial	SY100S324JC	Sn-Pb
SY100S324JCTR[1]	J28-1	Commercial	SY100S324JC	Sn-Pb
SY100S324JY[2]	J28-1	Industrial	SY100S324JY with Pb-Free bar-line indicator	Matte-Tin
SY100S324JYTR[1, 2]	J28-1	Industrial	SY100S324JY with Pb-Free bar-line indicator	Matte-Tin

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Sim.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–986	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with 50Ω
V_{OL}	Output LOW Voltage	–1810	–1674	–1620	mV	V_{IN} = V_{IL} (Min.)	
V_{OHC}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage	—	—	–1610	mV	V_{IN} = V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0	—	0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	—	—	–1.5	V	I_{IN} = –10mA	
I_{IH}	Input HIGH Current Data Enable	 — —	 — —	 20 120	 μA	 V_{IN} = +2.4V All Other Inputs V_{IN} = GND	
I_{IH}	Input HIGH Current Breakdown Test, All Inputs	—	—	1.0	mA	V_{IN} = +5.5V, V_{TTL} = Max., All Other Inputs V_{IN} = GND	
I_{IL}	Input LOW Current Data Enable	 –1.2 –6.7	 — —	 — —	 mA	 V_{IN} = +0.4V All Other Inputs V_{IN} = V_{IH}	
I_{EE}	V_{EE} Power Supply Current	–70	–45	–28	mA	All Inputs V_{IN} = +4.0V	
I_{TTL}	V_{TTL} Power Supply Current	—	25	35	mA	All Inputs V_{IN} = GND	

AC ELECTRICAL CHARACTERISTICS

PLCC /FLATPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	400	850	1400	ps	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	350	—	1700	ps	

SWITCHING WAVEFORM

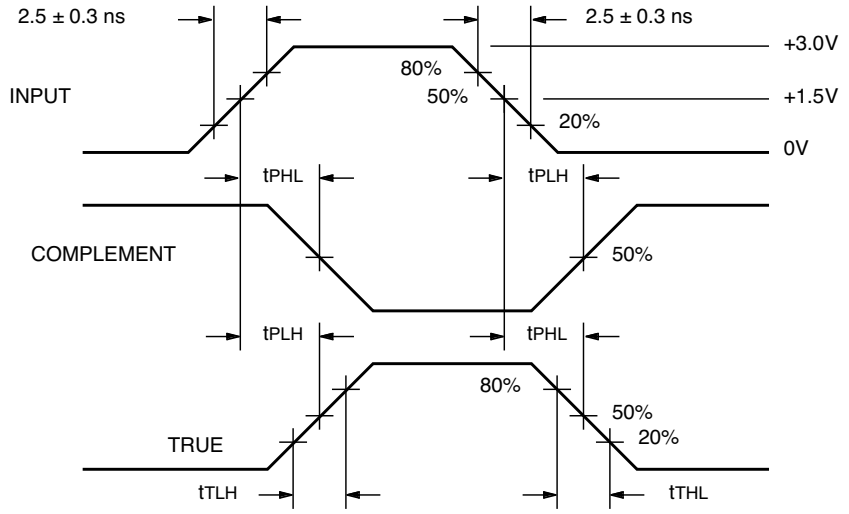


Figure 1. Propagation Delay and Transition Times

Note:

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

TEST CIRCUIT

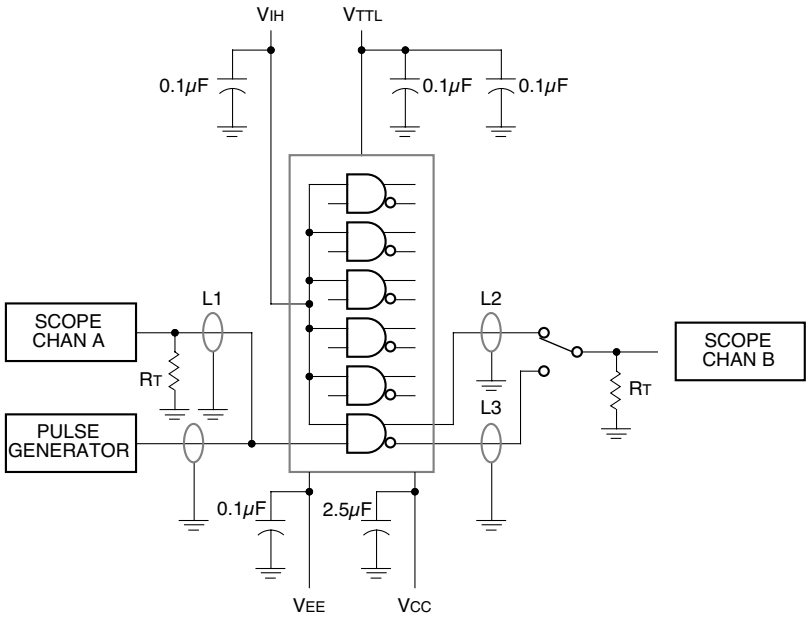


Figure 2. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V, V_{TTL} = +7.0V, V_{IH} = +6.0V

L1, L2 and L3 = equal length 50Ω impedance lines

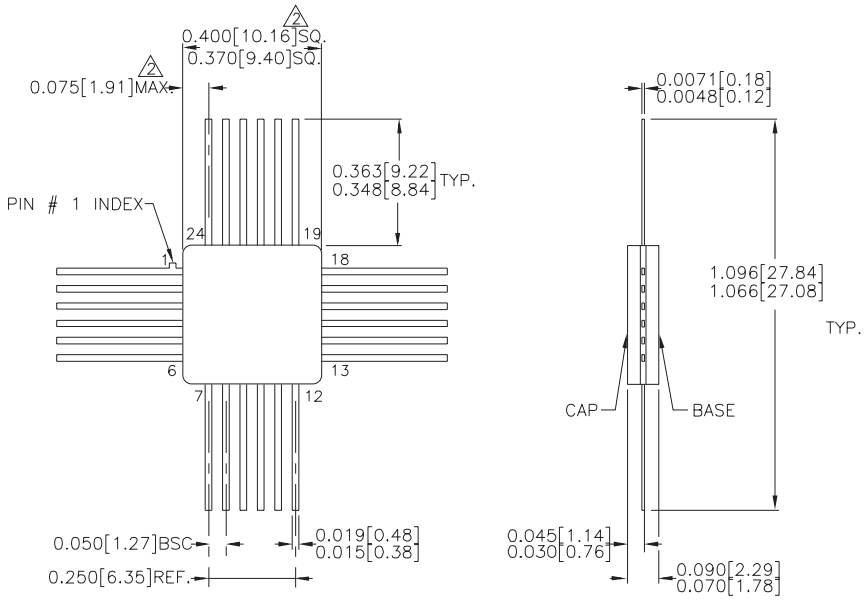
R_T = 50Ω terminator internal to scope

Decoupling 0.1μF from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3pF

24-PIN CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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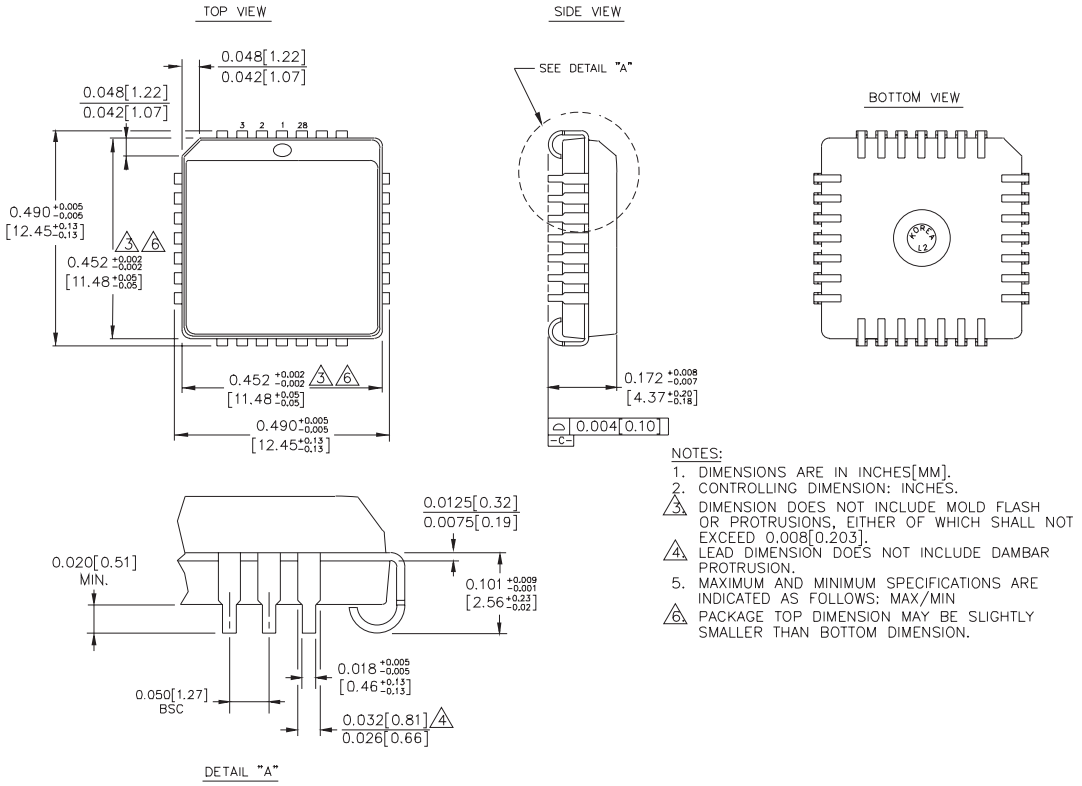
28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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