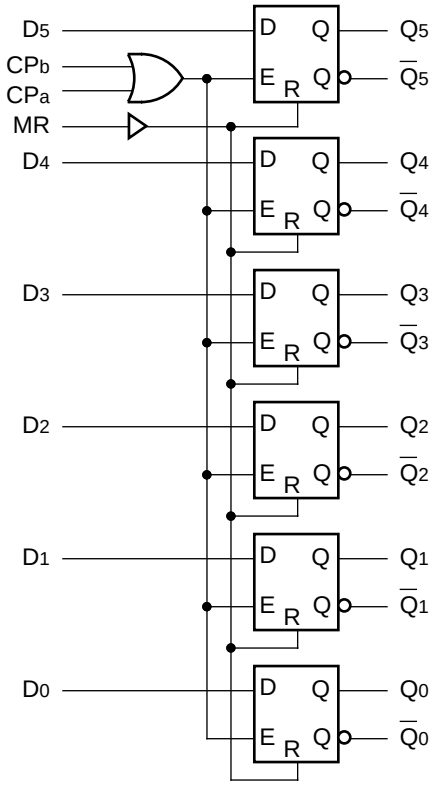
FEATURES

- **Max. toggle frequency of 700MHz**
- **Clock to Q max. of 1200ps**
- **I_{EE} min. of –98mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than Fairchild 300K**
- **Better than 20% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

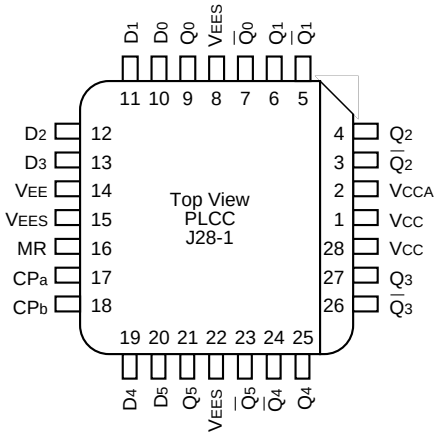
DESCRIPTION

The SY100S351 offers six D-type, edge-triggered, master/slave flip-flops with differential outputs, and is designed for use in high-performance ECL systems. The flip-flops are controlled by the signal from the logical OR operation on a pair of common clock signals (CP_a, CP_b). Data enters the master when both CP_a and CP_b are LOW and transfers to the slave when either CP_a or CP_b (or both) go to a logic HIGH. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

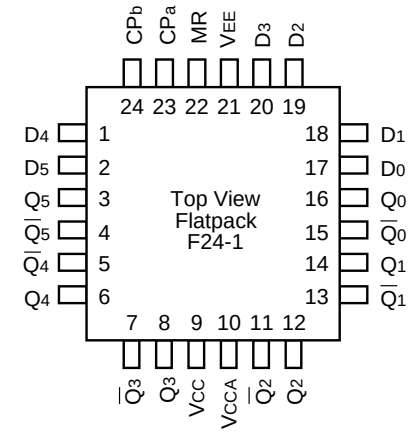
BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S351FC	F24-1	Commercial	SY100S351FC	Sn-Pb
SY100S351FCTR[1]	F24-1	Commercial	SY100S351FC	Sn-Pb
SY100S351JC	J28-1	Commercial	SY100S351JC	Sn-Pb
SY100S351JCTR[1]	J28-1	Commercial	SY100S351JC	Sn-Pb
SY100S351JZ[2]	J28-1	Commercial	SY100S351JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S351JZTR[1, 2]	J28-1	Commercial	SY100S351JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
D_0 — D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0 — Q_5	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_5$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLES

Asynchronous Operation[1]				
Inputs				Outputs
D_n	CP_a	CP_b	MR	Q_n (t+1)
X	X	X	H	L

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   t = Time before CP Positive Transition
   t+1 = Time after CP Positive Transition
   u = LOW-to-HIGH Transition

Synchronous Operation[1]				
Inputs				Outputs
D_n	CP_a	CP_b	MR	Q_n (t+1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Q_n(t)
X	u	H	L	Q_n(t)
X	L	L	L	Q_n(t)

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	MR	—	—	270		
	D_0 – D_5	—	—	200		
	CP_a, CP_b	—	—	300		
I_{EE}	Power Supply Current	–98	–71	–49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

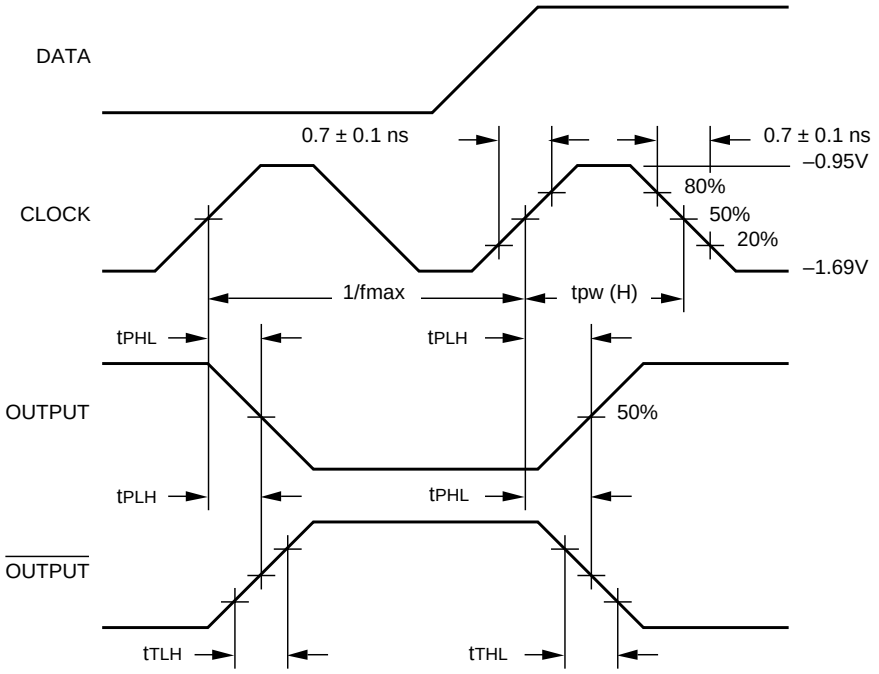
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	—	1200	—	1200	—	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time D_0–D_5 MR (Release Time)	 500 1000	 — —	 500 1000	 — —	 500 1000	 — —	ps	
t_H	Hold Time, D_0–D_5	550	—	550	—	550	—	ps	
t_{PW} (H)	Pulse Width HIGH CP_a, CP_b, MR	1000	—	1000	—	1000	—	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

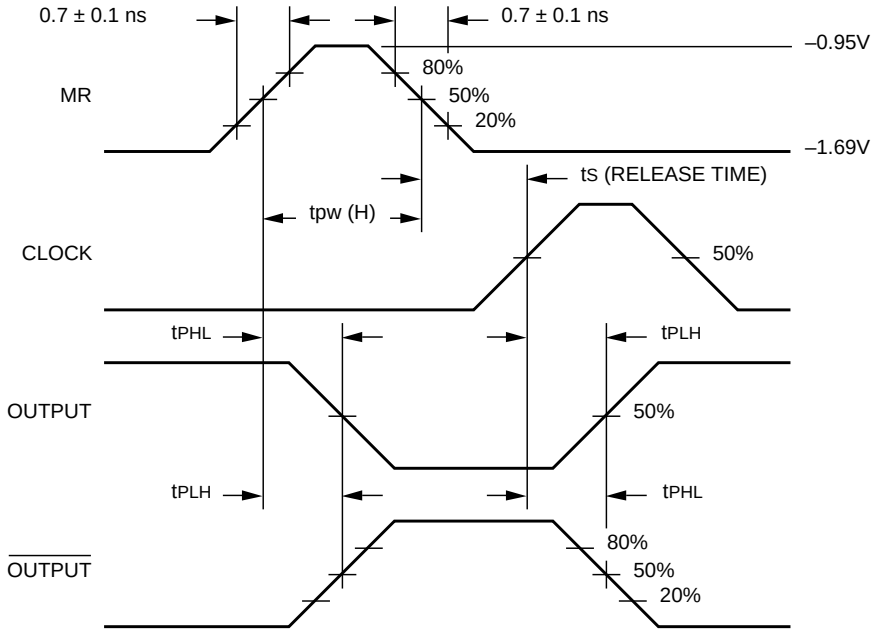
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	—	1200	—	1200	—	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time D_0–D_5 MR (Release Time)	 500 1000	 — —	 500 1000	 — —	 500 1000	 — —	ps	
t_H	Hold Time, D_0–D_5	550	—	550	—	550	—	ps	
t_{PW} (H)	Pulse Width HIGH CP_a, CP_b, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS



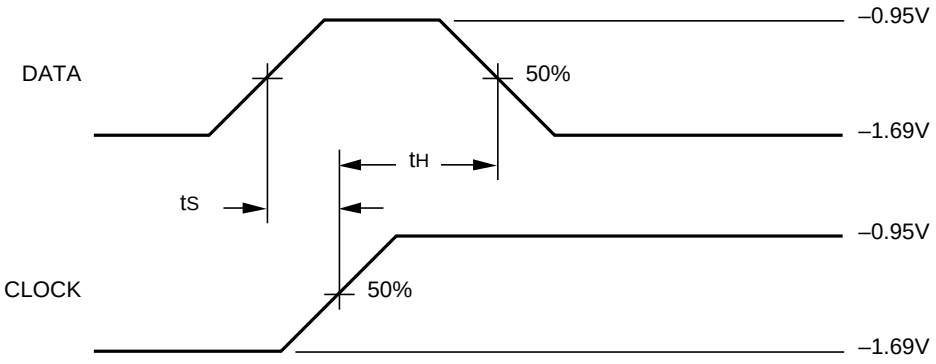
Propagation Delay (Clock) and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND



Propagation Delay (Resets)

TIMING DIAGRAMS

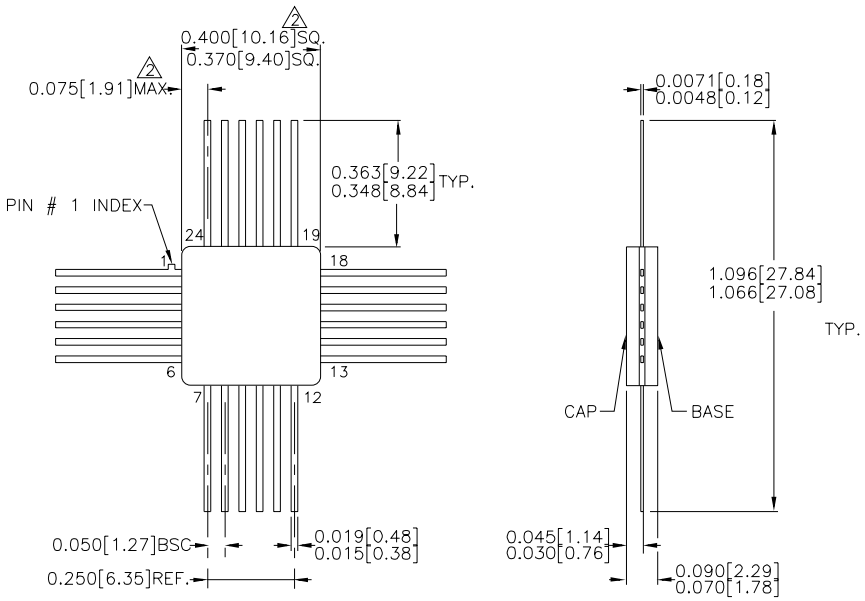


Data Set-up and Hold Time

Notes:

1. V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND
2. t_S is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

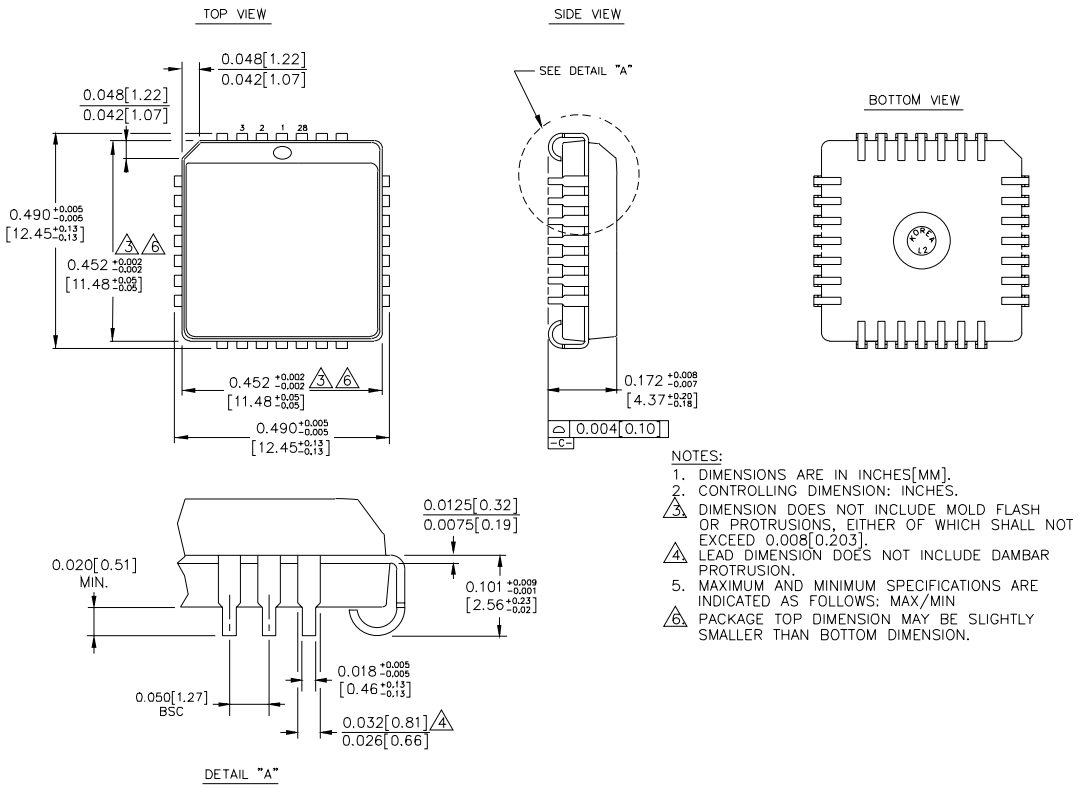
24-PIN CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



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