AccessRunner™
ADSL Modem Device Set for PCI Applications

Controller-less, Scalable, Discrete Multitone-based, G.dmt- and G.lite-compliant, ADSL Modem Device Set for PCI Applications

Conexant's AccessRunner™ ADSL modem device set is compliant with the full-rate ANSI T1.413 Issue 2 and ITU G.dmt (G.992.1) ADSL standards, and with the splitterless ITU G.lite (G.992.2) specification. This rate-adaptive solution is designed for controller-less PCI desktop applications and supports downstream data rates of up to 8 Mbps and upstream data rates of up to 1 Mbps.

The device set takes advantage of the processing power available with most new computers by eliminating the need for a separate microcontroller, resulting in a cost-effective solution suitable for both G.dmt and G.lite applications. Host-based software provides support for current industry standards for PPP over AAL5 over ATM over ADSL and RFC 1483 for Windows 98 and Windows 2000.

The device set, as shown in Figure 1, consists of four chips:

- PCI bus interface (AccessRunner P46 in a 176-pin TQFP)
- DMT-based data pump (AccessRunner 11627 in a 176-pin TQFP)
- Analog front end (AccessRunner 20431 in a 32-pin TQFP)
- Line driver (AccessRunner 20441 in a 16-pin SSOP or 32-pin TQFP)

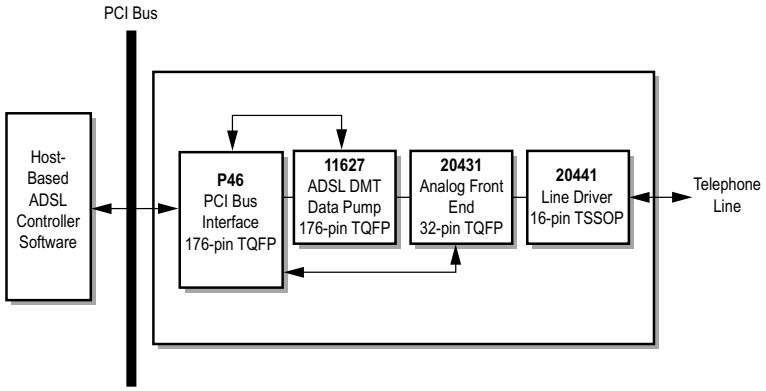


Figure 1. AccessRunner ADSL Modem for PCI Applications

Features

- Complete controller-less PCI ADSL solution
- Compliant with ADSL standards
  - Full-rate ANSI T1.413 Issue 2 and ITU G.dmt (G.992.1) standards
  - Splitterless ITU G.lite (G.992.2) specification
- DMT modulation and demodulation
- Full-rate adaptive modem
  - Maximum downstream rate of 8 Mbps
  - Maximum upstream rate of 1 Mbps
- Supports splitterless ADSL implementation
- WAN mode support: PPP over AAL5/ATM over ADSL via Windows 98/2000
- LAN mode support: RFC 1483 via Windows 98/2000
- Compliant with PCI Local Bus Specification, Revision 2.2
- Compliant with PCI Bus Power Management Interface Specification, Version 1.0
- Tone detection for low power mode

D20431 AFE Features

- Receive signal path includes:
  - Integrated hybrid receiver circuit with programmable gain
  - High pass filtering and 27dB of Automatic Gain Control (AGC) to improve signal-to-echo ratio
  - 14-bit ADC
- Transmit signal path includes:
  - 30dB of AGC for transmit power control
  - Low pass filtering to suppress noise in the receive band
  - 14-bit DAC
- Independent digital serial data and control interfaces
- Low power tone detection mode.

ADSL (Asymmetric Digital Subscriber Line) is a transmission technology used to carry user data over a single twisted pair line from the Central Office to the customer premises. The downstream (Central Office to Customer Premises) direction typically supports a much higher data rate than the upstream or return (Customer Premises to Central Office) channel. This asymmetric nature lends itself to applications like remote LAN access, Internet access, and video delivery. The downstream data rates can go up to 8 Mbps. The upstream data rates can go up to 1 Mbps. Actual data rates depend on the transceiver implementation, loop length, impairments, and transmitted power.

The Conexant ADSL Modem Device Set for PCI Applications is based upon a scalable architecture. This architecture will enable the device set to support an emerging set of ADSL specifications called G.lite. G.lite is expected to make it possible for telcos to deploy consumer-oriented, “always on” 1.5 Mbps Internet access services without the need for splitter equipment or wiring changes at the customer premises.

D20441 Line Driver Features

- Differential input and output line driver
- Thermal shutdown capability
- Line impedance matching during power-down
- Fixed differential gain

11627 ADSL DMT Data Pump Features

- Low power (0.5W) consumption
- DSP-based programmable ADSL data pump
- No external Interleave RAM, 16 Kbytes built-in
- Single 3.3V ± 5% power supply
- Echo cancellation
- Digital interface and rate buffering
- ADSL framing
- Forward Error Correction (FEC) encoding and decoding and interleaving
- Constellation encoding/decoding
- IFFT modulation and FFT demodulation
- Transmit and receive signal digital filtering
- Time domain equalization
- Frequency domain equalization
- Clock recovery
- CRC and scrambling
- Digital interface framing
- ATM mode
- Bit-synchronous mode

Ordering Information

Product	Package	Device Number
AccessRunner P46 PCI Bus Interface	176-pin TQFP	P46
AccessRunner 11627 ADSL Discrete Multitone (DMT) Data Pump	176-pin TQFP	11627
AccessRunner 20431 Analog Front End	32-pin TQFP	20431
AccessRunner 20441 Line Driver	16-pin SSOP	20441-12
	32-pin TQFP	20441-11

Revision History

Revision	Date	Comments
A	07/09/99	Initial release
B	10/19/99	Defined dash numbers and updated figures for 20441 line driver, changed document number from DSL-015, A

Detailed Description

P46 PCI Bus Interface

The P46 PCI bus interface is the bridge device between the 11627 ADSL DMT data pump and the host computer. It provides the control, interface, and data manipulation for the 11627 data pump, the 20431 AFE, the 20441 line driver, and hybrid circuitry. It is compliant with the PCI Local Bus Specification, Revision 2.2 and PCI Bus Power Management Interface Specification, Version 1.0.

20431 Analog Front End

The 20431 AFE is designed for use in full-rate and G.lite (G.992.2) ADSL modems. The ADSL AFE interfaces with the transmit line driver (20441) and the hybrid receive circuitry on the analog side, and with the ADSL DMT data pump (11627) on the digital side. The receive section filters out the unwanted echo and boosts the wanted signal before performing an A/D conversion. The transmit section converts digital data to analog signals and performs a smoothing operation before presenting the signals to the line driver.

The 20431 is designed to operate from a 3.3V supply (nominal), assuming that it is regulated within ± 5%. The maximum allowable supply voltage is 3.6V.

11627 ADSL DMT Data Pump

The 11627 DMT data pump is a T1.413 Issue 2 and G.992.1 compliant custom digital signal processing (DSP) chip built specifically for DMT ADSL transmission for use in ADSL modems. Brief descriptions of each functional block within the data pump are provided in the following sections; refer to Figure 2.

ATM Transmission Convergence (TC)

In the transmit direction, this block is in charge of embedding ATM cells into the serial data streams being fed into the digital interface.

In the receive direction, this block extracts the ATM cell boundaries from the serial data streams coming from the digital interface.

To reduce traffic on the PCI bus, the TC block performs idle cell insertion in the transmit direction and idle cell deletion and header error correction in the receive direction.

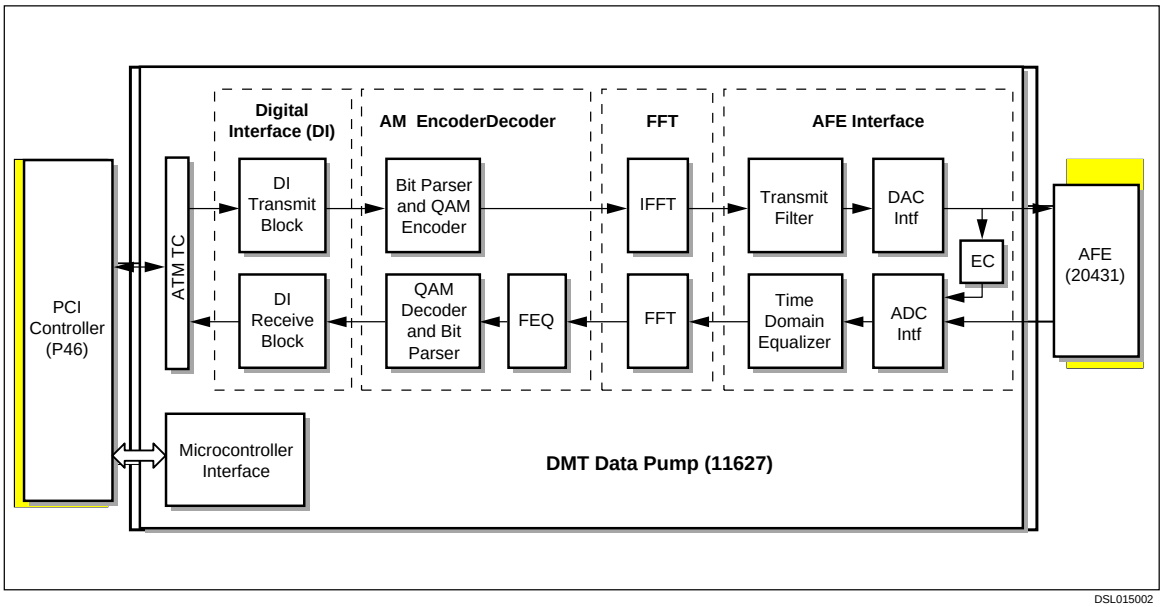


Figure 2. AccessRunner 11627 DMT Data Pump Functional Block Diagram

Digital Interface (DI)

The DI Transmit Block performs the following functions: transmit data multiplexing and buffering, fast and interleave data stream framing, transmit data synchronization control, eoc/aoc insertion, CRC encoding, scrambling, FEC encoding, and data interleaving.

The DI Receive Block performs the following functions: data de-interleaving, FEC decoding, descrambling, CRC check, receive data synchronization and receive clock generation, demultiplexing and buffering of receive data and receive eoc/aoc.

QAM Encoder/Decoder

The QAM Encoder/Decoder performs the following functions: constellation encoding, clock recovery, receive gain compensation, frequency domain equalization (FEQ), slicing, and constellation decoding. The block also performs other functions like frequency domain signal processing, signal power, error power averaging and computations related to frequency domain training.

FFT

The FFT performs IFFT for modulation of the transmit symbol, and FFT for demodulation of the receive symbol.

Analog Front End (AFE) Interface

The AFE Interface performs the following functions: transmit signal filtering, time domain equalization, and time domain signal power averaging, and echo cancellation (EC).

Microcontroller Interface

The microcontroller interface enables the host computer via the PCI controller to set parameters to control DSP sequencing and to read/write coefficients or data.

20441 Line Driver

The 20441 line driver is designed for use in full-rate and G.lite (G.992.2) ADSL modems. It is optimized for ideal ADSL performance providing low noise, high bandwidth, and superior linearity. The 20441 line driver transmits a DMT modulated signal in the 25 – 132 kHz band. It operates from a single 5V ±TBD% supply, refer to Figure 3.

The driver is optimized for ADSL performance: it has a very low noise figure, high bandwidth and good linearity.

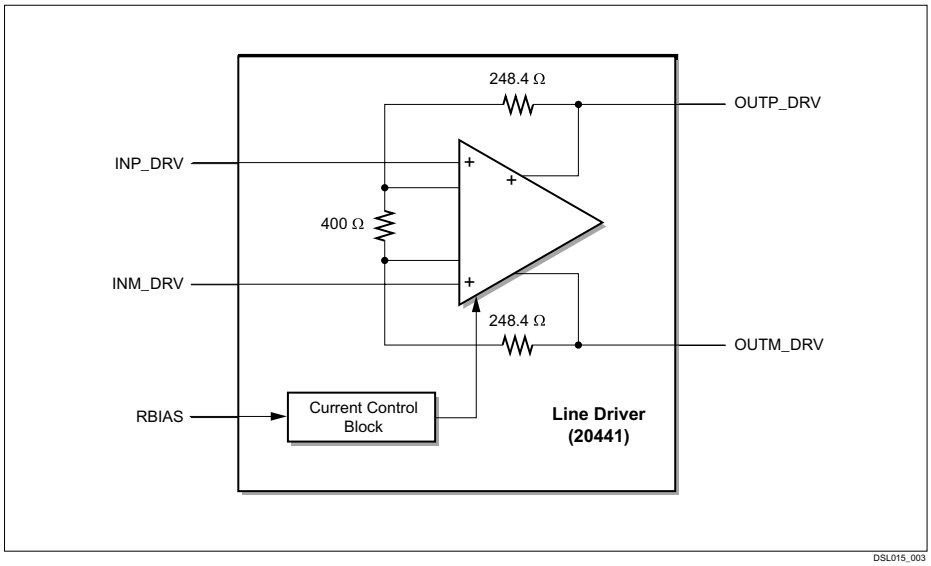


Figure 3. AccessRunner 20441 Line Driver

P46 PCI Bus Interface Device Hardware Pins and Signals

The pin assignments for the P46 are shown in Figure 4 and listed in Table 1. The signals are defined in Table 2.

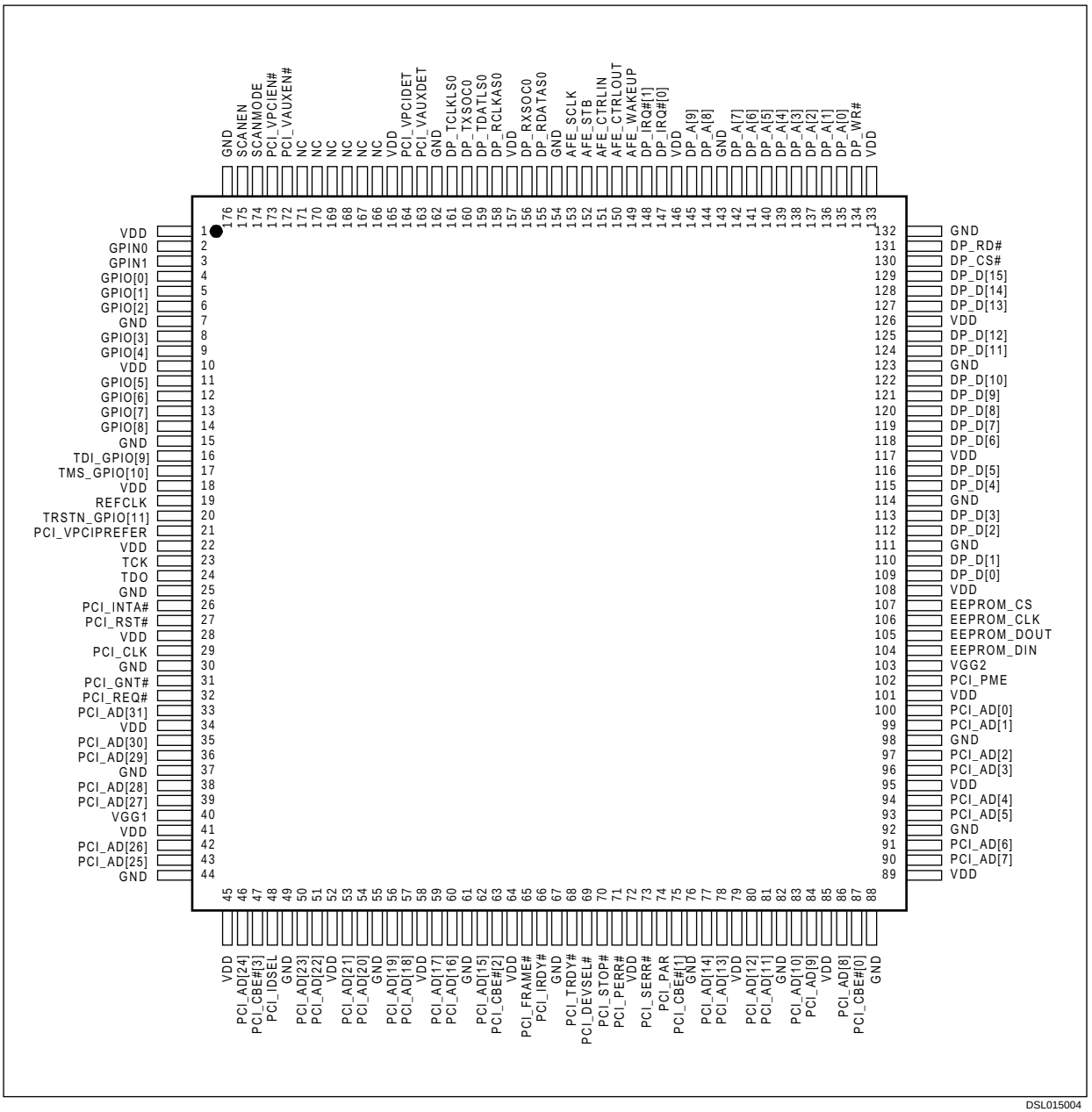


Figure 4. P46 Pinout Diagram

Table 1. P46 Pin Designations by Number

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD	45	VDD	89	VDD	133	VDD
2	GPIN0	46	PCI_AD[24]	90	PCI_AD[7]	134	DP_WR#
3	GPIN1	47	PCI_CBE#[3]	91	PCI_AD[6]	135	DP_A[0]
4	GPIO[0]	48	PCI_IDSEL	92	GND	136	DP_A[1]
5	GPIO[1]	49	GND	93	PCI_AD[5]	137	DP_A[2]
6	GPIO[2]	50	PCI_AD[23]	94	PCI_AD[4]	138	DP_A[3]
7	GND	51	PCI_AD[22]	95	VDD	139	DP_A[4]
8	GPIO[3]	52	VDD	96	PCI_AD[3]	140	DP_A[5]
9	GPIO[4]	53	PCI_AD[21]	97	PCI_AD[2]	141	DP_A[6]
10	VDD	54	PCI_AD[20]	98	GND	142	DP_A[7]
11	GPIO[5]	55	GND	99	PCI_AD[1]	143	GND
12	GPIO[6]	56	PCI_AD[19]	100	PCI_AD[0]	144	DP_A[8]
13	GPIO[7]	57	PCI_AD[18]	101	VDD	145	DP_A[9]
14	GPIO[8]	58	VDD	102	PCI_PME	146	VDD
15	GND	59	PCI_AD[17]	103	VGG2	147	DP_IRQ#[0]
16	TDI_GPIO[9]	60	PCI_AD[16]	104	EEPROM_DIN	148	DP_IRQ#[1]
17	TMS_GPIO[10]	61	GND	105	EEPROM_DOUT	149	AFE_WAKEUP
18	VDD	62	PCI_AD[15]	106	EEPROM_CLK	150	AFE_CTRLOUT
19	REFCLK	63	PCI_CBE#[2]	107	EEPROM_CS	151	AFE_CTRLIN
20	TRSTN_GPIO[11]	64	VDD	108	VDD	152	AFE_STB
21	PCI_VPCIPREFER	65	PCI_FRAME#	109	DP_D[0]	153	AFE_SCLK
22	VDD	66	PCI_IRDY#	110	DP_D[1]	154	GND
23	TCK	67	GND	111	GND	155	DP_RDATAS0
24	TDO	68	PCI_TRDY#	112	DP_D[2]	156	DP_RXSOC0
25	GND	69	PCI_DEVSEL#	113	DP_D[3]	157	VDD
26	PCI_INTA#	70	PCI_STOP#	114	GND	158	DP_RCLKAS0
27	PCI_RST#	71	PCI_PERR#	115	DP_D[4]	159	DP_TDATLS0
28	VDD	72	VDD	116	DP_D[5]	160	DP_TXSOC0
29	PCI_CLK	73	PCI_SERR#	117	VDD	161	DP_TCLKLS0
30	GND	74	PCI_PAR	118	DP_D[6]	162	GND
31	PCI_GNT#	75	PCI_CBE#[1]	119	DP_D[7]	163	PCI_VAUXDET
32	PCI_REQ#	76	GND	120	DP_D[8]	164	PCI_VPCIDET
33	PCI_AD[31]	77	PCI_AD[14]	121	DP_D[9]	165	VDD
34	VDD	78	PCI_AD[13]	122	DP_D[10]	166	NC
35	PCI_AD[30]	79	VDD	123	GND	167	NC
36	PCI_AD[29]	80	PCI_AD[12]	124	DP_D[11]	168	NC
37	GND	81	PCI_AD[11]	125	DP_D[12]	169	NC
38	PCI_AD[28]	82	GND	126	VDD	170	NC
39	PCI_AD[27]	83	PCI_AD[10]	127	DP_D[13]	171	NC
40	VGG1	84	PCI_AD[9]	128	DP_D[14]	172	PCI_VAUXEN#
41	VDD	85	VDD	129	DP_D[15]	173	PCI_VPCIEN#
42	PCI_AD[26]	86	PCI_AD[8]	130	DP_CS#	174	SCANMODE
43	PCI_AD[25]	87	PCI_CBE#[0]	131	DP_RD#	175	SCANEN
44	GND	88	GND	132	GND	176	GND

Table 2. P46 Pin Signals by Group

Pin Name	I/O[1]	Description
PCI INTERFACE		
PCI_AD[31:0]	I/O	Address/Data
PCI_CBE#[3:0]	I/O	Command/Byte Enables
PCI_FRAME#	I/O	Frame
PCI_IRDY#	I/O	Initiator Ready
PCI_TRDY#	I/O	Target Ready
PCI_PAR	I/O	Parity (Even)
PCI_STOP#	I/O	Target Stop
PCI_DEVSEL#	I/O	Target Response Device Select
PCI_IDSEL	I	Unique Select for Configuration
PCI_PERR#	I/O	Parity Error
PCI_SERR#	O	System Error
PCI_REQ#	O	Master Request
PCI_GNT#	I	Grant
PCI_CLK	I	PCI clock
PCI_RST#	I (S)	Reset
PCI_INTA#	O	Interrupt A
PCI_PME	O	PCI Power Management Event Signal
ADSL DMT DATA PUMP (11627) SERIAL CHANNEL INTERFACE		
DP_RDATAS0	I	Receive AS0/ATM0 Serial Data
DP_RXSOC0	I	Receive ATM0 Start of Cell
DP_RCLKAS0	I	Receive AS0/ATM0 Data Clock
DP_TDATLS0	O	Transmit LS0/ATM0 Serial Data
DP_TXSOC0	O	Transmit ATM0 Start of Cell
DP_TCLKLS0	I	Transmit LS0/ATM0 Data Clock
ADSL DMT DATA PUMP (11627) MICRO INTERFACE		
DP_WR#	O	Data Pump Device Write Enable
DP_RD#	O	Data Pump Device Read Enable
DP_D[15:0]	I/O (PU)	Data Pump Data Lines
DP_A[9:0]	O	Data Pump Address Lines
DP_CS#	O	Data Pump Chip Select
DP_IRQ#[1:0]	I (PU,S)	Data Pump Interrupt Request Lines
ANALOG FRONT END INTERFACE		
AFE_SCLK	I	Serial AFE Clock
AFE_STB	O	AFE Strobe
AFE_CTRLIN	O	Serial Data Sent to AFE
AFE_CTRLOUT	I	Serial Data Received from AFE

[1] PD Resistive pull-down
PU Resistive pull-up
S Schmitt

Pin Name	I/O[1]	Description
AFE_WAKEUP	I (S)	DSL Power Management Wakeup Signal from AFE
SERIAL EEPROM		
EEPROM_CS	O	EEPROM Chip Select
EEPROM_CLK	O	EEPROM Clock
EEPROM_DIN	I	EEPROM Data Input
EEPROM_DOUT	O	EEPROM Data Output
PCI POWER MANAGEMENT		
PCI_VAUXDET	I (PD,S)	Vaux Detect
PCI_VPCIDET	I (PD,S)	Vpci Detect
PCI_VAUXEN#	O	Vaux Enable
PCI_VPCIEN#	O	Vpci Enable
PCI_VPCIPREFER	I	This pin is used to determine whether Vpci or Vaux is the preferred power supply. 1=Vpci preferred, 0=Vaux preferred
MISCELLANEOUS		
GPIO[1:0]	I/O (PU,S)	General Purpose Schmitt Input/Output
GPIO[2:5], GPIO[8]	I/O (PU)	General Purpose Input/Output
GPIO[6]	I/O	General Purpose Input/Output (also used for active low reset)
GPIO[7]	I/O	General Purpose Input/Output (also used for active high reset)
TDI_GPIO[9]	I/O (PU)	JTAG test data input OR general purpose input/output. Function of this pin is dependant upon value of JTAGEN bit. When operating in JTAG mode this signal contains serial data that is shifted in on the rising edge of TCK.
TMS_GPIO[10]	I/O (PU)	JTAG test mode select OR general purpose input/output. Function of this pin is dependant upon value of JTAGEN bit. When operating in JTAG mode this siganl controls the operation of the TAP controller.
TRSTN_GPIO[11]	I/O (PU)	JTAG reset OR general purpose input/output. Function of this pin is dependant upon value of JTAGEN bit. When operating in JTAG mode, a high to low transition on this signal forces the TAP controller into a logic reset state.
TCK	I	JTAG clock.
TDO	O	JTAG data output. This pin generates serial data that is shifted out on the falling edge of TCK..
GPIN0	I (S)	General purpose schmitt input (modem ring detect)
GPIN1	I (PU,S)	General purpose schmitt input (modem offhook)
SCANEN	I (PD)	Scan chain enable. Used to shift data in and out of the scan chain.
SCANMODE	I (PD)	Scan mode enable pin. When tied high it will put the device into scan test mode.
REFCLK	I	35.328 MHz reference clock used to create the internal 53 MHz system clock
POWER AND GROUND		
VDD		3.3V Power
GND		Ground
VGG1		I/O Clamp Power Supply for PCI Signalling Environment (connect to VIO pin of PCI Bus)
VGG2		I/O Clamp Power Supply for Backend (connect to 3.3 volt supply)

11627 ADSL DMT Data Pump Hardware Pins and Signals

The pin assignments for the 11627 are shown in Figure 5 and listed in Table 3. The signals are defined in Table 4.

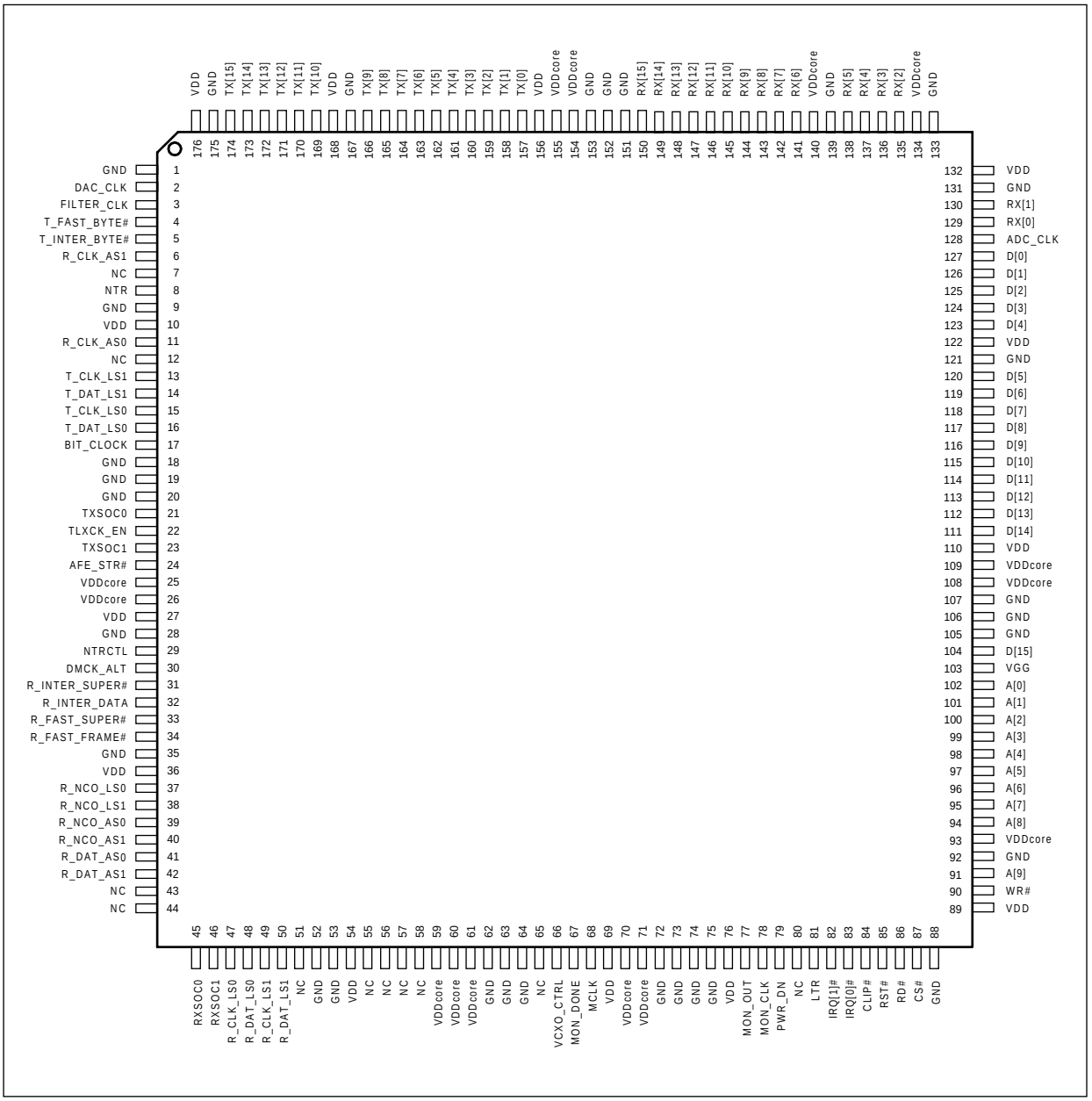


Figure 5. 11627 Pinout Diagram

Table 3. 11627 Pin Designations by Number

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	GND	37	R_NCO_LS0	73	GND	109	VDDcore	145	RX[10]
2	DAC_CLK	38	R_NCO_LS1	74	GND	110	VDD	146	RX[11]
3	FILTER_CLK	39	R_NCO_AS0	75	GND	111	D[14]	147	RX[12]
4	T_FAST_BYTE#	40	R_NCO_AS1	76	VDD	112	D[13]	148	RX[13]
5	T_INTER_BYTE#	41	R_DAT_AS0	77	MON_OUT	113	D[12]	149	RX[14]
6	R_CLK_AS1	42	R_DAT_AS1	78	MON_CLK	114	D[11]	150	RX[15]
7	NC	43	NC	79	PWR_DN	115	D[10]	151	GND
8	NTR	44	NC	80	NC	116	D[9]	152	GND
9	GND	45	RXSOC0	81	LTR	117	D[8]	153	GND
10	VDD	46	RXSOC1	82	IRQ[1]#	118	D[7]	154	VDDcore
11	R_CLK_AS0	47	R_CLK_LS0	83	IRQ[0]#	119	D[6]	155	VDDcore
12	NC	48	R_DAT_LS0	84	CLIP#	120	D[5]	156	VDD
13	T_CLK_LS1	49	R_CLK_LS1	85	RST#	121	GND	157	TX[0]
14	T_DAT_LS1	50	R_DAT_LS1	86	RD#	122	VDD	158	TX[1]
15	T_CLK_LS0	51	NC	87	CS#	123	D[4]	159	TX[2]
16	T_DAT_LS0	52	GND	88	GND	124	D[3]	160	TX[3]
17	BIT_CLOCK	53	GND	89	VDD	125	D[2]	161	TX[4]
18	GND	54	VDD	90	WR#	126	D[1]	162	TX[5]
19	GND	55	NC	91	A[9]	127	D[0]	163	TX[6]
20	GND	56	NC	92	GND	128	ADC_CLK	164	TX[7]
21	TXSOC0	57	NC	93	VDDcore	129	RX[0]	165	TX[8]
22	TLXCK_EN	58	NC	94	A[8]	130	RX[1]	166	TX[9]
23	TXSOC1	59	VDDcore	95	A[7]	131	GND	167	GND
24	AFE_STR#	60	VDDcore	96	A[6]	132	VDD	168	VDD
25	VDDcore	61	VDDcore	97	A[5]	133	GND	169	TX[10]
26	VDDcore	62	GND	98	A[4]	134	VDDcore	170	TX[11]
27	VDD	63	GND	99	A[3]	135	RX[2]	171	TX[12]
28	GND	64	GND	100	A[2]	136	RX[3]	172	TX[13]
29	NTRCTL	65	NC	101	A[1]	137	RX[4]	173	TX[14]
30	DMCK_ALT	66	VCXO_CTRL	102	A[0]	138	RX[5]	174	TX[15]
31	R_INTER_SUPER#	67	MON_DONE	103	VGG	139	GND	175	GND
32	R_INTER_DATA	68	MCLK	104	D[15]	140	VDDcore	176	VDD
33	R_FAST_SUPER#	69	VDD	105	GND	141	RX[6]		
34	R_FAST_FRAME#	70	VDDcore	106	GND	142	RX[7]		
35	GND	71	VDDcore	107	GND	143	RX[8]		
36	VDD	72	GND	108	VDDcore	144	RX[9]		

Table 4. 11627 Pin Signals by Group

Pin Name	I/O	Description
AFE ANALOG-to-DIGITAL INTERFACE		
RX[15:0]	I	Receive Data Lines In the parallel mode of operation, data is clocked by the signal ADC_CLK using the full data bus. In the serial mode of operation, a strobe signal (AFE_STR#) from the AFE shall trigger the transfer of data over a programmable width serial bus.
ADC_CLK	O	Receive Clock for Parallel Mode
CLIP#	O	Clip Interrupt This signal is used for monitoring incoming data for saturation. Goes low for one clock (ADC_CLK) cycle whenever clipping is detected.
AFE DIGITAL-to-ANALOG INTERFACE		
TX[15:0]	O	Transmit Data Lines In the parallel mode of operation, data is clocked by the signal DAC_CLK using the full data bus. In the serial mode of operation, a strobe signal (AFE_STR#) from the AFE shall trigger the transfer of data over a programmable width serial bus.
DAC_CLK	O	Transmit Clock for Parallel Mode
FILTER_CLK	O	AFE Filter Clock This signal is used by the DAC interface block to strobe the external AFE filters.
AFE_STR#	I	AFE Strobe Signal
DIGITAL INTERFACE (DI)		
TLXCK_EN	I	LSX Transmit Data Clock Generation Enable
T_CLK_LS0	I/O	Transmit Data Clock (LS0)
T_CLK_LS1	I/O	Transmit Data Clock (LS1)
T_DAT_LS0	I	Transmit Data (LS0)
T_DAT_LS1	I	Transmit Data (LS1)
R_CLK_LS0	I	Receive Data Clock (LS0)
R_CLK_LS1	I	Receive Data Clock (LS1)
R_DAT_LS0	O	Receive Data (LS0)
R_DAT_LS1	O	Receive Data (LS1)
R_CLK_AS0	I	Receive Data Clock (AS0)
R_CLK_AS1	I	Receive Data Clock (AS1)
R_DAT_AS0	O	Receive Data (AS0)
R_DAT_AS1	O	Receive Data (AS1)
R_NCO_LS0	O	Receive LS0 NCO Output
R_NCO_LS1	O	Receive LS1 NCO Output
R_NCO_AS0	O	Receive AS0 NCO Output
R_NCO_AS1	O	Receive AS1 NCO Output
BIT_CLOCK	O	Serial Data Bit Clock Output Used to synchronize the serial input and output data bit streams, enables, and superframe qualifiers.
T_FAST_BYTE#	O	Transmit Fast Data Bit Input Enable
T_INTER_BYTE#	O	Transmit Interleaved Data Bit Input Enable
R_FAST_FRAME#	O	Receive Fast Data Bit Output Frame Qualifier
R_FAST_SUPER#	O	Receive Fast Data Bit Output Superframe Qualifier

Pin Name	I/O	Description
R_INTER_DATA	O	Receive Interleaved Data Bit Output Clocked at BIT_CLOCK rate.
R_INTER_SUPER#	O	Receive Interleaved Data Bit Output Superframe Qualifier
PCI CONTROLLER INTERFACE		
D[15:0]	I/O	PCI Controller Interface Data Bus 16-bit input/output bus to send/receive data to/from PCI controller.
A[9:0]	I	PCI Controller Interface Address Bus 10-bit input bus to receive address from PCI controller.
WR#	I	Data Write Enable
RD#	I	Data Read Enable
CS#	I	Chip Select
IRQ[1:0]#	O	Programmable Interrupts
MISCELLANEOUS		
RST#	I	Global Chip Reset When low, puts chip into reset condition.
MCLK	I	High-speed Master Clock Connect to 35.328 MHz VCXO, which is 16 times the maximum Nyquist rate.
VXCO_CTRL	O	Oversampled VCXO analog control voltage
MON_OUT	O	1-bit serial D/A output used for constellation monitoring
MON_CLK	O	Serial Monitor Clock Operates at 138 kHz.
MON_DONE	O	New Symbol Constellation Qualifier
DMCK_ALT	I	External 2x Clock
LTR	O	8 kHz Local Timing Reference
NTR	I/O	8 kHz Network Timing Reference
NTRCTL	I	Network Timing Reference I/O Control
TXSOC0	I	TC0 Block Transmit Start of Cell.
TXSOC1	I	TC1 Block Transmit Start of Cell.
RXSOC0	O	TC0 Block Receive Start of Cell
RXSOC1	O	TC1 Block Receive Start of Cell
PWR_DN	I	Power Down Control Pin
POWER AND GROUND		
VDD		3.3V Power (I/O)
VDDcore		2.5V Power (Core)
GND		Ground
VGG		I/O Clamp Power Supply (connect to 5 volt supply for 5 volt tolerance)

20431 ADSL Analog Front End Hardware Pins and Signals

The pin assignments for the 20431 are shown in Figure 6 and defined in Table 5.

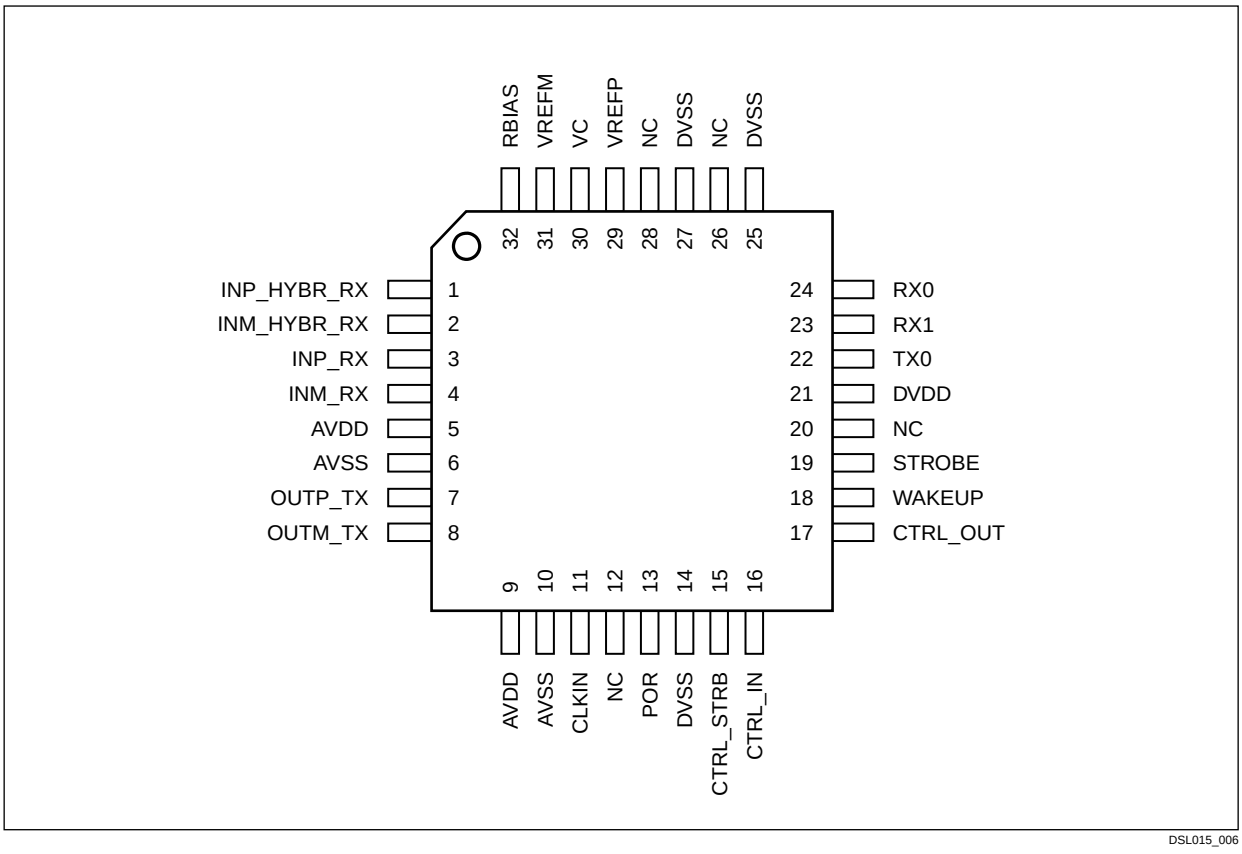


Figure 6. 20431 Pinout Diagram

Table 5. 20431 Pin Signals by Group

Pin Name	I/O	Description	Pin Number(s)
ADSL Digital Serial Data and Control Interface Signals			
CLKIN	I	Clock input (35.328MHz)	11
POR	I	Power On Reset	13
CTRL_STRB	I	Strobe for the control interface	15
CTRL_IN	I	Digital input of the control interface	16
CTRL_OUT	O	Digital output of the control interface	17
WAKEUP	O	Digital output for tone detection mode	18
STROBE	O	Strobe for the data interface	19
TX0	I	Digital transmit input	22
RX1	O	Digital receive output	23
RX0	O	Digital receive output	24
ADSL HYBRID CIRCUIT AND LINE DRIVER INTERFACE			
INP_HYBR_RX	I	Positive input of hybrid receiver circuit	1
INM_HYBR_RX	I	Negative input of hybrid receiver circuit	2
INP_RX	I	Positive input of receive path	3
INM_RX	I	Negative input of receive path	4
OUTP_TX	O	Positive output of transmit path	7
OUTM_TX	O	Negative output of transmit path	8
Overhead Signals			
VREFP	---	Analog reference voltage (2.5V)	29
VC	---	Analog reference voltage (1.5V)	30
VREFM	---	Analog reference voltage (0.5V)	31
RBIAS	---	Analog current reference	32
AVDD	---	Analog supply	5, 9
AVSS	---	Analog ground	6, 10
DVSS	---	Digital ground	14, 25, 27
DVDD	---	Digital supply	21

20441 ADSL Line Driver Hardware Pins and Signals

The pin assignments for the 20441 in both 16-pin TSSOP and 32-pin TQFP packages are shown in Figure 7 and defined in Table 6.

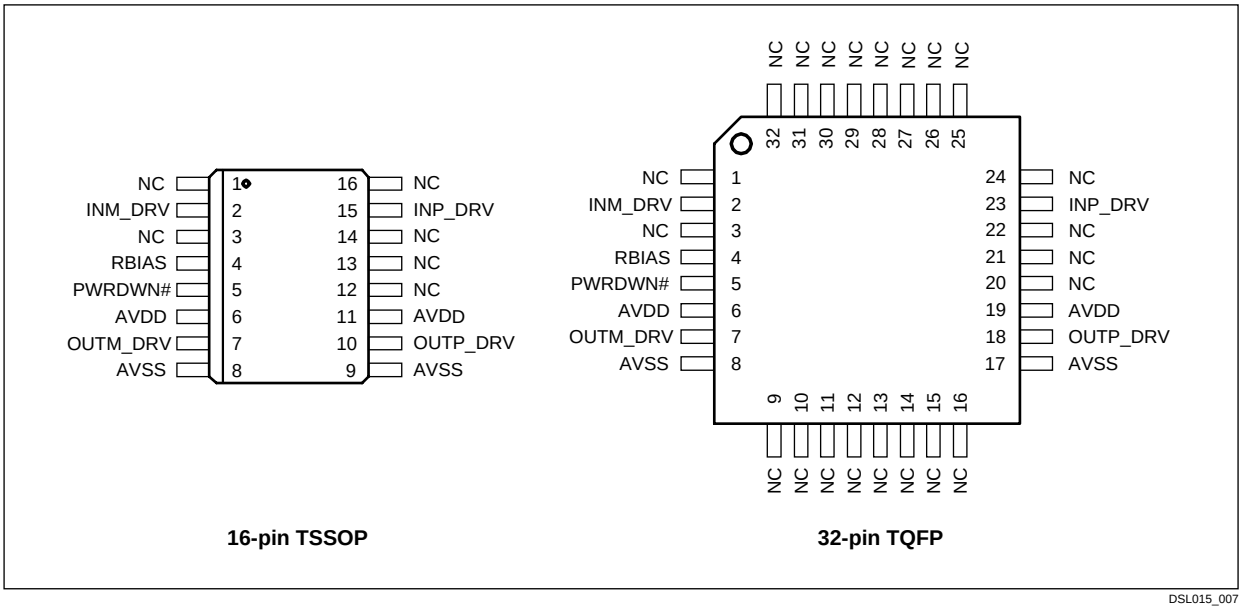


Figure 7. 20441 Pinout Diagrams

Table 6. 20441 Pin Signals by Group

Pin Name	I/O	Description	Comment	Pin Number(s)	
				16 SSOP	32 TQFP
INP_DRV	I	Positive transmit output of the AFE	Analog input	15	23
INM_DRV	I	Negative transmit output of the AFE	Analog input	2	2
OUTP_DRV	O	Positive output of the line driver	Analog output I_{max}=244mA (16 SSOP) I_{max}=280mA (32 SSOP)	10	18
OUTM_DRV	O	Negative output of the line driver	Analog output I_{max}=244mA (16 SSOP) I_{max}=280mA (32 TQFP)	7	7
PWRDWN#	I	Power down control (0 = power down)	Digital input (3V level)	5	5
RBIAS	I	Current setting external resistor	Tied to 125kΩ resistor (±1%)	4	4
POWER					
AVDD		Analog supply (+5V)	I_{max}=273.2mA (16 SSOP) I_{max}=309.2mA (32 TQFP)	6, 11	6, 19
AVSS		Analog ground	I_{max}=273.2mA (16 SSOP) I_{max}=309.2mA (32 TQFP)	8, 9	8, 17

Electrical and Environmental Specifications

AccessRunner P46 PCI Bus Interface Device

Table 7. DC Characteristics

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Power					
Power Supply	VDD	3.0	3.6	VDC	
PCI Signal/Power Levels – 3V signalling environment					
I/O Clamp Power Supply	VIO	VDD	3.6	VDC	
Input Low Voltage	VIL	-0.5	0.3 * Vdd	VDC	
Input High Voltage	VIH	0.5 * Vdd	Vdd + 0.5	VDC	
Output Low Voltage	VOL		0.1 * Vdd	VDC	Iout = -500 mA
Output High Voltage	VOH	0.9 * Vdd		VDC	Iout = 1500mA
PCI Signal/Power Levels – 5V signaling environment					
I/O Clamp Power Supply	VIO	VDD	5.25	VDC	
Input Low Voltage	VIL	-0.5	0.8	VDC	
Input High Voltage	VIH	2.0	Vdd + 0.5	VDC	
Output Low Voltage	VOL		0.55	VDC	Iout = 3mA, signals without pullups
Output Low Voltage	VOL		0.55	VDC	Iout = 6mA, signals with pullups
Output High Voltage	VOH	2.4		VDC	Iout = -2mA
TTL Signal Levels					
Input Low Voltage	VIL	-0.5	0.8	VDC	
Input High Voltage	VIH	2.0	Vdd + 0.5	VDC	
Output Low Voltage	VOL		0.4	VDC	
Output High Voltage	VOH	2.4		VDC	
Misc					
Pull-Up Resistance	Rpu	50	200	Kohm	
Pull-Down Resistance	Rpd	50	200	Kohm	

AccessRunner 11627 ADSL DMT Data Pump

Table 8. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply (I/O)	VDD	3.135	3.3	3.465	Volts
Power Supply (Core)	VDDcore	2.375	2.5	2.625	Volts
Ambient Operating Temperature	TA	-40		+85	°C
Humidity				90	%

Table 9. Absolute Maximum Ratings

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Power Supply	VDD			3.6	Volts
Voltage on any Signal Pin		GND-0.3		VDD+0.3	Volts
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature	TSOL			+260	°C
Vapor Phase Soldering	TVSOL			+220	°C
Air Flow		0			l.f.p.m

Table 10. DC Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Digital Inputs					
Input High Voltage	VIH	0.9*VDD		VDD	Volts
Input Low Voltage	VIL	GND		0.1*VDD	Volts
Input Leakage Current	IIL/IIH	-10		10	µA
Input Capacitance	CIN		2.9		pF
Digital Outputs					
Output High Voltage	VOH	0.9*VDD		VDD	Volts
Output Low Voltage	VOL	GND		0.1*VDD	Volts
Tri-State Output Leakage	ILK	10		10	µA
Output Capacitance	COUT		3.1		pF
Digital Bi-directionals					
Tri-State Output Leakage	ILK	-10		10	µA
Input/Output Capacitance	CINOUT		3.9		pF

AccessRunner 20431 AFE

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power supply	3.135	3.3	3.465	V
Operating junction temperature	-40		+100	°C
Operating ambient temperature	-40		+85	°C

Table 12. Absolute Maximum Ratings

Parameter	Min	Max	Units
Power supply	-0.35	3.6	V
Analog input voltage	-0.35	Vdd+0.35	V
Digital input voltage	-0.35	Vdd+0.35	V
Input current per Pin	-10	10	mA
Output current per Pin	-50	50	mA
Short circuit duration, to GND or Vdd		1	sec
Ambient temperature (power applied)	-55	+125	°C
Storage temperature	-65	+150	°C

Table 13. Power Consumption

Parameter	Min	Typ	Max	Units
Analog		40.5		mA
Digital		25		mA

Table 14. Digital Characteristics

Parameter	Min	Max	Units
High level input voltage	0.65*VDD	VDD+0.35	V
Low level input voltage	-0.35	0.25*VDD	V
High level output voltage	0.85*VDD	VDD	V
Low level output voltage	0	0.1*VDD	V
Input leakage current	-10	10	µA
Output leakage current	-10	10	µA

AccessRunner 20441 Line Driver

Table 15. Power Consumption

Parameter	Min	Typ	Max	Units
Line driver		18	24	mA

Table 16. Absolute Maximum Ratings

Parameter	Min	Max	Units
Power supply	-0.35	7	V
Analog input voltage	-0.35	Vdd+0.35	V
Digital input voltage	-0.35	Vdd+0.35	V
Input current per Pin	-10	10	mA
Output current per Pin	-50	50	mA
Short circuit duration, to GND or Vdd		1	Sec
Ambient temperature (power applied)	-55	+125	°C
Storage temperature	-65	+150	°C

Table 17. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power supply	4.75	5	5.25	V
Operating junction temperature	-40		+110	°C
Operating ambient temperature	0		+70	°C

Package Dimensions

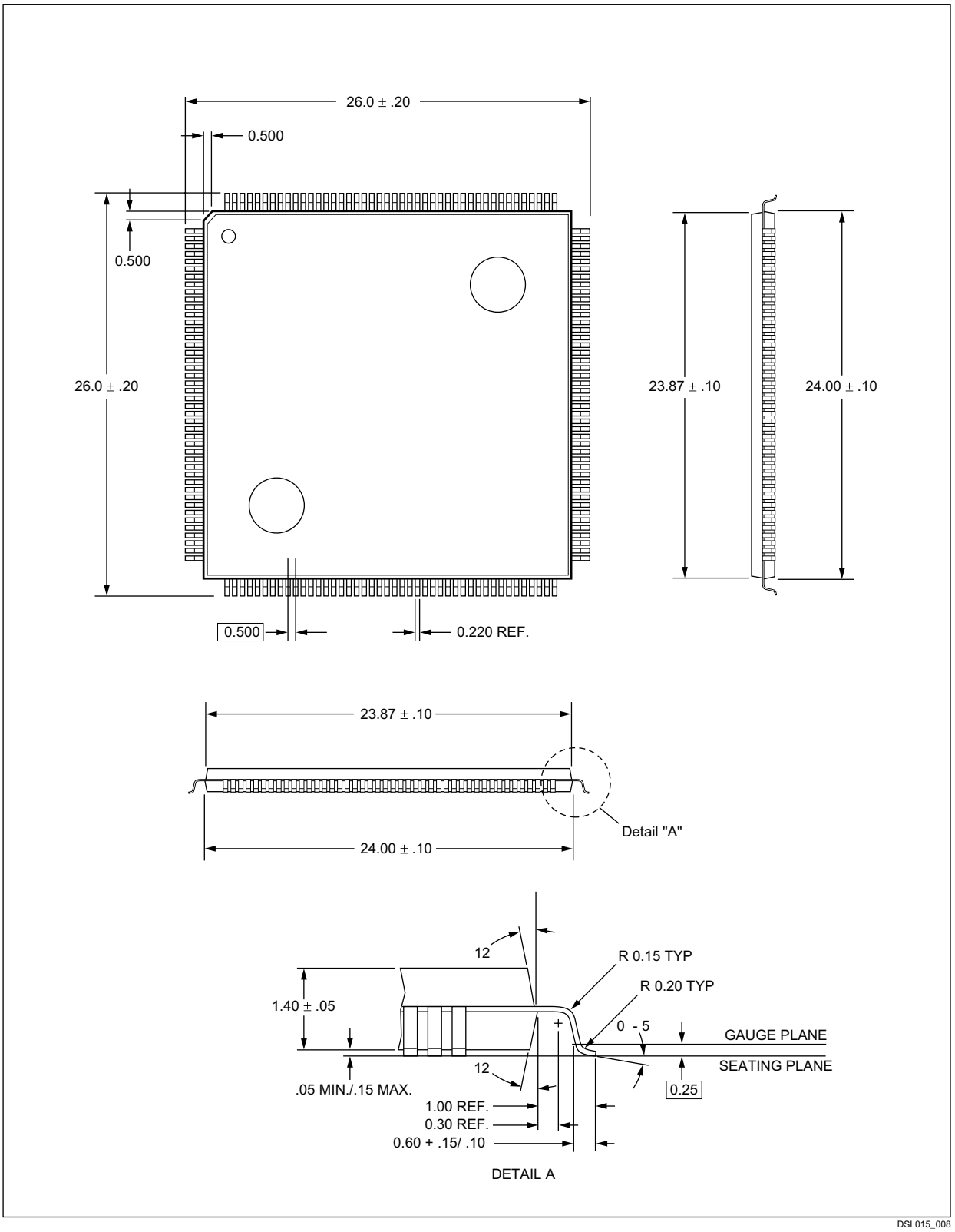
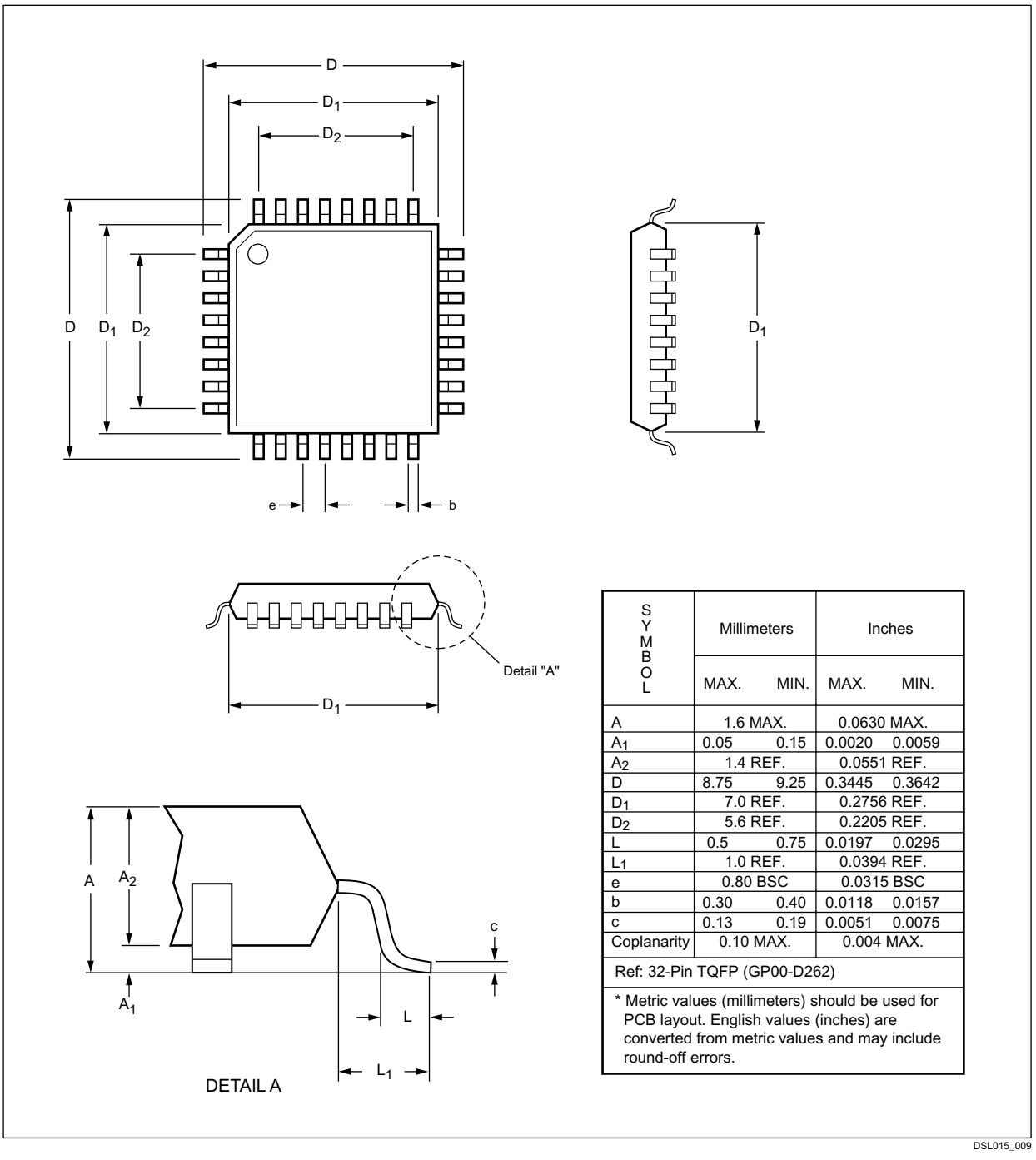


Figure 8. 176-pin TQFP Package Dimensions



SYMBOL	Millimeters		Inches	
	MAX.	MIN.	MAX.	MIN.
A	1.6 MAX.		0.0630 MAX.	
A_1	0.05	0.15	0.0020	0.0059
A_2	1.4 REF.		0.0551 REF.	
D	8.75	9.25	0.3445	0.3642
D_1	7.0 REF.		0.2756 REF.	
D_2	5.6 REF.		0.2205 REF.	
L	0.5	0.75	0.0197	0.0295
L_1	1.0 REF.		0.0394 REF.	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX.		0.004 MAX.	
Ref: 32-Pin TQFP (GP00-D262)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 9. 32-pin TQFP Package Dimensions

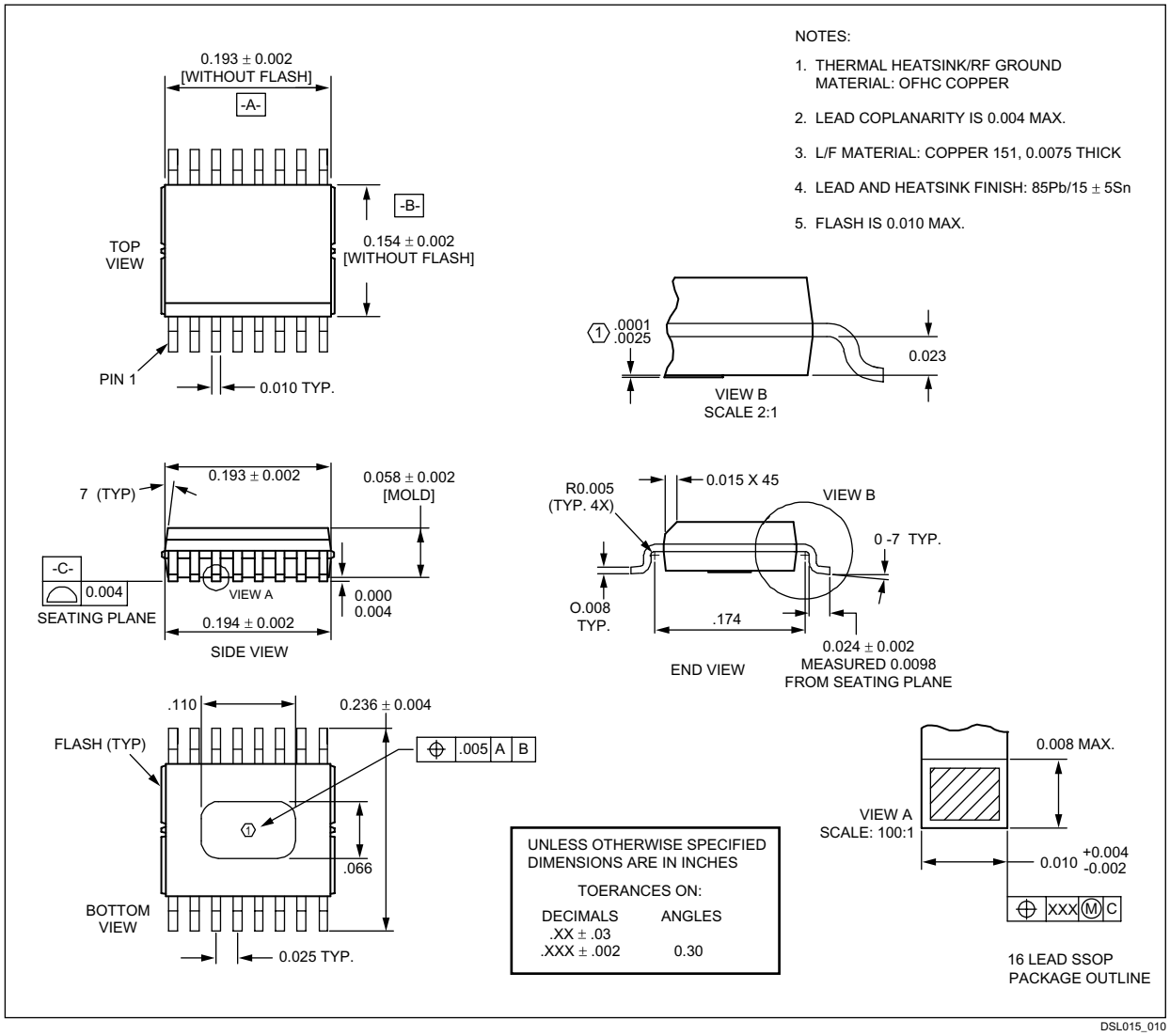


Figure 10. 16-pin SSOP Package Dimensions

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