



LC651204N/F/L, LC651202N/F/L

4-Bit Single-Chip Microcontrollers for Small-Scale Control Applications

Preliminary

Overview

The LC651204N/F/L and LC651202N/F/L are small-scale application microcontroller products in Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and as such they fully support the basic architecture and instruction set of that series. These microcontrollers are provided in a 30-pin package and include 2 kilobytes (KB) and 4 KB of on-chip ROM. These products are appropriate for use in a wide range of applications, from applications that use a small number of controls and circuits that were previously implemented in standard logic to larger scale applications including audio equipment such as decks and players, office equipment, communications equipment, automotive equipment, and home appliances. Except for the lack of an A/D converter, these microcontrollers provide the same functionality as the LC651104, 02N/F/L.

Features

- Fabricated in a CMOS process for low power (An instruction-controlled standby function is provided.)
- ROM/RAM
LC651204N/F/L - ROM: 4K × 8 bits, RAM: 256 × 4 bits
LC651202N/F/L - ROM: 2K × 8 bits, RAM: 256 × 4 bits
- Instruction set: The 80-instruction set provided by all members of the LC6500 series.
- Wide operating power-supply voltage range of 2.5 to 5.5 volts (L version)
- Instruction cycle time: 0.92 μs (F version)
- On-chip serial I/O circuit
- Highly flexible I/O ports
 - Number of ports: 6 ports with a total of 22 pins
 - All ports: Can be used for both input and output
 - I/O voltage: 15 V maximum (Only for C, D, E, and F ports with open-drain output specifications)
 - Output current: 20 mA maximum sink current (Capable of directly driving LEDs.)
- Options that allow specifications to be customized to match those of the application system.
 - Specification of open-drain output or built-in pull-up resistor: can be specified for all ports in bit units.

Specification of the output level at reset: Can be specified to be high or low for ports C and D in port units.

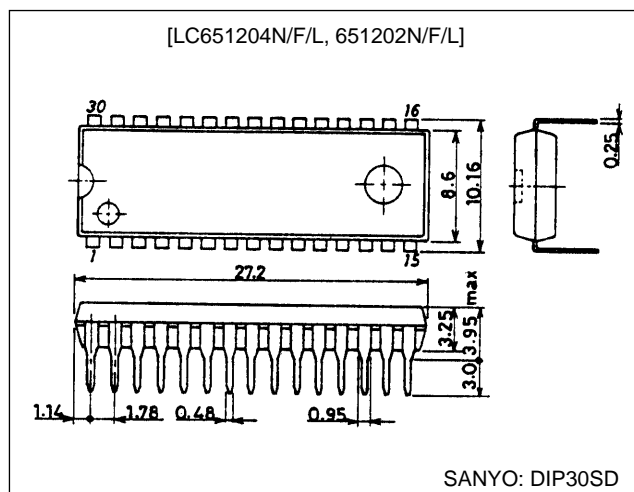
- Interrupt functions
 - Timer overflow vector interrupt (The interrupt state can be tested by the CPU.)
 - Vector interrupts initiated by the $\overline{\text{INT}}$ pin or full/empty states of the serial I/O circuit. (The interrupt state can be tested by the CPU.)
- Stack levels: 8 levels (shared with interrupts)
- Timers: 4-bit prescaler plus 8-bit programmable timers
- Clock oscillator options to match application system specifications.
 - Oscillator circuit options: 2-pin ceramic oscillator (N, F, and L versions)
 - Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
- Supports continuous output of a square wave signal (with a period 64 times the cycle time)
- Watchdog timer
 - RC time constant scheme
 - A watchdog timer function can be allocated to one of the external pins as an option.
- EP version: LC65E1104, OTP version: LC65P1104

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Package Dimensions

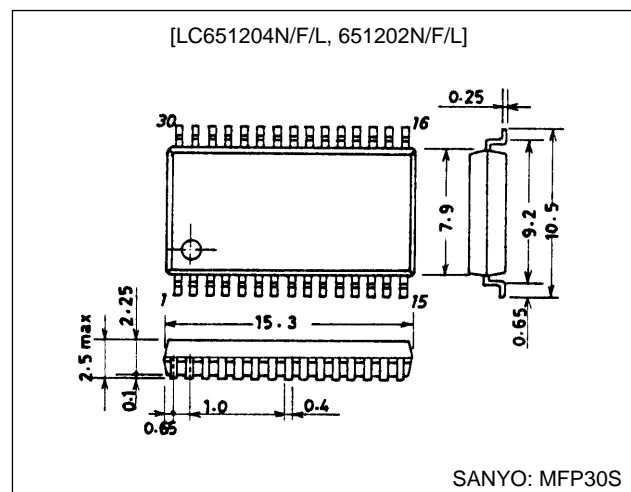
unit : mm

3196-DIP30SD



unit : mm

3073A-MFP30S



Note: The package drawings shown above are provided without error tolerances and are for reference purposes only. Contact Sanyo for official package drawings.

Function Overview

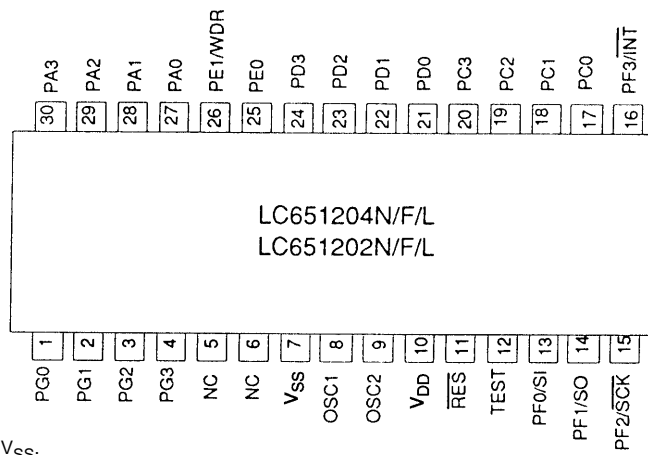
Item		LC651204N/1202N	LC651204F/1202F	LC651204L/1202L
Memory	ROM	4096 × 8 bits (1204N)	4096 × 8 bits (1204F)	4096 × 8 bits (1204L)
		2048 × 8 bits (1202N)	2048 × 8 bits (1202F)	2048 × 8 bits (1202L)
	RAM	256 × 4 bits (1204/1202N)	256 × 4 bits (1204/1202F)	256 × 4 bits (1204/1202L)
Instruction	Instruction set	80	80	80
	Table reference	Supported	Supported	Supported
Built-in functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal
	Timers	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
	Stack levels	8	8	8
	Standby function	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction
I/O ports	Number of ports	22 I/O pins	22 I/O pins	22 I/O pins
	Serial ports	4-bit or 8-bit I/O	4-bit or 8-bit I/O	4-bit or 8-bit I/O
	I/O voltage	15 V max.	15 V max.	15 V max.
	Output current	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.	10 mA typ. 20 mA max.
	I/O circuit types	Open drain (n-channel) or built-in pull-up resistor output selectable on a per-bit basis.		
	Output levels at reset	High or low can be selected in port units. (ports C and D only)		
	Square wave output	Supported	Supported	Supported
Characteristics	Minimum cycle time	2.77 μs (V _{DD} ≥ 3 V)	0.92 μs (V _{DD} ≥ 3 V)	3.84 μs (V _{DD} ≥ 2.5 V)
	Power-supply voltage	3 to 5.5 V	3 to 5.5 V	2.5 to 5.5 V
	Power-supply current	1.5 mA typ.	2 mA typ.	1.5 mA typ.
Oscillator	Oscillator	Ceramic (800 kHz, 1 MHz, 4 MHz)	Ceramic (4 MHz)	Ceramic (800 kHz, 1 MHz, 4 MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other functions	Package	DIP30S-D MFP30S	DIP30S-D MFP30S	DIP30S-D MFP30S

Note: Sanyo will announce details on oscillator elements and oscillator circuit constants as recommended application circuits are developed. Customers should check with Sanyo for the latest information as the development process progresses.

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Pin Assignment

Common assignments for the DIP and MFP packages



Note: NC pins must be connected to V_{SS} .

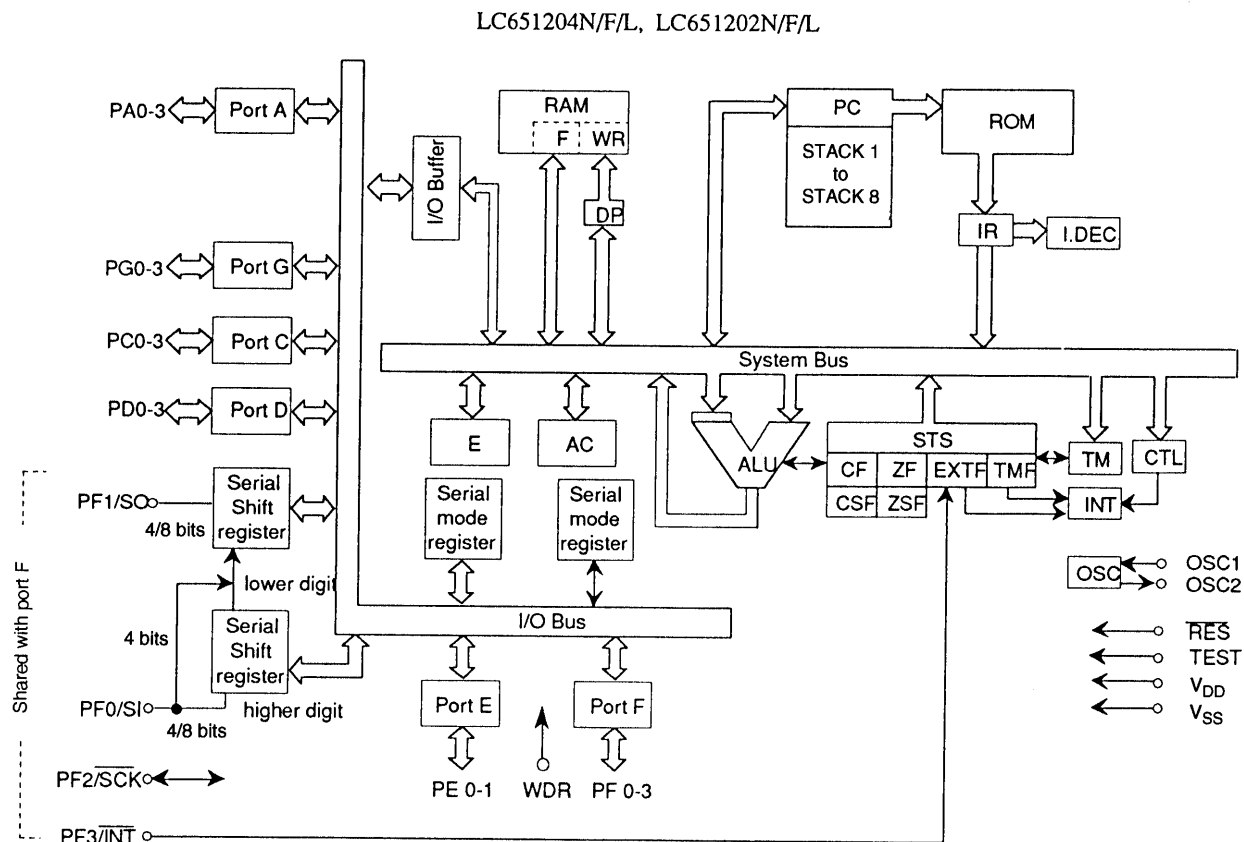
Top view

Pin Functions

Pin	Function
OSC1, OSC2	Connections for a ceramic oscillator element
\overline{RES}	Reset
PA0 to 3	I/O dual-function port A0 to A3
PC0 to 3	I/O dual-function port C0 to C3
PD0 to 3	I/O dual-function port D0 to D3
PE0 to 1	I/O dual-function port E0 to E1
PF0 to 3	I/O dual-function port F0 to F3
PG0 to 3	I/O dual-function port G0 to G3
TEST	Test
\overline{INT}	Interrupt request
SI	Serial input
SO	Serial output
\overline{SCK}	Serial clock input and output
NC	No connection
WDR	Watchdog reset

Note: The SI, SO, \overline{SCK} , and \overline{INT} pins are shared function pins that are also used as PF0 to PF3.

System Block Diagram



- | | |
|--------------------------------|--|
| RAM: Data memory | ROM: Program memory |
| F: Flag | PC: Program counter |
| WR: Working register | INT: Interrupt control |
| AC: Accumulator | IR: Instruction register |
| ALU: Arithmetic and logic unit | I.DEC: Instruction decoder |
| DP: Data pointer | CF, CSF: Carry flag, carry save flag |
| E: E register | ZF, ZSF: Zero flag, zero save flag |
| CTL: Control register | EXTIF: External interrupt request flag |
| OSC: Oscillator circuit | TMF: Internal interrupt request flag |
| TM: Timer | |
| STS: Status register | |

Development Support

Sanyo provides the following items to support application development using the LC651204 and LC651202.

1. User's manual

The "LC651104/1102 User's Manual" is used with these microcontrollers.

2. Development tool manual

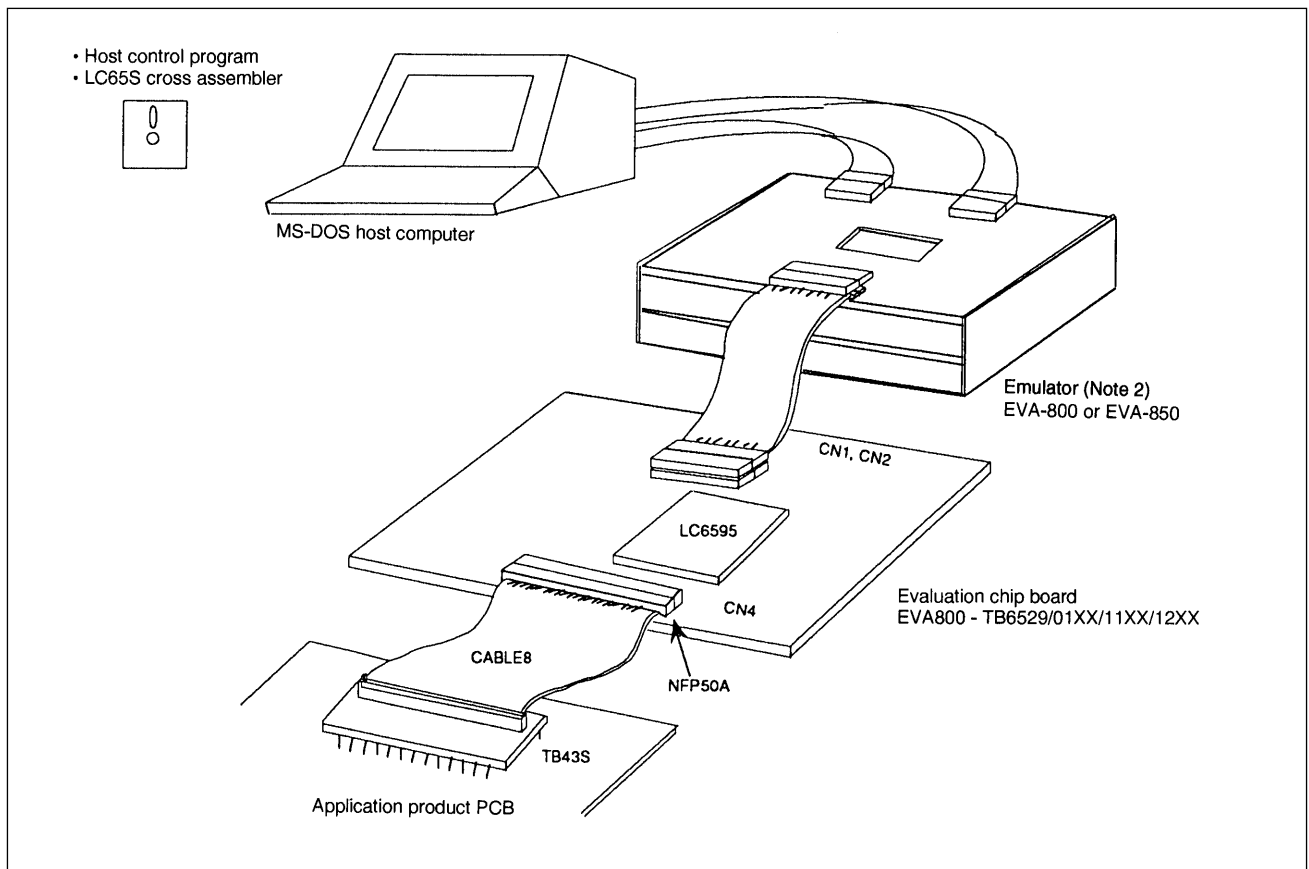
See the "EVA800 - LC651104/1102 Development Tool Manual" for details on use of the EVA-800 system.

3. Development tool

- Program development (using the EVA-800 system)
 - MS-DOS host computer system *1
 - Cross assembler ... MS-DOS-based cross assembler: LC65S.EXE
 - Evaluation chip: LC6595
 - Emulator: The EVA-800 main unit plus the evaluation chip
- Program development (using the EVA-86000 system): Use the EVA86K-ECB651100.
- Program evaluation
 - The <LC65E1104> on-chip EPROM microcontroller

Development Support System

EVA-800 System



Note: 1. MS-DOS is a registered trademark of Microsoft Corporation

2. Here, "EVA-800" is a generic term for several emulators. Suffixes (A, B, etc.) will be attached to the name as new versions are developed. Note that the EVA-800 emulator (i.e., the model with no suffix) is an old version and cannot be used.

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Pin Functions

Pin	Pin no.	I/O	Function	Options	State at reset	Handling when unused
V _{DD}	1	—	Power supply	—	—	—
V _{SS}	1	—				
OSC1	1	Input	<ul style="list-style-type: none"> System clock oscillator Connect an external ceramic oscillator element to these pins 	(1) External clock (2) Two-pin ceramic oscillator (3) Divider circuit option	—	—
OSC2	1	Output	<ul style="list-style-type: none"> Leave OSC2 open if an external clock is supplied. 	1. No divider circuit 2. Divide-by-three circuit 3. Divide-by-four circuit		
PA0 to PA3	4	I/O	<ul style="list-style-type: none"> I/O port A0 to A3 Input in 4-bit units using the IP instruction Output in 4-bit units using the OP instruction Port bits can be tested in bit units using the BP and BNP instructions. Port bits can be set or cleared in bit units using the SPB and RPB instructions. PA3 is used for standby control. Applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle. 	(1) Output open drain (2) Built-in pull-up resistor <ul style="list-style-type: none"> Options (1) and (2) can be specified in bit units. 	High-level output (i.e., the output n-channel transistor will be off.)	Open drain output select the options, connect to V _{SS} .
PC0 to PC3	4	I/O	<ul style="list-style-type: none"> I/O port C0 to C3 The PC0 to PC3 pin functions are identical to those of the PA0 to 3 pins.* High or low can be specified as the output at reset as an option. Note: These pins do not have a standby control function. 	(1) Output open drain (2) Built-in pull-up resistor (3) High-level output at reset (4) Low-level output at reset <ul style="list-style-type: none"> Options (1) and (2) can be specified in bit units. Option (3) and (4) are specified in 4-bit units. 	<ul style="list-style-type: none"> High-level output Low-level output (Depending on the option specified.)	The same as PA0 to PA3.
PD0 to PD3	4	I/O	<ul style="list-style-type: none"> I/O port D0 to D3 The PD0 to PD3 pin functions and options are identical to those of the PC0 to PC3 pins. 	The same as PC0 to PC3.	The same as PC0 to PC3.	The same as PA0 to PA3.

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Pin	Pin no.	I/O	Function	Options	State at reset	Handling when unused
PE0 to PE1 /WDR	2	I/O	<ul style="list-style-type: none"> I/O port E0 to E1 Input in 4-bit units using the IP instruction Output in 4-bit units using the OP instruction Port bits can be set or cleared in bit units using the SPB and RPB instructions. Port bits can be tested in bit units using the BP and BNP instructions. The PE0 pin also has a continuous pulse (64·T_{cyc}) output function. The PE1 pin can be set to function as the WDR watchdog timer reset pin as an option. 	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units. (3) Normal port PE1 (4) Watchdog timer reset WDR (5) (3) or (4) can be specified.	High-level output (i.e., the output n-channel transistor will be off.)	The same as PA0 to PA3.
PF0/SI PF1/SO PF2/SCK PF3/INT	4	I/O	<ul style="list-style-type: none"> I/O port F0 to F3 This port has the same functions and options as PE0 to PE1. * The pins PF0 to PF3 are also used as the serial interface and the INT pin. The function used can be selected under program control. SISerial input port SO.....Serial output port SCK ..Serial clock input or output INTInterrupt request input Serial I/O can be switched between 4-bit and 8-bit operation under program control. Note: This port does not provide a continuous pulse output function. 	The same as PA0 to PA3.	The same as PA0 to PA3. The serial port function is disabled. The interrupt source is INT.	The same as PA0 to PA3.
PG0 to PG3	4	I/O	<ul style="list-style-type: none"> I/O port G0 to G3 This port has the same functions and options as PE0 to PE1. * Note: This port does not provide a continuous pulse output function. 	The same as PA0 to PA3.	The same as PA0 to PA3.	The same as PA0 to PA3.
NC	2		<ul style="list-style-type: none"> NC pin. This pin must be connected to V_{SS} in the EP and OTP versions. 	—	—	Connect to V _{SS} .
RES	1	Input	<ul style="list-style-type: none"> System reset input Connect an external capacitor for the power up reset. A low level must be applied for at least four clock cycles for the reset startup sequence to operate correctly. 	—	—	—
TEST	1	Input	<ul style="list-style-type: none"> LSI test pin Must be connected to V_{SS}. 	—	—	Must be connected to V _{SS} .

Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The OSC2 pin must be left open.
Ceramic oscillator		

Divider Options

Option	Circuit	Conditions and notes
No divider (1/1)		<ul style="list-style-type: none"> • Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 1444 kHz (LC651204N and LC651202N) • The oscillator frequency or the external clock frequency must not exceed 4330 kHz (LC651204F and LC651202F) • The oscillator frequency or the external clock frequency must not exceed 1040 kHz (LC651204L and LC651202L)
Built-in divide-by-three circuit		<ul style="list-style-type: none"> • Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz
Built-in divide-by-four circuit		<ul style="list-style-type: none"> • Supports both oscillator options. • The oscillator frequency or the external clock frequency must not exceed 4330 kHz

Caution: The oscillator and divider options are summarized in the following tables. The information presented in those tables is crucial when using these products.

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**Divider Options for the LC651204N/1202N, LC651204F/1202F, and LC651204L/1202L
LC651204N, LC651202N**

Circuit type	Frequency	Divider option (cycle time)	V _{DD} range	Notes
Ceramic oscillator	800 kHz	1/1 (5 μs)	3 to 5.5 V	
	1 MHz	1/1 (4 μs)	3 to 5.5 V	
	4 MHz	1/3 (3 μs) 1/4 (4 μs)	3 to 5.5 V 3 to 5.5 V	This frequency cannot be used with the 1/1 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670 k to 1444 kHz	1/1 (6 to 2.77 μs)	3 to 5.5 V	
	2000 k to 4330 kHz	1/3 (6 to 2.77 μs)	3 to 5.5 V	
	2600 k to 4330 kHz	1/4 (6 to 3.70 μs)	3 to 5.5 V	
Use of an external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204F, LC651202F

Circuit type	Frequency	Divider option (cycle time)	V _{DD} range	Notes
Ceramic oscillator	4 MHz	1/1 (1 μs)	3 to 5.5 V	
External clock generated by a two-terminal RC oscillator circuit	670 k to 4330 kHz	1/1 (6 to 0.92 μs)	3 to 5.5 V	
Use of an external clock with the ceramic oscillator circuit	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

LC651204L LC651202L

Circuit type	Frequency	Divider option (cycle time)	V _{DD} range	Notes
Ceramic oscillator	800 kHz	1/1 (5 μs)	2.5 to 5.5 V	
	1 MHz	1/1 (4 μs)	2.5 to 5.5 V	
	4 MHz	1/4 (4 μs)	2.5 to 5.5 V	This frequency cannot be used with the 1/1, 1/3 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670 k to 1040 kHz	1/1 (6 to 3.84 μs)	2.5 to 5.5 V	
	2000 k to 3120 kHz	1/3 (6 to 3.84 μs)	2.5 to 5.5 V	
	2600 k to 4160 kHz	1/4 (6 to 3.84 μs)	2.5 to 5.5 V	
Use of an external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

Port C and D Output State at Reset Options

The output levels at reset of the I/O ports C and D can be selected from the following two options, which are specified in 4-bit units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

Port Output Circuit Type Option

The output circuit types of the I/O ports can be selected from the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		Ports A, C, D, E, F, and G
Pull-up resistor output		

Watchdog Timer Reset Option

Whether the PE1/WDR pin functions as the normal port PE1 or as the WDR watchdog timer reset pin can be selected as an option.

LC651204N/F/L, LC651202N/F/L

LC651204N, 651202N

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V _{DD} max		V _{DD}	-0.3 to +7.0	V
Output voltage	V _O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V _I (1)		OSC1 *1	-0.3 to V _{DD} +0.3	V
	V _I (2)		TEST, $\overline{\text{RES}}$	-0.3 to V _{DD} +0.3	V
I/O voltage	V _{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	V
	V _{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to V _{DD} +0.3	V
	V _{IO} (3)	PA0 to 3, PG0 to 3		-0.3 to V _{DD} +0.3	V
Peak output current	I _{OP}		I/O ports	-2 to +20	mA
Average output current	I _{OA}	Average value per pin over a 100-ms period	I/O ports	-2 to +20	mA
	ΣI_{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to PC3 PD0 to PD3 PE0 to PE1	-15 to +100	mA
	ΣI_{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to PF3 PG0 to PG3 PA0 to PA3	-15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = -40 to +85°C (MFP package)		150	mW
Operating temperature	T _{opr}			-40 to +85	°C
Storage temperature	T _{stg}			-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to 85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			Unit	
				min	typ	max		
Operating power-supply voltage	V _{DD}		V _{DD}	3.0		5.5	V	
Standby power-supply voltage	V _{ST}	RAM and register values retained *3	V _{DD}	1.8		5.5	V	
Input high-level voltage	V _{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V _{DD}		13.5	V	
	V _{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (4)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with OD specifications	0.8 V _{DD}		13.5	V	
	V _{IH} (5)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with PU specifications	0.8 V _{DD}		V _{DD}	V	
	V _{IH} (6)	V _{DD} = 1.8 to 5.5 V		$\overline{\text{RES}}$	0.8 V _{DD}		V _{DD}	V
	V _{IH} (7)	External clock specifications		OSC1	0.8 V _{DD}		V _{DD}	V

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings				
				min	typ	max	Unit	
Input low-level voltage	V _{IL} (1)	Output n-channel transistor off	V _{DD} = 4 to 5.5 V	Port	V _{SS}		0.2V _{DD}	V
	V _{IL} (2)	Output n-channel transistor off	V _{DD} = 3 to 5.5 V	Port	V _{SS}		0.2V _{DD}	V
	V _{IL} (3)	Output n-channel transistor off	V _{DD} = 4 to 5.5 V	$\overline{\text{INT}}$, SCK, SI	V _{SS}		0.2V _{DD}	V
	V _{IL} (4)	Output n-channel transistor off	V _{DD} = 3 to 5.5 V	$\overline{\text{INT}}$, SCK, SI	V _{SS}		0.2V _{DD}	V
	V _{IL} (5)	External clock specifications	V _{DD} = 4 to 5.5 V	OSC1	V _{SS}		0.2V _{DD}	V
	V _{IL} (6)	External clock specifications	V _{DD} = 3 to 5.5 V	OSC1	V _{SS}		0.2V _{DD}	V
	V _{IL} (7)		V _{DD} = 4 to 5.5 V	TEST	V _{SS}		0.2V _{DD}	V
	V _{IL} (8)		V _{DD} = 3 to 5.5 V	TEST	V _{SS}		0.2V _{DD}	V
	V _{IL} (9)		V _{DD} = 4 to 5.5 V	$\overline{\text{RES}}$	V _{SS}		0.2V _{DD}	V
	V _{IL} (10)		V _{DD} = 3 to 5.5 V	$\overline{\text{RES}}$	V _{SS}		0.2V _{DD}	V
Operating frequency (cycle time)	f _{op} (T _{cyc})	Frequencies up to 4.33 MHz are supported if the divide-by-three or divide-by-four divider circuit option is used.	V _{DD} = 3 to 5.5 V		670 (6)		1444 (2.77)	kHz (μs)
External clock conditions	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.444 MHz.	V _{DD} = 3 to 5.5 V	OSC1	670		4330	kHz
Frequency	textH, textL		V _{DD} = 3 to 5.5 V	OSC1	69			ns
Pulse width	textR, textF		V _{DD} = 3 to 5.5 V	OSC1			50	ns
Rise and fall times								
Guaranteed oscillator constants		Figure 2				See Table 1.		
Ceramic oscillator								

LC651204N/F/L, LC651202N/F/L

Electrical Characteristics at Ta = -40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Input high-level current	I _{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = 13.5 V	Ports C, D, E, and F with open-drain specifications			5.0	μA
	I _{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = V _{DD}	Ports A and G with open-drain specifications			1.0	μA
	I _{IH} (3)	External clock mode, V _{IN} = V _{DD}	OSC1			1.0	μA
Input low-level current	I _{IL} (1)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with open-drain specifications	-1.0			μA
	I _{IL} (2)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	I _{IL} (3)	V _{IN} = V _{SS}	$\overline{\text{RES}}$	-45	-10		μA
	I _{IL} (4)	External clock mode, V _{IN} = V _{SS}	OSC1	-1.0			μA
Output high-level voltage	V _{OH} (1)	I _{OH} = -50 μA V _{DD} = 4.0 to 5.5 V	Ports with pull-up resistor specifications	V _{DD} -1.2			V
	V _{OH} (2)	I _{OH} = -10 μA V _{DD} = 3.0 to 5.5 V	Ports with pull-up resistor specifications	V _{DD} -0.5			V
Output low-level voltage	V _{OL} (1)	I _{OL} = 10 mA, V _{DD} = 4.0 to 5.5 V	Port			1.5	V
	V _{OL} (2)	I _{OL} = 1 mA, with the I _{OL} for all ports no more than 1 mA. V _{DD} = 3.0 to 5.5 V	Port			0.5	V
Schmitt characteristics	Hysteresis voltage	V _{HIS}			0.1 V _{DD}		V
	High-level threshold voltage	V _{tH}	$\overline{\text{RES}}$, $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI OSC1 with Schmitt specifications *4	0.4 V _{DD}		0.8 V _{DD}	V
	Low-level threshold voltage	V _{tL}		0.2 V _{DD}		0.6 V _{DD}	V
Current drain	I _{DDOP} (1)	Operating, output n-channel transistors off, Ports = V _{DD} Figure 2, 4 MHz, divide-by-three circuit	V _{DD}		1.5	5	mA
Ceramic oscillator	I _{DDOP} (2)	Figure 2, 4 MHz, divide-by-four circuit	V _{DD}		1.5	4	mA
	I _{DDOP} (3)	Figure 2, 800 kHz	V _{DD}		1.5	4	mA
External clock	I _{DDOP} (4)	670 to 1444 kHz, no divider circuit 2000 to 4330 kHz, divide-by-three circuit 2600 to 4330 kHz, divide-by-four circuit	V _{DD}		1.5	5	mA
Standby mode	I _{DDst}	Output n-channel transistor off, V _{DD} = 5.5 V Ports = V _{DD} , V _{DD} = 3 V	V _{DD}		0.05	10	μA
			V _{DD}		0.025	5	μA

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LC651204N/F/L, LC651202N/F/L

Continued from preceding page.

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Oscillator characteristics							
Ceramic oscillator Oscillator frequency	f_{CFOSC} *5	Figure 2, fo = 800 kHz	OSC1, OSC2	768	800	832	kHz
		Figure 2, fo = 1 MHz	OSC1, OSC2	960	1000	1040	kHz
		Figure 2, fo = 4 MHz, divide-by-three or divide-by-four circuit	OSC1, OSC2	3840	4000	4160	kHz
Oscillator stabilization time	t_{CFS}	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz Divide-by-three or divide-by-four circuit			5	ms	
Pull-up resistors I/O ports	R_{PP}	Output n-channel transistor off $V_{in} = V_{SS}, V_{DD} = 5 V$	Ports with pull-up resistor specifications	8	14	30	k Ω
\overline{RES}	R_u	$V_{in} = V_{SS}, V_{DD} = 5 V$	\overline{RES}	100	250	400	k Ω
External reset characteristics							
Reset time	t_{RST}				See Figure 4.		
Pin capacitance	C_p	f = 1 MHz With all pins other than the pin being measured at $V_{IN} = V_{SS}$			10		pF
Serial clock Input clock cycle time	t_{CKCY} (1)	Figure 5	\overline{SCK}	3.0			μs
Output clock cycle time	t_{CKCY} (2)	Figure 5	\overline{SCK}		$64 \times T_{CYC}$ *6		μs
Input clock low-level pulse width	t_{CKL} (1)	Figure 5	\overline{SCK}	1.0			μs
Output clock low-level pulse width	t_{CKL} (2)	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs
Input clock high-level pulse width	t_{CKH} (1)	Figure 5	\overline{SCK}	1.0			μs
Output clock high-level pulse width	t_{CKH} (2)	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs

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LC651204N/F/L, LC651202N/F/L

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Parameter	Symbol	Conditions	V _{DD} (v)	Applicable pins/notes	Ratings			
					min	typ	max	Unit
Serial input								
Data setup time	t _{ICK}	Stipulated with respect to the rising edge of SCK.		SI	0.4			μs
Data hold time	t _{CKI}	Figure 5		SI	0.4			μs
Serial output								
Output delay time	t _{CKO}	Stipulated with respect to the falling edge of SCK. For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			0.6	μs
Pulse output	t _{PCY}	Figure 6		PE0		64 × T _{CYC}		μs
Period		T _{cyc} = 4 × the system clock period						
High-level pulse width	t _{PH}	For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0		32 × T _{CYC} ±10%		μs
Low-level pulse width	t _{PL}			PE0		32 × T _{CYC} ±10%		μs
Watchdog timer	Guaranteed constants *7	C _W	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.1±5%	μF
		R _W			WDR		680±1%	kΩ
		R _I			WDR		100±1%	Ω
	Clear time (discharge)	t _{WCT}	See Figure 7.		WDR	100		μs
	Clear period (charge)	t _{WCCY}	See Figure 7.		WDR	29		ms
	Guaranteed constants *7	C _W	When PE1 has open-drain output specifications	4 to 5.5	WDR		0.047±5%	μF
		R _W			WDR		680±1%	kΩ
		R _I			WDR		100±1%	Ω
	Clear time (discharge)	t _{WCT}	See Figure 7.		WDR	40		μs
	Clear period (charge)	t _{WCCY}	See Figure 7.		WDR	15		ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 3 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period
3. The operating power-supply voltage V_{DD} must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for f_{COSC} are the frequencies for which oscillation is possible. The center frequency when a ceramic oscillator is used may differ by about 1% from the nominal value listed by the manufacturer of the ceramic oscillator element. See the specifications of the ceramic oscillator element for details.
6. T_{cyc} = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

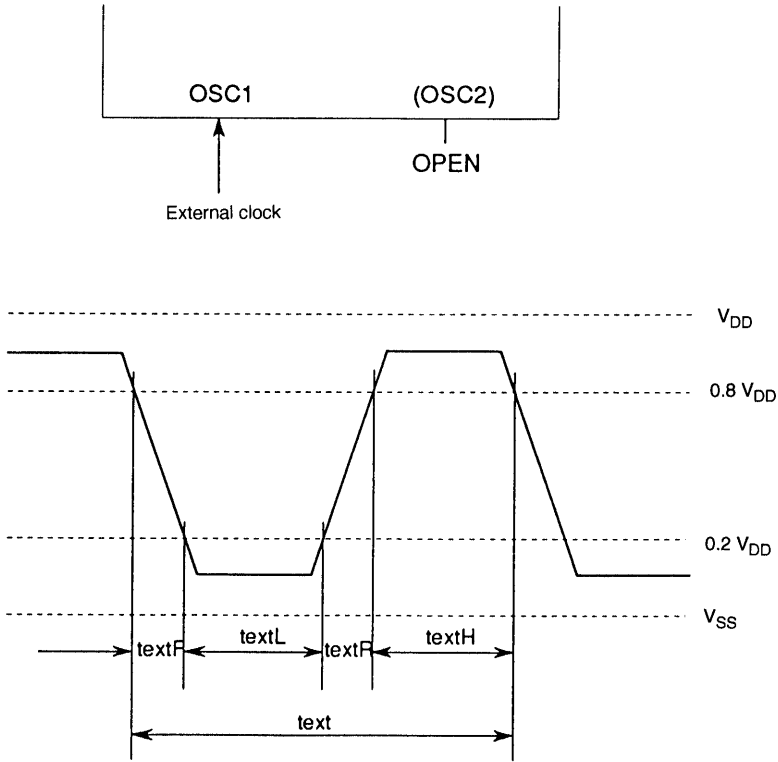


Figure 1 External Clock Input Waveform

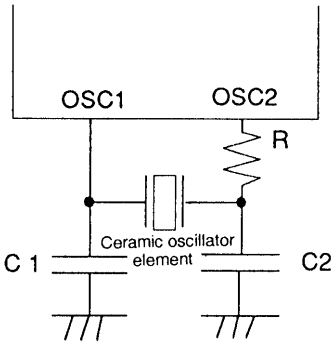


Figure 2 Ceramic Oscillator Circuit

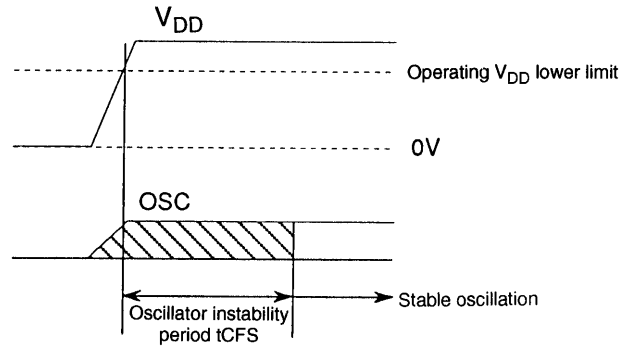


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG CST4.00MGW (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera Corporation) KBR4.0MSA KBR4.0MKS (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
1 MHz (Kyocera Corporation) KBR1000F	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	0 Ω
800 kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
800 kHz (Kyocera Corporation) KBR800F	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	0 Ω

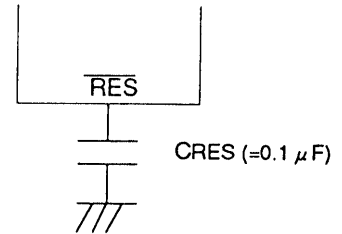


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

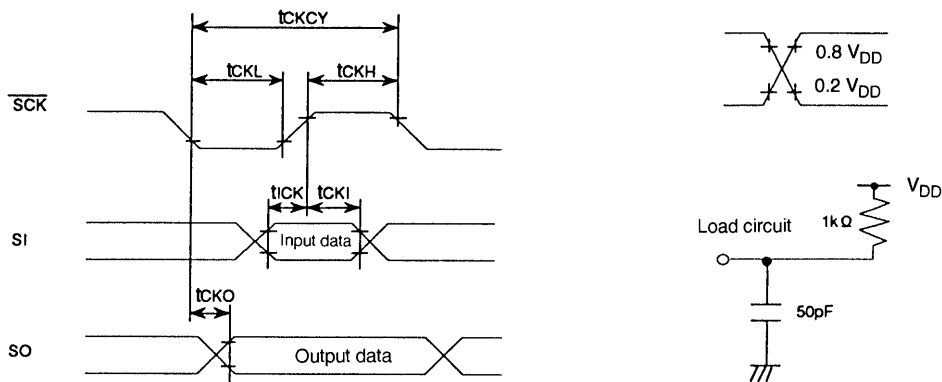
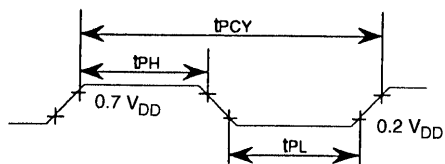
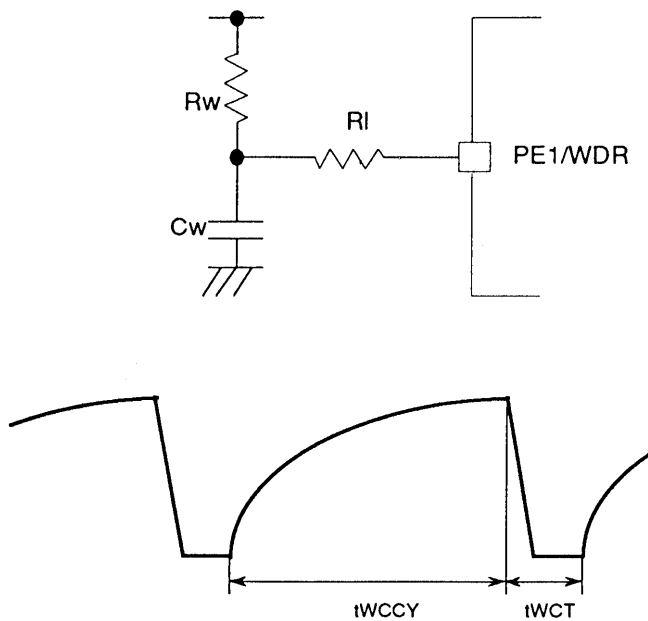


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



t_{WCCY}: Charge time due to the external components C_w, R_w, and R_l.
 t_{WCT}: Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204N/F/L, LC651202N/F/L

LC651204F, 651202F

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V _{DD} max		V _{DD}	-0.3 to +7.0	V
Output voltage	V _O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V _I (1)		OSC1 *1	-0.3 to V _{DD} +0.3	V
	V _I (2)		TEST, \overline{RES}	-0.3 to V _{DD} +0.3	V
I/O voltage	V _{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	V
	V _{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to V _{DD} +0.3	V
	V _{IO} (3)	PA0 to 3, PG0 to 3		-0.3 to V _{DD} +0.3	V
Peak output current	I _{OP}		I/O ports	-2 to +20	mA
Average output current	I _{OA}	Average value per pin over a 100-ms period	I/O ports	-2 to +20	mA
	Σ I _{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1 *2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	mA
	Σ I _{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = -40 to +85°C (MFP package)		150	mW
Operating temperature	T _{opr}			-40 to +85	°C
Storage temperature	T _{stg}			-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V, VDD = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			Unit	
				min	typ	max		
Operating power-supply voltage	V _{DD}		V _{DD}	3.0		5.5	V	
Standby power-supply voltage	V _{ST}	RAM and register values retained *3	V _{DD}	1.8		5.5	V	
Input high-level voltage	V _{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V _{DD}		13.5	V	
	V _{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (4)	Output n-channel transistors off	The \overline{INT} , \overline{SCK} , and SI pins with OD specifications	0.8 V _{DD}		13.5	V	
	V _{IH} (5)	Output n-channel transistors off	The \overline{INT} , \overline{SCK} , and SI pins with PU specifications	0.8 V _{DD}		V _{DD}	V	
	V _{IH} (6)	V _{DD} = 1.8 to 5.5 V		\overline{RES}	0.8 V _{DD}		V _{DD}	V
	V _{IH} (7)	External clock specifications		OSC1	0.8 V _{DD}		V _{DD}	V
Input low-level voltage	V _{IL} (1)	Output n-channel transistors off	Port	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (2)	Output n-channel transistors off	\overline{INT} , \overline{SCK} , SI	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (3)	External clock specifications	OSC1	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (4)		TEST	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (5)		\overline{RES}	V _{SS}		0.2 V _{DD}	V	

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LC651204N/F/L, LC651202N/F/L

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating frequency (cycle time)	fop (T cyc)			670 (6)		4330 (0.97)	kHz (μs)
External clock conditions							
Frequency	text	Figure 1	OSC1	670		4330	kHz
Pulse width	textH, textL		OSC1	69			ns
Rise and fall times	textR, textF		OSC1			50	ns
Guaranteed oscillator constants		Figure 2		See table 1.			
Ceramic oscillator							

Electrical Characteristics at Ta = -40 to +85°C, VSS = 0 V, VDD = 3.0 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Input high-level current	I _{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = 13.5 V	Ports C, D, E, and F with open-drain specifications			5.0	μA
	I _{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = V _{DD}	Ports A and G with open-drain specifications			1.0	μA
	I _{IH} (3)	External clock mode, V _{IN} = V _{DD}	OSC1			1.0	μA
Input low-level current	I _{IL} (1)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with open-drain specifications	-1.0			μA
	I _{IL} (2)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	I _{IL} (3)	V _{IN} = V _{SS}	$\overline{\text{RES}}$	-45	-10		μA
	I _{IL} (4)	External clock mode, V _{IN} = V _{SS}	OSC1	-1.0			μA
Output high-level voltage	V _{OH} (1)	I _{OH} = -50 μA	Ports with pull-up resistor specifications	V _{DD} - 1.2			V
	V _{OH} (2)	I _{OH} = -10 μA	Ports with pull-up resistor specifications	V _{DD} - 0.5			V
Output low-level voltage	V _{OL} (1)	I _{OL} = 10 mA	Port			1.5	V
	V _{OL} (2)	I _{OL} = 1 mA, with the I _{OL} for all ports no more than 1 mA.	Port			0.5	V
Schmitt characteristics	Hysteresis voltage	V _{HIS}			0.1 V _{DD}		V
	High-level threshold voltage	V _{tH}	$\overline{\text{RES}}$, $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI OSC1 with Schmitt specifications *4	0.4 V _{DD}		0.8 V _{DD}	V
	Low-level threshold voltage	V _{tL}		0.25V _{DD}		0.6 V _{DD}	V
Current drain	I _{DDOP} (1)	Figure 2, 4 MHz	V _{DD}		2	6	mA
Ceramic oscillator							
External clock	I _{DDOP} (2)	670 to 1444 kHz *1 Operating, output n-channel transistors off, Ports = V _{DD}	V _{DD}		2	6	mA
Standby mode	I _{DDst}	Output n-channel transistor off, Ports = V _{DD}	V _{DD} = 5.5 V		0.05	10	μA
			V _{DD} = 3 V	V _{DD}		0.025	5

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LC651204N/F/L, LC651202N/F/L

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Oscillator characteristics							
Ceramic oscillator							
Oscillator frequency	f_{CFOSC}	Figure 2, $f_o = 4 \text{ MHz} *5$	OSC1, OSC2	3840	4000	4160	kHz
Oscillator stabilization time	t_{CFS}	Figure 3, $f_o = 4 \text{ MHz}$				5	ms
Pull-up resistors		Output n-channel transistor off					
I/O ports	R_{PP}	$V_{in} = V_{SS}, V_{DD} = 5 \text{ V}$	Ports with pull-up resistor specifications	8	14	30	$k\Omega$
\overline{RES}	R_u	$V_{in} = V_{SS}, V_{DD} = 5 \text{ V}$	\overline{RES}	100	250	400	$k\Omega$
External reset characteristics							
Reset time	t_{RST}				See Figure 4.		
Pin capacitance	C_p	$f = 1 \text{ MHz}$ With all pins other than the pin being measured at $V_{IN} = V_{SS}$			10		pF
Serial clock							
Input clock cycle time	$t_{CKCY} (1)$	Figure 5	\overline{SCK}	2.0			μs
Output clock cycle time	$t_{CKCY} (2)$	Figure 5	\overline{SCK}		$64 \times T_{CYC} *6$		μs
Input clock low-level pulse width	$t_{CKL} (1)$	Figure 5	\overline{SCK}	0.6			μs
Output clock low-level pulse width	$t_{CKL} (2)$	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs
Input clock high-level pulse width	$t_{CKH} (1)$	Figure 5	\overline{SCK}	0.6			μs
Output clock high-level pulse width	$t_{CKH} (2)$	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs
Serial input							
Data setup time	t_{ICK}	Stipulated with respect to the rising edge of \overline{SCK} .	SI	0.2			μs
Data hold time	t_{ICKI}	Figure 5	SI	0.2			μs
Serial output							
Output delay time	t_{CKO}	Stipulated with respect to the falling edge of \overline{SCK} . For n-channel open-drain outputs only. External resistance: 1 $k\Omega$, external capacitance: 50 pF. Figure 5	SO			0.4	μs
Pulse output							
Period	t_{PCY}	Figure 6	PE0		$64 \times T_{CYC}$		μs
High-level pulse width	t_{PH}	$T_{cyc} = 4 \times$ the system clock period For n-channel open-drain outputs only: External resistance: 1 $k\Omega$, external capacitance: 50 pF	PE0		$32 \times T_{CYC} \pm 10\%$		μs
Low-level pulse width	t_{PL}		PE0		$32 \times T_{CYC} \pm 10\%$		μs

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LC651204N/F/L, LC651202N/F/L

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Parameter	Symbol	Conditions	V_{DD} (v)	Applicable pins/notes	Ratings				
					min	typ	max	Unit	
Watchdog timer	Guaranteed constants *7	C_W	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.01±5%		μF
		R_W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R_I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t_{WCT}	See Figure 7.		WDR	10			μs
	Clear period (charge)	t_{WCCY}	See Figure 7.		WDR	3.0			ms
	Guaranteed constants *7	Guaranteed constants *7	C_W		When PE1 has open-drain output specifications	4.5 to 5.5	WDR		0.01±5%
R_W			When PE1 has open-drain output specifications	WDR			680±1%		kΩ
R_I			When PE1 has open-drain output specifications	WDR			100±1%		Ω
Clear time (discharge)		t_{WCT}	See Figure 7.	WDR	10				μs
Clear period (charge)		t_{WCCY}	See Figure 7.	WDR	3.3				ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period
3. The operating power-supply voltage V_{DD} must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for f_{CFOSC} are the frequencies for which oscillation is possible.
6. $T_{cyc} = 4 \times$ the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

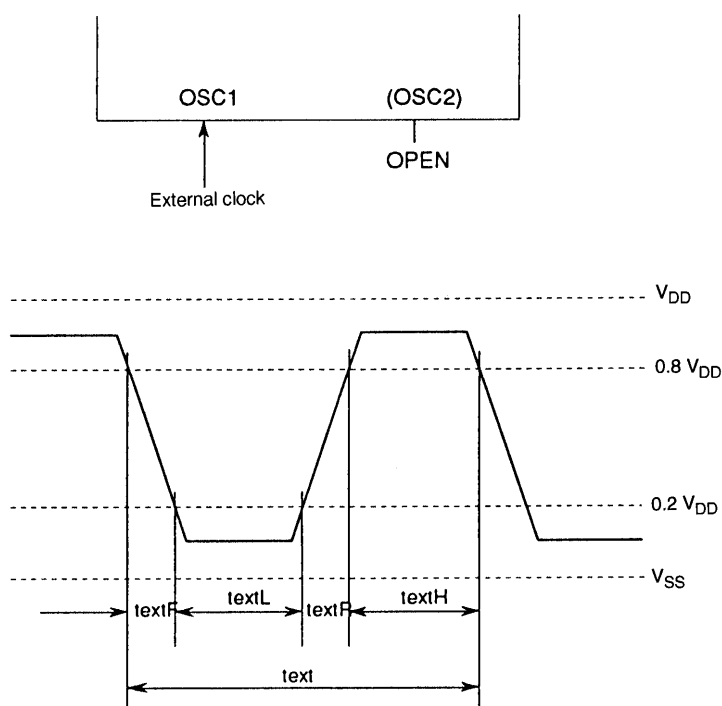


Figure 1 External Clock Input Waveform

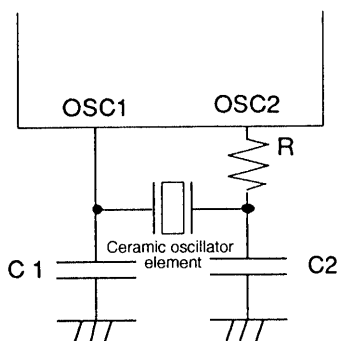


Figure 2 Ceramic Oscillator Circuit

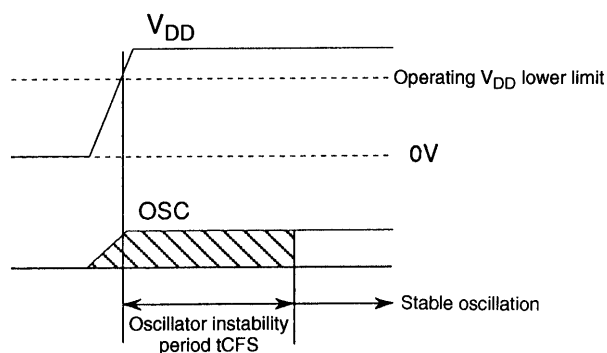


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG CST4.00MGW (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
4 MHz (Kyocera Corporation) KBR4.0MSA KBR4.0MKS (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω

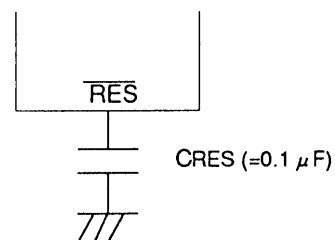


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

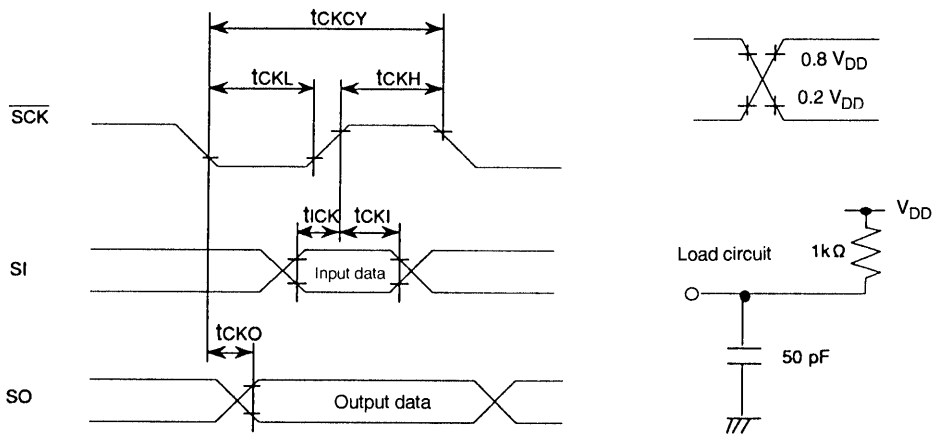


Figure 5 Serial I/O Timing

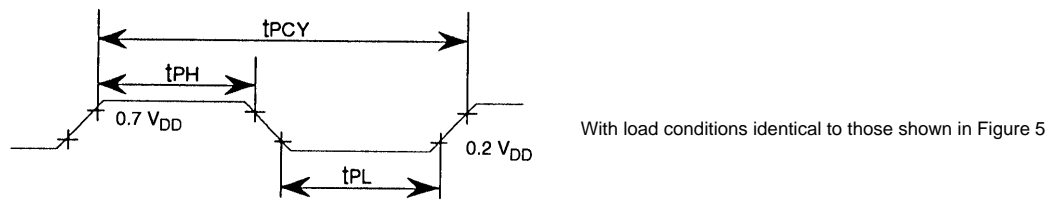
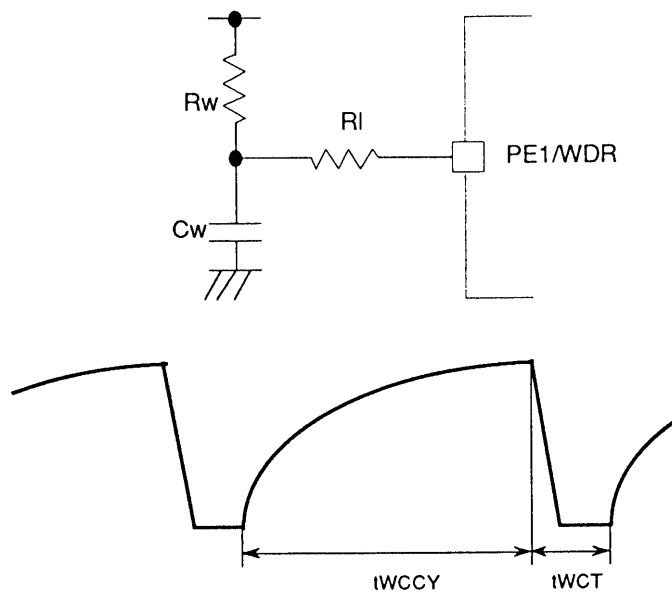


Figure 6 Port PE0 Pulse Output Timing



t_{WCCY} : Charge time due to the external components C_W , R_W , and R_I .
 t_{WCT} : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

LC651204N/F/L, LC651202N/F/L

LC651204L, 651202L

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings	Unit
Maximum supply voltage	V _{DD} max		V _{DD}	-0.3 to +7.0	V
Output voltage	V _O		OSC2	Voltages up to any generated voltage are allowed.	V
Input voltage	V _I (1)		OSC1*1	-0.3 to V _{DD} +0.3	V
	V _I (2)		TEST, $\overline{\text{RES}}$	-0.3 to V _{DD} +0.3	V
I/O voltage	V _{IO} (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	V
	V _{IO} (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to V _{DD} +0.3	V
	V _{IO} (3)	PA0 to 3, PG0 to 3		-0.3 to V _{DD} +0.3	V
Peak output current	I _{OP}		I/O ports	-2 to +20	mA
Average output current	I _{OA}	Average value per pin over a 100-ms period	I/O ports	-2 to +20	mA
	Σ I _{OA} (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1 *2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	mA
	Σ I _{OA} (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3 *2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	mA
Allowable power dissipation	Pd max (1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = -40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V, VDD = 2.5 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			Unit	
				min	typ	max		
Operating power-supply voltage	V _{DD}		V _{DD}	2.5		5.5	V	
Standby power-supply voltage	V _{ST}	RAM and register values retained *3	V _{DD}	1.8		5.5	V	
Input high-level voltage	V _{IH} (1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7 V _{DD}		13.5	V	
	V _{IH} (2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (3)	Output n-channel transistors off	Port A, G	0.7 V _{DD}		V _{DD}	V	
	V _{IH} (4)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with OD specifications	0.8 V _{DD}		13.5	V	
	V _{IH} (5)	Output n-channel transistors off	The $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI pins with PU specifications	0.8 V _{DD}		V _{DD}	V	
	V _{IH} (6)	V _{DD} = 1.8 to 5.5 V		$\overline{\text{RES}}$	0.8 V _{DD}		V _{DD}	V
	V _{IH} (7)	External clock specifications		OSC1	0.8 V _{DD}		V _{DD}	V
Input low-level voltage	V _{IL} (1)	Output n-channel transistors off	Port	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (2)	Output n-channel transistors off	$\overline{\text{INT}}$, $\overline{\text{SCK}}$, SI	V _{SS}		0.15 V _{DD}	V	
	V _{IL} (3)	External clock specifications	OSC1	V _{SS}		0.15 V _{DD}	V	
	V _{IL} (4)		TEST	V _{SS}		0.2 V _{DD}	V	
	V _{IL} (5)		$\overline{\text{RES}}$	V _{SS}		0.15 V _{DD}	V	

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Continued from preceding page.

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Operating frequency (cycle time)	fop (T _{Cyc})	Frequencies up to 4.16 MHz are supported if the divide-by-four divider circuit option is used.		670 (6)		1040 (3.84)	kHz (μs)
External clock conditions Frequency Pulse width Rise and fall times	text textH, textL textR, textF	Figure 1. The divide-by- three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.040 MHz.	OSC1 OSC1 OSC1	670 150		4160 100	kHz ns ns
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See table 1.			

Electrical Characteristics at Ta = -40 to +85°C, V_{SS} = 0 V, V_{DD} = 2.5 to 5.5 V (unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Input high-level current	I _{IH} (1)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = 13.5 V	Ports C, D, E, and F with open drain specifications			5.0	μA
	I _{IH} (2)	Output n-channel transistor off (Includes the n-channel transistor off leakage current.) V _{IN} = V _{DD}	Ports A and G with open drain specifications			1.0	μA
	I _{IH} (3)	External clock mode, V _{IN} = V _{DD}	OSC1			1.0	μA
Input low-level current	I _{IL} (1)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with open drain specifications	-1.0			μA
	I _{IL} (2)	Output n-channel transistor off V _{IN} = V _{SS}	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	I _{IL} (3)	V _{IN} = V _{SS}	$\overline{\text{RES}}$	-45	-10		μA
	I _{IL} (4)	External clock mode, V _{IN} = V _{SS}	OSC1	-1.0			μA
Output high-level voltage	V _{OH} (1)	I _{OH} = -10 μA	Ports with pull-up resistor specifications	V _{DD} - 0.5			V
Output low-level voltage	V _{OL} (1)	I _{OL} = 3 mA	Port			1.5	V
	V _{OL} (2)	I _{OL} = 1 mA, with the I _{OL} for all ports no more than 1 mA.	Port			0.4	V
Schmitt characteristics	Hysteresis voltage	V _{HIS}			0.1 V _{DD}		V
	High-level threshold voltage	V _{tH}	$\overline{\text{RES}}$, $\overline{\text{INT}}$, $\overline{\text{SCK}}$, and SI OSC1 with Schmitt specifications *4	0.4 V _{DD}		0.8 V _{DD}	V
	Low-level threshold voltage	V _{tL}		0.2 V _{DD}		0.6 V _{DD}	V

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings				
				min	typ	max	Unit	
Current drain	I _{DDOP} (1)	Operating, output n-channel transistors off, Ports = V _{DD} Figure 2, 4 MHz, divide-by-four circuit	V _{DD}		1.5	4	mA	
Ceramic oscillator		I _{DDOP} (2)	Figure 2, 4 MHz, divide-by-four circuit V _{DD} = 2.5 V	V _{DD}		0.5	1	mA
		I _{DDOP} (3)	Figure 2, 800 kHz	V _{DD}		1.5	4.0	mA
External clock	I _{DDOP} (4)	670 to 1024 kHz, no divider circuit 2000 to 3120 kHz, divide-by-three circuit 2600 to 4160 kHz, divide-by-four circuit	V _{DD}		1.5	4	mA	
Standby mode	I _{DDst}	Output n-channel transistor off, Ports = V _{DD}	V _{DD}		0.05	10	μA	
			V _{DD}		0.020	4	μA	
Oscillator characteristics	f _{CFOSC} *5	Figure 2, fo = 800 kHz Figure 2, fo = 1 MHz Figure 2, fo = 4 MHz, divide-by-four circuit	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	768 960 3840	800 1000 4000	832 1040 4160	kHz kHz kHz	
Oscillator frequency								
Oscillator stabilization time								t _{CFS}
Pull-up resistors I/O ports	R _{PP}	Output n-channel transistor off V _{in} = V _{SS} , V _{DD} = 5 V	Ports with pull-up resistor specifications	8	14	30	kΩ	
$\overline{\text{RES}}$	R _u	V _{in} = V _{SS} , V _{DD} = 5 V	$\overline{\text{RES}}$	100	250	400	kΩ	
External reset characteristics	t _{RST}			See Figure 4.				
Reset time								
Pin capacitance	C _p	f = 1 MHz With all pins other than the pin being measured at V _{IN} = V _{SS}			10		pF	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			
				min	typ	max	Unit
Serial clock Input clock cycle time	$t_{CKCY} (1)$	Figure 5	\overline{SCK}	6.0			μs
Output clock cycle time	$t_{CKCY} (2)$	Figure 5	\overline{SCK}		$64 \times T_{CYC}$ *6		μs
Input clock low-level pulse width	$t_{CKL} (1)$	Figure 5	\overline{SCK}	2.0			μs
Output clock low-level pulse width	$t_{CKL} (2)$	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs
Input clock high-level pulse width	$t_{CKH} (1)$	Figure 5	\overline{SCK}	2.0			μs
Output clock high-level pulse width	$t_{CKH} (2)$	Figure 5	\overline{SCK}		$32 \times T_{CYC}$		μs
Serial input Data setup time	t_{iCK}	Stipulated with respect to the rising edge of \overline{SCK} .	SI	0.5			μs
Data hold time	t_{CKI}	Figure 5	SI	0.5			μs
Serial output Output delay time	t_{CKO}	Stipulated with respect to the falling edge of \overline{SCK} . For n-channel open-drain outputs only: External resistance: 1 k Ω , external capacitance: 50 pF. Figure 5	SO			1.0	μs
Pulse output period	t_{PCY}	Figure 6	PE0		$64 \times T_{CYC}$		μs
High-level pulse width	t_{PH}	$T_{cyc} = 4 \times$ the system clock period For n-channel open-drain outputs only: External resistance: 1 k Ω , external capacitance: 50 pF	PE0		$32 \times T_{CYC}$ $\pm 10\%$		μs
Low-level pulse width	t_{PL}		PE0		$32 \times T_{CYC}$ $\pm 10\%$		μs

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Parameter	Symbol	Conditions	V _{DD} (v)	Applicable pins/notes	Ratings				
					min	typ	max	Unit	
Watchdog timer	Guaranteed constants *7	C _W	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.1±5%		μF
		R _W	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		R _I	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t _{WCT}	See Figure 7.		WDR	100			μs
	Clear period (charge)	t _{WCCY}	See Figure 7.		WDR	26			ms
	Guaranteed constants *7	C _W	When PE1 has open-drain output specifications		2.5 to 5.5	WDR		0.047±5%	
R _W		When PE1 has open-drain output specifications	WDR			680±1%		kΩ	
R _I		When PE1 has open-drain output specifications	WDR			100±1%		Ω	
Clear time (discharge)		t _{WCT}	See Figure 7.	WDR		40			μs
Clear period (charge)		t _{WCCY}	See Figure 7.	WDR		12			ms

Note: 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.

2. The average over a 100-ms period
3. The operating power-supply voltage V_{DD} must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for f_{CFOSC} are the frequencies for which oscillation is possible.
6. T_{cyc} = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

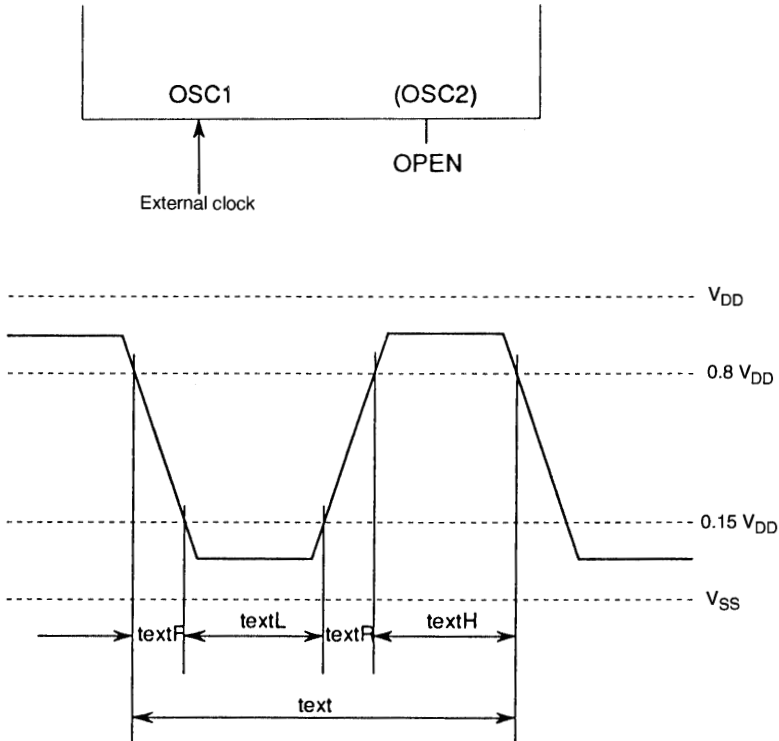


Figure 1 External Clock Input Waveform

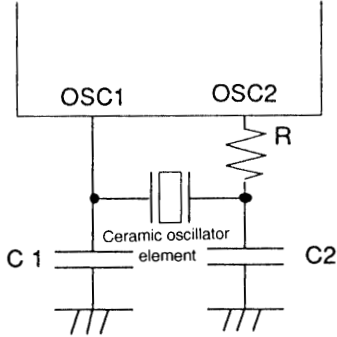


Figure 2 Ceramic Oscillator Circuit

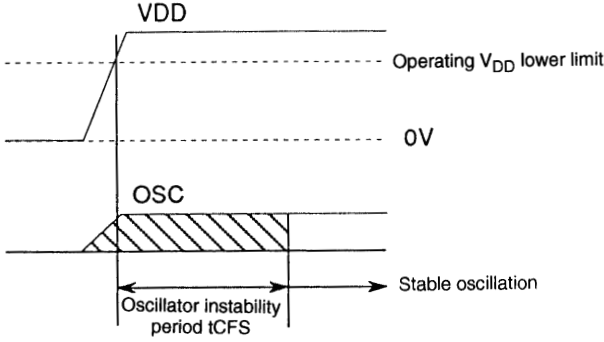


Figure 3 Oscillator Stabilization Period

Table 1: Guaranteed Ceramic Oscillator Constants

4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MGU CST4.0MGWU (built-in capacitor version)	C1	33 pF ± 10%
	C2	33 pF ± 10%
	R	0 Ω
1 MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
1 MHz (Kyocera Corporation) KBR1000F	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	0 Ω
800 kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF ± 10%
	C2	100 pF ± 10%
	R	2.2 kΩ
800 kHz (Kyocera Corporation) KBR800F	C1	220 pF ± 10%
	C2	220 pF ± 10%
	R	0 Ω

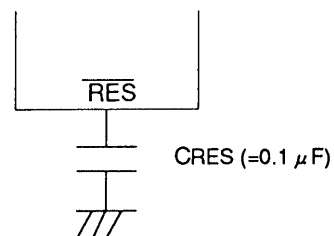


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

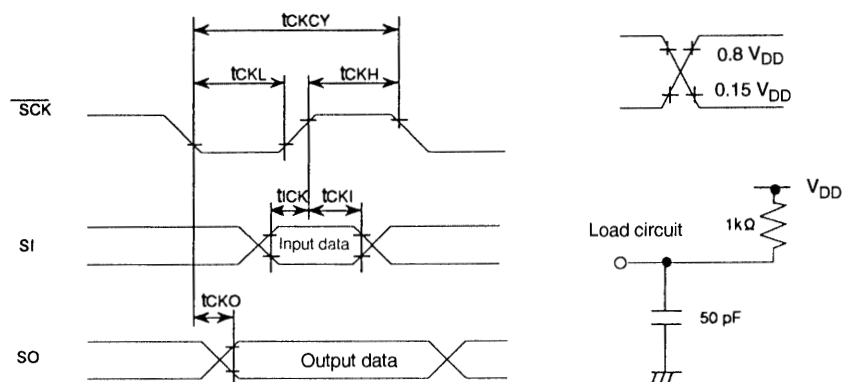
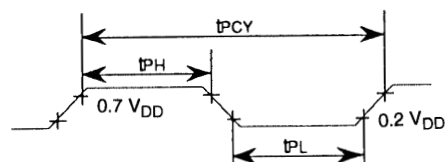
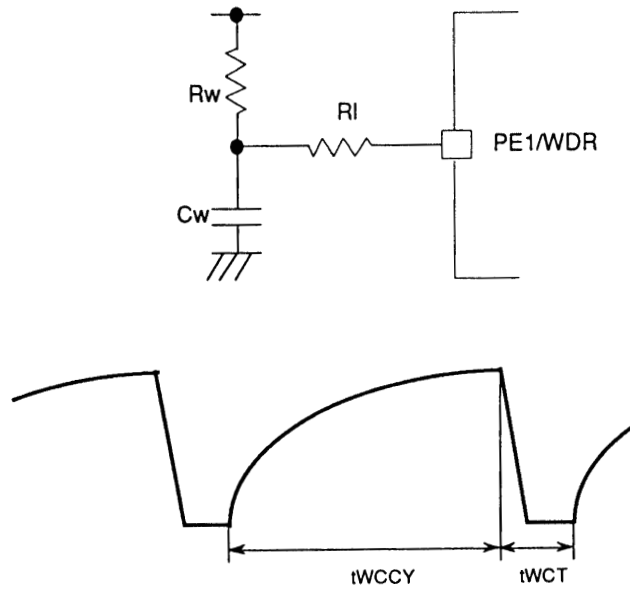


Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



t_{WCCY} : Charge time due to the external components C_w , R_w , and R_I
 t_{WCT} : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

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LC651204/1202 Instruction Set (by function)

Abbreviations

AC: Accumulator	M: Memory	ZF : Zero flag
ACT: Accumulator bit t	M(DP): Memory addressed by DP	() [] : Indicates the contents of the item enclosed.
CF: Carry flag	P(DPL): I/O port specified by DPL	← : Transfer and direction
CTL: Control register	PC: Program counter	+ : Addition
DP: Data pointer	STACK: Stack pointer	- : Subtraction
E: E register	TM: Timer	^ : Logical AND
EXTF: External interrupt request flag	TMF: Timer (internal) interrupt request flag	∨ : Logical OR
F _n : Flag bit n	At, Ha, La: Working registers	⊕ : Logical exclusive OR

Instruction group	Mnemonic	Instruction code								Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes	
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀							
Accumulator manipulation instructions	CLA	Clear AC	1	1	0	0	0	0	0	0	1	1	AC ← 0	Clears AC.	ZF	*1
	CIC	Clear CF	1	1	1	0	0	0	0	1	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	1	1	1	1	0	0	0	1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	1	1	1	0	1	0	1	1	1	1	AC ← (AC)	Sets AC to the one's	ZF	
	INC	Increment AC	0	0	0	0	1	1	1	0	1	1	AC ← (AC) + 1	Increments AC.	ZF CF	
	DEC	Decrement AC	0	0	0	0	1	1	1	1	1	1	AC ← (AC) - 1	Decrements AC.	ZF CF	
	RAL	Rotate AC left through CF	0	0	0	0	0	0	0	1	1	1	AC ₀ ← (CF), AC _{p+1} ← (AC _p), CF ← (AC ₃)	Shifts AC together with CF left.	ZF CF	
	TAE	Transfer AC to E	0	0	0	0	0	0	1	1	1	1	E ← (AC)	Moves the contents of AC to E.		
	XAE	Exchange AC with E	0	0	0	0	1	1	0	1	1	1	(AC) ↔ (E)	Exchanges the contents of AC and E.		
	Memory manipulation instructions	INM	Increment M	0	0	1	0	1	1	1	0	1	1	M(DP) ← [M(DP)] + 1	Increments M(DP).	ZF CF
DEm		Decrement M	0	0	1	0	1	1	1	1	1	1	M(DP) ← [M(DP)] - 1	Decrements M(DP).	ZF CF	
SmB bit		Set M data bit	0	0	0	0	1	0	B ₁	B ₀	1	1	M(DP, B ₁ B ₀) ← 1	Sets the bit in M(DP) specified by B ₁ B ₀ to 1.		
RMB bit		Reset M data bit	0	0	1	0	1	0	B ₁	B ₀	1	1	M(DP, B ₁ B ₀) ← 0	Clears the bit in M(DP) specified by B ₁ B ₀ to 0.		
Arithmetic and comparison instructions	AD	Add M to AC	0	1	1	0	0	0	0	0	1	1	AC ← (AC) + [M(DP)]	Adds the contents of AC and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	ADC	Add M to AC with CF	0	0	1	0	0	0	0	0	1	1	AC ← (AC) + [M(DP)] + (CF)	Adds the contents of AC, CF, and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1	1	1	0	0	1	1	0	1	1	AC ← (AC) + 3	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1	1	1	0	1	0	1	0	1	1	AC ← (AC) + 10	Adds 10 to AC.	ZF	
	EXL	Exclusive or M to AC	1	1	1	1	0	1	0	1	1	1	AC ← (AC) ⊕ [M(DP)]	Takes the logical exclusive OR of AC and M(DP) and stores the result in AC.	ZF	
	AND	And M to AC	1	1	1	0	0	1	1	1	1	1	AC ← (AC) ∧ [M(DP)]	Takes the logical AND of AC and M(DP) and stores the result in AC.	ZF	
	OR	Or M to AC	1	1	1	0	0	1	0	1	1	1	AC ← (AC) ∨ [M(DP)]	Takes the logical OR of AC and M(DP) and stores the result in AC.	ZF	
	CM	Compare AC with M	1	1	1	1	1	0	1	1	1	1	[M(DP)] + (AC) + 1	Compares the contents of AC and M(DP) and sets or clears CF and ZF accordingly.	ZF CF	
	CI data	Compare AC with immediate data	0	0	1	0	0	1	0	0	2	2	I ₃ I ₂ I ₁ I ₀ + (AC) + 1	Compares the contents of AC and the immediate data I ₃ I ₂ I ₁ I ₀ and sets or clears CF and ZF accordingly.	ZF CF	
	CLI data	Compare DP _L with immediate data	0	0	1	0	0	1	0	0	2	2	(DP _L) ∨ I ₃ I ₂ I ₁ I ₀	Compares the contents of DPL and the immediate data.	ZF	
Load and store instructions	LI data	Load AC with immediate data	1	1	0	0	I ₃	I ₂	I ₁	I ₀	1	1	AC ← I ₃ I ₂ I ₁ I ₀	Loads AC with the immediate data I ₃ I ₂ I ₁ I ₀ .	ZF	*1
	S	Store AC to M	0	0	0	0	0	0	1	0	1	1	M(DP) ← (AC)	Stores the contents of AC at M(DP).		
	L	Load AC from M	0	0	1	0	0	0	0	1	1	1	AC ← [M(DP)]	Loads the contents of M(DP) into AC.	ZF	
	XM data	Exchange AC with M then modify DP _H with immediate data	1	0	1	0	0	M ₂	M ₁	M ₀	1	2	(AC) ↔ [M(DP)] DP _H ← (DP _H) ⊕ 0 M ₂ M ₁ M ₀	Exchanges the contents of AC and M(DP). Then, replaces the contents of DPH with (DP _H) ⊕ 0 M ₂ M ₁ M ₀ .	ZF	ZF is set to indicate the result of the (DPH) ⊕ 0 M ₂ M ₁ M ₀ operation.
	X	Exchange AC with M	1	0	1	0	0	0	0	0	1	2	(AC) ↔ [M(DP)]	Exchanges the contents of AC and M(DP).	ZF	ZF is set according to the contents of DPH at the point the instruction was executed.
	XI	Exchange AC with M then increment DP _L	1	1	1	1	1	1	1	0	1	2	(AC) ↔ [M(DP)] DP _L ← (DP _L) + 1	Exchanges the contents of AC and M(DP). Then, increments the contents of DP _L .	ZF	ZF is set to indicate the result of the DP _L + 1 operation.
XD	Exchange AC with M then Decrement DP _L	1	1	1	1	1	1	1	1	1	2	(AC) ↔ [M(DP)] DP _L ← (DP _L) - 1	Exchanges the contents of AC and M(DP). Then, Decrements the contents of DP _L .	ZF	ZF is set to indicate the result of the DP _L - 1 operation.	
RTBI	Read table data from program ROM	0	1	1	0	0	0	1	1	1	2	AC, E ↔ ROM (PCh, E, AC)	Loads into AC and E the ROM data stored at the location given by the lower 8 bits of the PC, E and AC.			

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Instruction group	Mnemonic	Instruction code								Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes		
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀								
Data pointer manipulation instructions	LDZ data	Load DP _H with Zero and DP _L with immediate data respectively		1	0	0	0	l ₃	l ₂	l ₁	l ₀	1	1	DP _H ← 0 DP _L ← l ₃ l ₂ l ₁ l ₀	Loads 0 into DP _H and the immediate data l ₃ l ₂ l ₁ l ₀ into DP _L .		
	LHI data	Load DPH with immediate data		0	1	0	0	l ₃	l ₂	l ₁	l ₀	1	1	DP _H ← l ₃ l ₂ l ₁ l ₀	Loads the immediate data l ₃ l ₂ l ₁ l ₀ into DP _H .		
	IND	Increment DP _L		1	1	1	0	1	1	1	0	1	1	DP _L ← (DP _L) + 1	Increases the contents of DP _L .	ZF	
	DED	Decrement DP _L		1	1	1	0	1	1	1	1	1	1	DP _L ← (DP _L) - 1	Decrements the contents of DP _L .	ZF	
	TAL	Transfer AC to DP _L		1	1	1	1	1	1	1	1	1	1	DP _L ← (AC)	Moves the contents of AC to DP _L .		
	TLA	Transfer DPL to AC		1	1	1	0	1	0	0	1	1	1	AC ← (DP _L)	Moves the contents of DPL to AC.	ZF	
	XAH	Exchange AC with DPH		0	0	1	0	0	0	1	1	1	1	(AC) ↔ (DP _H)	Exchanges the contents of AC and DP _H .		
Working register manipulation instructions	XAt	Exchange AC with working register At		1	1	1	0	t1	t0			1	1	(AC) ↔ (A0)	Exchanges the contents of AC and the working register A0, A1, A2, or A3 specified by t1t0.		
	XA0			1	1	1	0	0	0	0	0	1	1	(AC) ↔ (A1)			
	XA1			1	1	1	0	0	1	0	0	1	1	(AC) ↔ (A2)			
	XA2			1	1	1	0	1	0	0	0	1	1	(AC) ↔ (A3)			
	XA3			1	1	1	0	1	1	0	0	1	1	(AC) ↔ (A3)			
	XHa	Exchange DPH with working register Ha		1	1	1	1	1	0	0	0	1	1	(DP _H) ↔ (H0)	Exchanges the contents of DP _H and the working register H0 or H1 specified by a.		
XH1	1	1	1	1	1	1	0	0	1	1	(DP _H) ↔ (H1)						
XLa	Exchange DPH with working register Ha		a											Exchanges the contents of DP _L and the working register L0 or L1 specified by a.			
XL0			1	1	1	1	1	0	0	0	1	1	(DP _L) ↔ (L0)				
XL1	1	1	1	1	1	1	0	0	1	1	(DP _L) ↔ (L1)						
Memory manipulation instructions	SFB flag	Set flag bit		0	1	0	1	B ₃	B ₂	B ₁	B ₀	1	1	F _n ← 1	Sets the flag specified by B ₃ B ₂ B ₁ B ₀ to 1.		
	RFB flag	Reset flag bit		0	0	0	1	B ₃	B ₂	B ₁	B ₀	1	1	F _n ← 0	Clears the flag specified by B ₃ B ₂ B ₁ B ₀ to 0.	ZF	The flags are divided into four groups, F0 to F3, F4 to F7, F8 to F11, and F12 to F15. ZF is set or cleared according to the 4 bits included in the specified flags.
Jump and subroutine instructions	JMP addr	Jumping in the current bank		0	1	1	0	1	P ₁₀	P ₉	P ₈	2	2	PC ← P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀	Jumps to the location specified by the immediate data P ₁₀ P ₉ P ₈ P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ .		
	JPEA	Jumping current page modified by E and AC		1	1	1	1	1	0	1	0	1	1	PC ₀ to ₇ ← (E, AC)	Jumps to the location given by replacing the lower 8 bits of the PC with E and AC.		
	CZP addr	Call subroutine in the zero page		1	0	1	1	P ₃	P ₂	P ₁	P ₀	1	1	STACK ← (PC) + 1 PC ₁₀ to ₆ , PC ₁ to ₀ ← 0 PC ₅ to ₂ ← P ₃ P ₂ P ₁ P ₀	Calls a subroutine on page 0.		
	CAL addr	Call subroutine		1	0	1	0	1	P ₁₀	P ₉	P ₈	2	2	STACK ← (PC) + 2	Calls a subroutine.		
	RT	Return from subroutine		0	1	1	0	0	0	1	0	1	1	PC ← (STACK)	Returns from a subroutine.		
	RTI	Return from interrupt routine		0	0	1	0	0	0	1	0	1	1	PC ← (STACK) CF, ZF ← CSF, ZSF	Returns from an interrupt handling routine.	ZF	CF
	BANK	Change bank		1	1	1	1	1	1	0	1	1	1		Specifies a pseudo I/O port and changes the bank.		Only valid for the immediately following JMP, I/O, or branch instruction.
Branch instructions	BAt addr	Change bank		0	1	1	1	0	0	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if Act = 1	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in AC specified by the immediate data t1t0 is 1.		The mnemonics are BA0 to BA3, reflecting the value of t.
	BNAt addr	Branch on no AC bit		0	0	1	1	0	0	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if Act = 0	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in AC specified by the immediate data t1t0 is 0.		The mnemonics are BNA0 to BNA3, reflecting the value of t.
	BMt addr	Branch on M bit		0	1	1	1	0	1	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M(DP, t ₁ t ₀)] = 1	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in M(DP) specified by the immediate data t ₁ t ₀ is 1.		The mnemonics are BM0 to BM3, reflecting the value of t.
	BNMt addr	Branch on no M bit		0	0	1	1	0	1	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [M(DP, t ₁ t ₀)] = 0	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in M(DP) specified by the immediate data t ₁ t ₀ is 0.		The mnemonics are BNM0 to BNM3, reflecting the value of t.
	BPt addr	Branch on Port bit		0	1	1	1	1	0	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [P(DP _L , t ₁ t ₀)] = 1	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in port P(DPL) specified by the immediate data t ₁ t ₀ is 1.		The mnemonics are BP0 to BP3, reflecting the value of t.
	BNPt addr	Branch on no Port bit		0	0	1	1	1	0	t ₁	t ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if [P(DP _L , t ₁ t ₀)] = 0	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in port P(DPL) specified by the immediate data t ₁ t ₀ is 0.		The mnemonics are BNP0 to BNP3, reflecting the value of t.
	BTM addr	Branch on timer		0	1	1	1	1	0	0	0	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P ₇ to P ₀ if TMF is 1. Also clears TMF.	TMF	

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Instruction group	Mnemonic		Instruction code				Number of bytes	Number of cycles	Operation	Description	Modified status flags	Notes					
			D ₇	D ₆	D ₅	D ₄							D ₃	D ₂	D ₁	D ₀	
Branch instructions	BNTM addr	Branch on no timer	0 P ₇	0 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	0 P ₁	0 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P ₇ to P ₀ if TMF is 0. Also clears TMF.	TMF		
	BI addr	Branch on interrupt	0 P ₇	1 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	0 P ₁	1 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if EXTF = 1 then EXTF ← 0	Branches to the location on the same page specified by P ₇ to P ₀ if EXTF is 1. Also clears EXTF.	EXTF		
	BNI addr	Branch on no interrupt	0 P ₇	0 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	0 P ₁	1 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if EXTF = 0 then EXTF ← 0	Branches to the location on the same page specified by P ₇ to P ₀ if EXTF is 0. Also clears EXTF.	EXTF		
	BC addr	Branch on CF	0 P ₇	1 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	1 P ₁	1 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if EXTF = 0	Branches to the location on the same page specified by P ₇ to P ₀ if EXTF is 1.			
	BNC addr	Branch on no CF	0 P ₇	0 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	1 P ₁	1 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if CF = 0	Branches to the location on the same page specified by P ₇ to P ₀ if CF is 0.			
	BZ addr	Branch on ZF	0 P ₇	1 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	1 P ₁	0 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if ZF = 1	Branches to the location on the same page specified by P ₇ to P ₀ if ZF is 1.			
	BNZ addr	Branch on no ZF	0 P ₇	0 P ₆	1 P ₅	1 P ₄	1 P ₃	1 P ₂	1 P ₁	0 P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if ZF = 0	Branches to the location on the same page specified by P ₇ to P ₀ if ZF is 0.			
	BFn addr	Branch on flag bit	1 P ₇	1 P ₆	0 P ₅	1 P ₄	n ₃ P ₃	n ₂ P ₂	n ₁ P ₁	n ₀ P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if F _n = 1	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in the 16 flags specified by n ₃ n ₂ n ₁ n ₀ is 1.		The mnemonics are BF0 to BF15, reflecting the value of n.	
	BNFn addr	Branch on no flag bit	1 P ₇	0 P ₆	0 P ₅	1 P ₄	n ₃ P ₃	n ₂ P ₂	n ₁ P ₁	n ₀ P ₀	2	2	PC ₇ to ₀ ← P ₇ P ₆ P ₅ P ₄ P ₇ P ₆ P ₅ P ₄ if F _n = 0	Branches to the location on the same page specified by P ₇ to P ₀ if the bit in the 16 flags specified by n ₃ n ₂ n ₁ n ₀ is 0.		The mnemonics are BFN0 to BFN15, reflecting the value of n.	
I/O instructions	IP	Input port to AC	0	0	0	0	1	1	0	0	1	1	AC ← [P(DP _L)]	Inputs the contents of port P(DP _L) to AC.	ZF		
	OP	Output port to AC	0	1	1	0	0	0	0	1	1	1	P(DP _L , B1 B0) ← (AC)	Outputs the contents of AC to port P(DP _L).			
	SPB bit	Set port bit	0	0	0	0	0	1	B ₁	B ₀	1	2	P(DP _L , B1 B0) ← 1	Sets to 1 the bit in port P(DP _L) specified by the immediate data B ₁ B ₀ .		Executing this instruction destroys the contents of the E register.	
	RPB bit	Reset port bit	0	0	1	0	0	1	B ₁	B ₀	1	2	P(DP _L , B1 B0) ← 1	Clears to 0 the bit in port P(DP _L) specified by the immediate data B ₁ B ₀ .	ZF	Executing this instruction destroys the contents of the E register.	
Other instructions	SCTL bit	Set control register bit (S)	0	0	1	0	1	1	0	0	2	2	CTL ← (CTL) ∨ B ₃ B ₂ B ₁ B ₀	Sets the bit (or bits) in the control register specified by B ₃ B ₂ B ₁ B ₀ .			
	RCTL bit	Reset control register bit (S)	0	0	1	0	1	1	0	0	2	2	CTL ← (CTL) ∨ B ₃ B ₂ B ₁ B ₀	Clears the bit (or bits) in the control register specified by B ₃ B ₂ B ₁ B ₀ .	ZF		
	WTTM	Write timer	1	1	1	1	1	0	1	1	1	1	1	TM ← (E), (AC) TMF ← 0	Loads the contents of E and AC into the timer. Also clears TMF.	TMF	
	HALT	Halt	1	1	1	1	0	1	1	0	1	1	1	Halt	Stops all operations.		This instruction is disabled only when all bits in port PA are 0.
	NOP	No operation	0	0	0	0	0	0	0	0	1	1	1	No operation	Consumes one machine cycle while performing no operation.		

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