TDK SEMICONDUCTOR CORP.

73K321L
CCITT V.23, V.21
Single-Chip Modem

April 2000

DESCRIPTION

The 73K321L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23 and V.21 compatible modem, capable of 0-300 bit/s full-duplex or 0-1200 bit/s half-duplex operation over dial-up telephone lines. The 73K321L provides 1200 bit/s operation in V.23 mode and 300 bit/s in V.21 mode. The 73K321L also can both detect and generate the 2100 Hz answer tone needed for call initiation. The 73K321L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28-pin DIP or PLCC package. The 73K321L operates from a single +5V supply with very low power consumption.

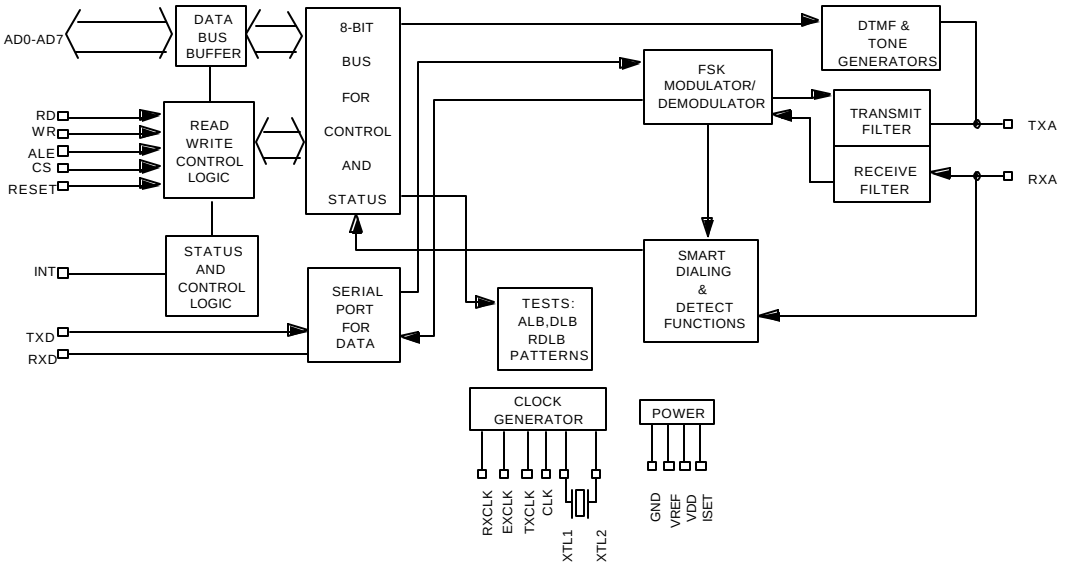
The 73K321L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling tones. The 73K321L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

(continued)

FEATURES

- **One-chip CCITT V.23 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (V.21) or 0-1200 bit/s (V.23) forward channel with or without 0-75 bits/s back channel**
- **Full Duplex 0-1200 bit/s (V.23) in 4-wire mode**
- **Pin and software compatible with other TDK Semiconductor Corporation K-Series 1-chip modems**
- **Interfaces directly with standard micro-processors (8048, 80C51 typical)**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors**
- **DTMF generator**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 60 mW @ 5V from a single power supply**

BLOCK DIAGRAM



DESCRIPTION (continued)

The 73K321L is ideal for either free standing or integral system modem applications where multi-standard data communications over the 2-wire switched telephone network is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K321L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The 73K321L is part of TDK Semiconductor's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The Serial Command mode allows access to the 73K321L control and status registers via a serial command port. In this mode the AD0, AD1 and AD2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after RD is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition). Special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone-pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
GND	28	I	System Ground.
VDD	15	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1µF capacitor.

PARALLEL MICROPROCESSOR CONTROL INTERFACE

ALE	12	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	20	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	O	Output clock. This pin is the output of the crystal oscillator frequency only in the 73K321.
$\overline{INT}$	17	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	I	Read. A low requests a read of the 73K321L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	I	Reset. An active high signal high on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR CONTROL INTERFACE (continued)

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
$\overline{WR}$	13	I	Write. A low on this informs the 73K321L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR CONTROL INTERFACE

AD0-AD2	4-6	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA (AD7)	11	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	14	I	Read. A low on this input informs the 73K321L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	13	I	Write. A low on this input informs the 73K321L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
NOTE: The Serial Control mode is provided by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become the address only. See the Serial Control Timing diagrams on page 18			

DTE USER INTERFACE

NAME	PLCC/DIP PIN NUMBER	TYPE	DESCRIPTION
EXCLK	19	I	External Clock. Used for serial control interface to clock control data in or out of the 73K321L.
RXCLK	23	O	Receive Clock. A clock which is 16 x1200, or 16 x 75 in V.23 mode, or 16 x 300 baud data rate is output in V.21.
RXD	22	O/ Weak Pull-up	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in Synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	O	Transmit Clock. TXCLK is always active. In V.23 mode the output is either a 16 x 1200 baud clock or 16 x 75 baud, in V.21 mode the clock is 16 x 300 baud.
TXD	21	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In Asynchronous modes (1200 or 300 baud) no clocking is necessary.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	I	Received modulated analog signal input from the phone line.
TXA	16	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	I I	These pins are for the internal crystal oscillator requiring an 11.0592 MHz Parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in Serial mode, or the AD0 and AD1 lines in Parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the 73K321L internal state. DR is a detect register which provides an indication of Monitored modem status conditions. TR, the tone control register, controls the DTMF generator; answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

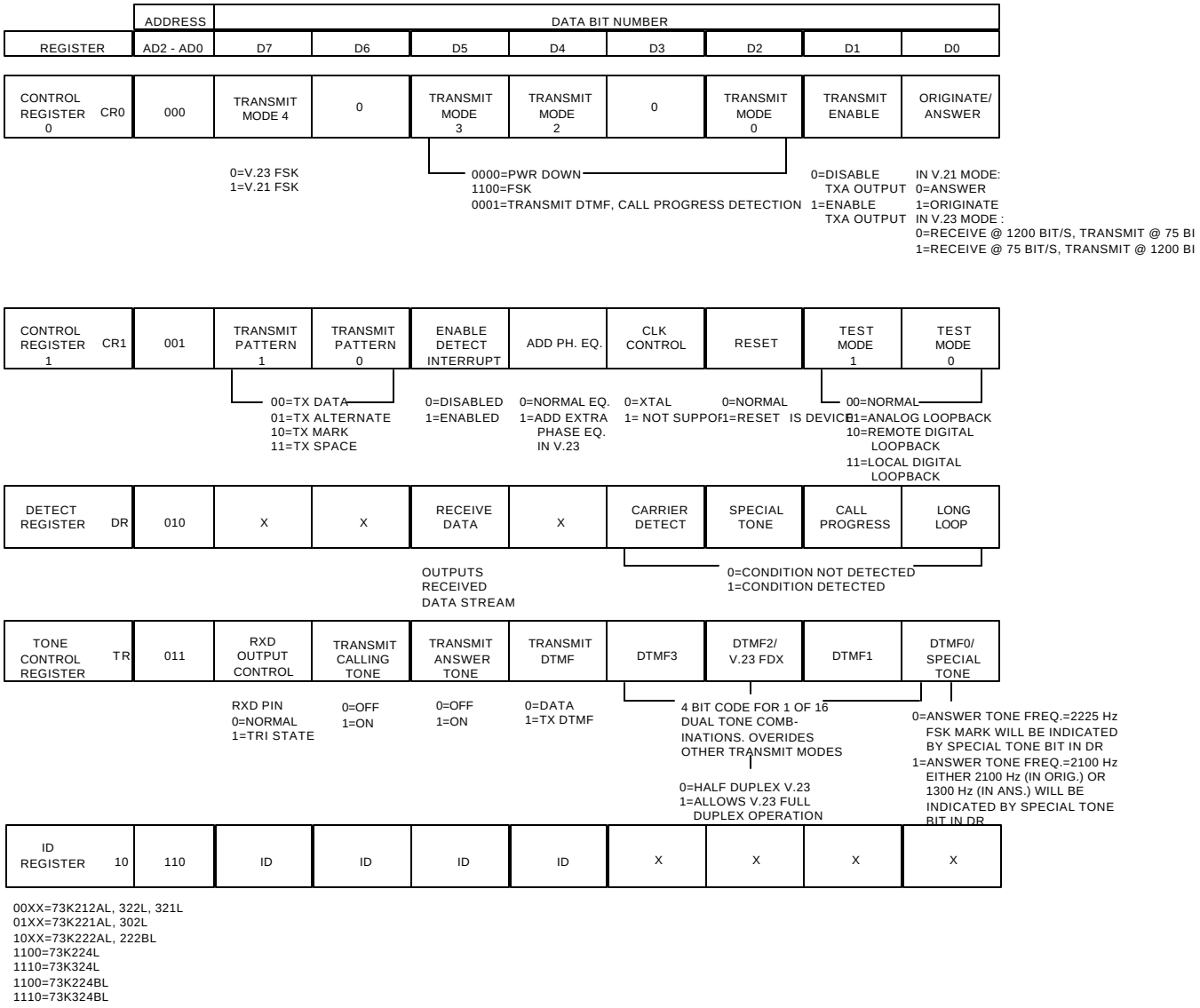
REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	TRANSMIT MODE 4	0	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	X	X	RECEIVE DATA	X	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ ANSWER/SPEC. TONE SELECT
ID REGISTER ID	110	ID	ID	ID	ID	X	X	X	X

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

X = Undefined, mask in software

REGISTER ADDRESS TABLE



00XX=73K212AL, 322L, 321L
01XX=73K221AL, 302L
10XX=73K222AL, 222BL
1100=73K224L
1110=73K324L
1100=73K224BL
1110=73K324BL

X = Undefined, mask in software
0 = Only write zero to these locations

CONTROL REGISTER 0

CR0 000	D7	D6	D5	D4	D3	D2	D1	D0
	TRANSMIT MODE 4	0	TRANSMIT MODE 3	TRANSMIT MODE 2	0	TX DTMF	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects Answer mode in V.21 (transmit in high band, receive in low band) or in V.23 mode, receive at1200 bit/s and transmit at 75 bit/s.
		1	Selects Originate mode in V.21 (transmit in low band, receive in high band) or in V.23 mode, receive at 75 bit/s and transmit at 1200 bit/s. If in V.23 and D2 of TR=1, selects V.23 full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D7, D5, D4, D2	Transmit Mode	D7 D5 D4 D2	
		0 0 0 0	Power Down
		0 0 0 1	Transmit DTMF
		0 1 1 0	V.23 Mode
		1 1 1 0	V.21 Mode
D6, D3	Unused	N/A	Not used; must be written as “0”

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL (WRITE 0)	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION		DESCRIPTION
D1, D0	Test Mode	D1	D0	
		0	0	Selects Normal Operating mode.
		0	1	Analog Loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1	0	Not used.
		1	1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	Program as 0		Not supported in the 73K321.See the TXCLK and RXCLK pin descriptions for 16x the data rate clocks.
D4	Add Ph. Eq.	0		Selects normal equalization.
		1		In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0		Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in Power Down modes.
		1		Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in Power Down mode.
D7, D6	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER

DR 010	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	RECEIVE DATA	X	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
D1	Call Progress Detect	1	Indicates low received signal level.
		0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band when CR0 D2 =1.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 Originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21 or V.23 Answer mode.
			(3) an FSK mark for the mode the device is set to receive in if D0 of TR = 0.
			NOTE: Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unused	Undefined	Not used in the 73K321L. Mask in software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Not Used	Undefined	Mask in software.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.234W/ FDX	DTMF 1	DTMF 0/ ANS. TONE/ SPECIAL TONE/ SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer Tone/ Special Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 Originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21 or V.23 Answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz answer tone in Answer mode.
		X 1 0 1	Transmit 2100 Hz answer tone in Answer mode.
D2	DTMF2/ V.23 4W/FDX	CR0 D7 D5 D4 D2 / TR D2	
		0 1 1 0 / 0	2-wire half duplex
		0 1 1 0 / 1	4-wire full duplex
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF (TR bit D4) and TX enable bit (CR0, bit D2) are set. Tone encoding is shown below:
		0 0 0 0 – 1 1 1 1	

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336

TONE REGISTER (continued)

BIT NO.	NAME	CONDITION	DESCRIPTION					
D3, D2, D1, D0 (continued)			KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
			*	1	0	1	1	941	1209
			#	1	1	0	0	941	1477
			A	1	1	0	1	697	1633
			B	1	1	1	0	770	1633
			C	1	1	1	1	852	1633
			D	0	0	0	0	941	1633
D4	Transmit DTMF	0	Disabled DTMF.						
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.						
D5	Transmit Answer Tone	0	Disables answer tone generator.						
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in Answer mode.						
D6	Transmit Calling Tone	0	Disables calling tone generator.						
		1	Transmit calling tone in either mode.						
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.						
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.						

ID REGISTER

ID	D7	D6	D5	D4	D3	D2	D1	D0
110	ID	ID	ID	ID	X	X	X	X

BIT NO.	NAME	CONDITION D7	D6	D5	D4	DESCRIPTION
D7, D6, D5 D4	Device Identification Signature	D7	D6	D5	D4	Indicates Device:
		0	0	X	X	73K212AL, 73K321L or 73K322L
		0	1	X	X	73K221AL or 73K302L
		1	0	X	X	73K222AL, 73K222BL
		1	1	0	0	73K224L
		1	1	1	0	73K324L
		1	1	0	0	73K224BL
		1	1	1	0	73K324BL
D3-D0	Not Used	Undefined				Mask in software.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD + 0.3V
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics; from pin to GND			40	pF
XTL2 Load Capacitor				20	

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Current	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path from TXA to the telephone line. 2 dB gain in the Receive path from the telephone line to RXA. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator					
Frequency Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, CR0 bit D2=1	-10	-9	-8	dBm0
Output Amplitude	High Band, CR0 bit D2=1	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for V.23 back channel	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		43		dB
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	Single Tone	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (continued)

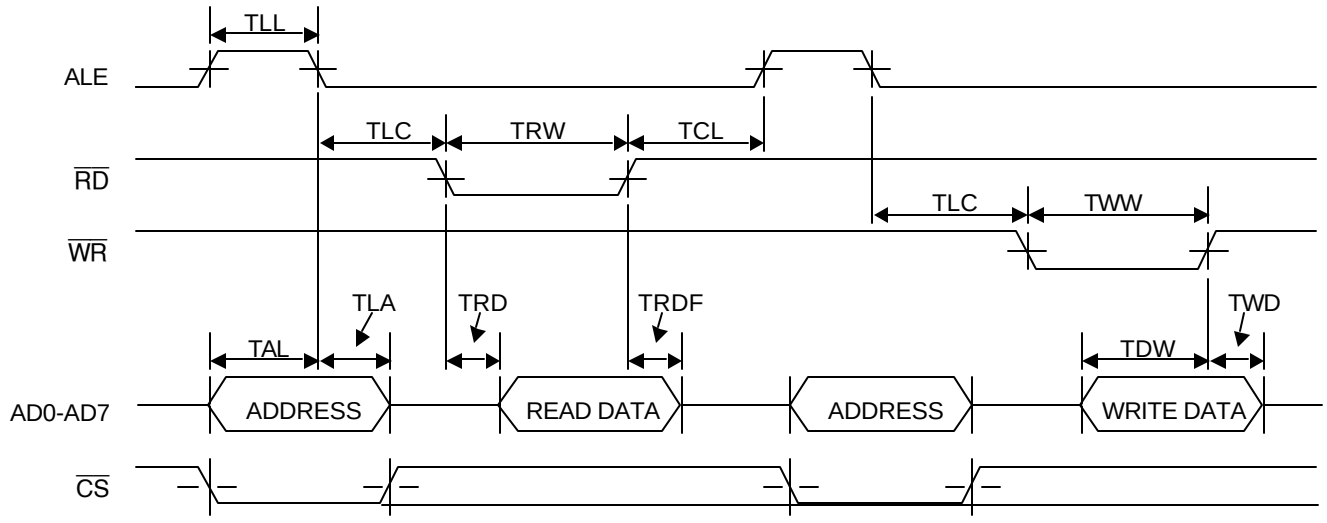
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step				
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time	-30 dBm0 to -70 dBm0 Step				
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA Enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms

DYNAMIC CHARACTERISTICS AND TIMING PARALLEL CONTROL INTERFACE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)						
TAL	$\overline{CS}$	$\overline{CS}$ setup before ALE Low	15			ns
	ADDR	ADDR hold after ALE Low	25			ns
TLA		$\overline{CS}$/ADDR hold after ALE Low	20			ns
TLC		ALE Low to $\overline{RD}$/$\overline{WR}$ Low	30			ns
TCL		$\overline{RD}$/$\overline{WR}$ Control to ALE High	-5			ns
TRD		Data out from $\overline{RD}$ Low			140	ns
TLL		ALE width	30			ns
TRDF		Data float after $\overline{RD}$ High			90	ns
TRW		$\overline{RD}$ width	200			ns
TWW		$\overline{WR}$ width	140			ns
TDW		Data setup before $\overline{WR}$ High	40			ns
TWD		Data hold after $\overline{WR}$ High	25			ns

NOTE: Asserting ALE, $\overline{CS}$, and $\overline{RD}$ or $\overline{WR}$ concurrently can cause unintentional register accesses. When using non-8031 compatible processors, care must be taken to prevent this from occurring when designing the interface logic.

BUS TIMING DIAGRAM (PARALLEL CONTROL MODE)

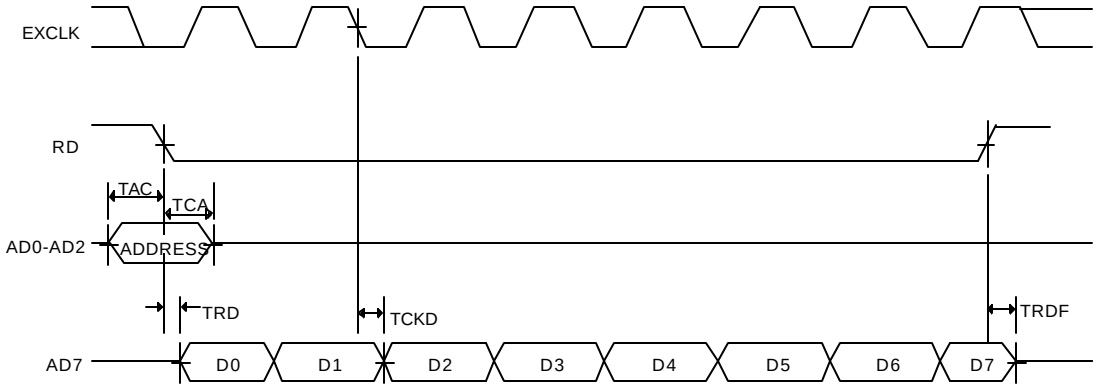


DYNAMIC CHARACTERISTICS AND TIMING SERIAL CONTROL INTERFACE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Timing (Refer to Timing Diagrams)					
TWW	$\overline{WR}$ width	140		25000	ns
TRD	Data out from $\overline{RD}$ Low			140	ns
TRDF	Data float after $\overline{RD}$ High			50	ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	200			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	85			ns

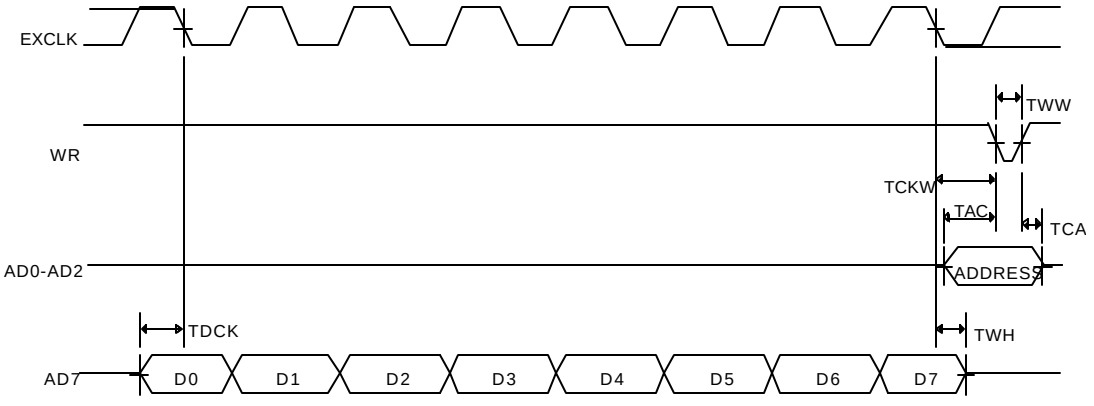
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

READ TIMING DIAGRAM (SERIAL CONTROL MODE)



Note: EXCLK must be low to read D0 after $\overline{RD}$ is asserted

WRITE TIMING DIAGRAM (SERIAL CONTROL MODE)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the Serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

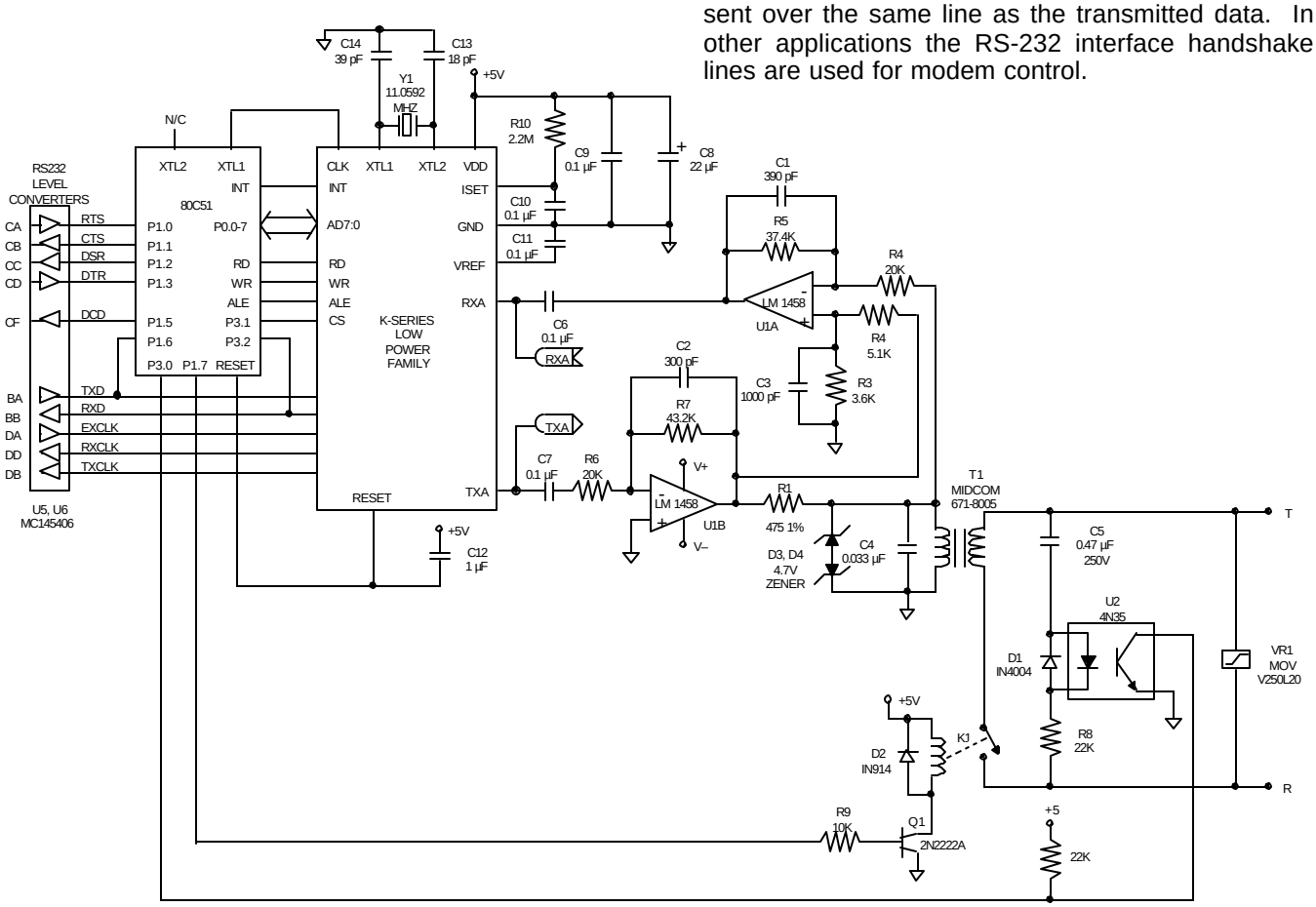


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the “hybrid” may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem’s detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal Common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply.

Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

TDK Semiconductor's 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

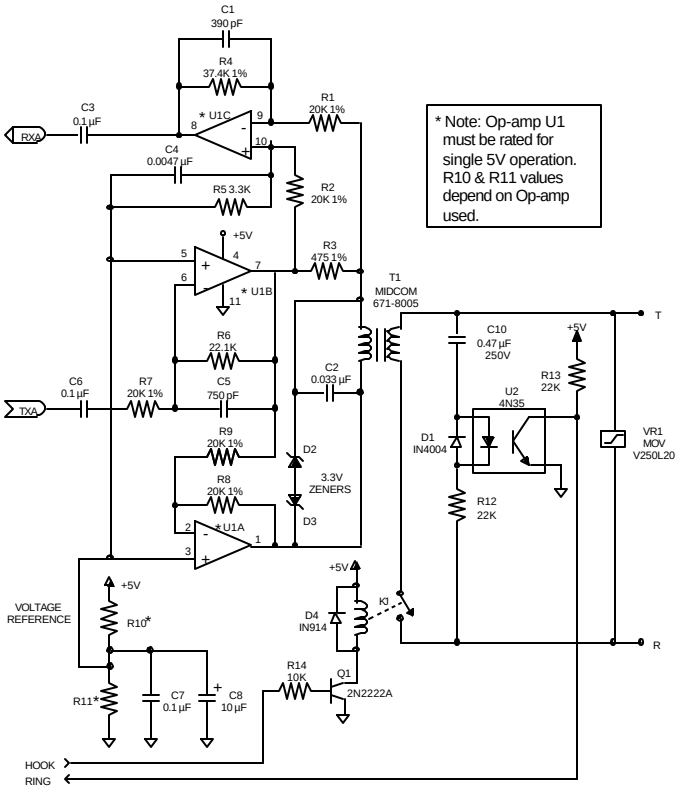


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a Parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a Parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

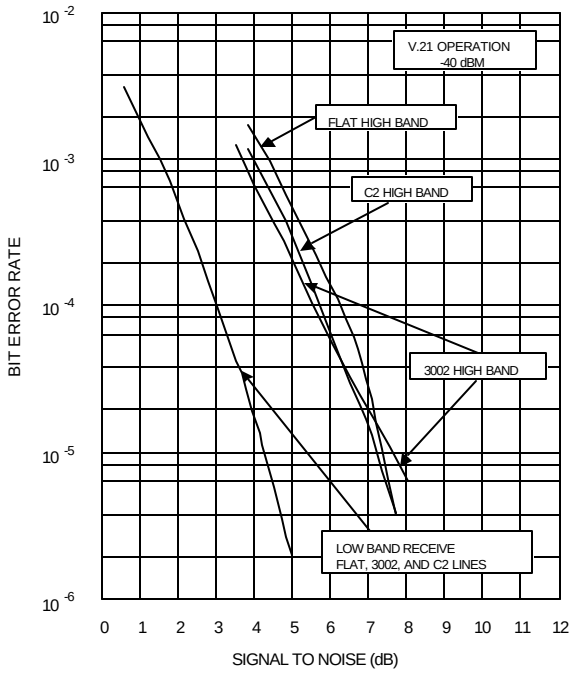
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

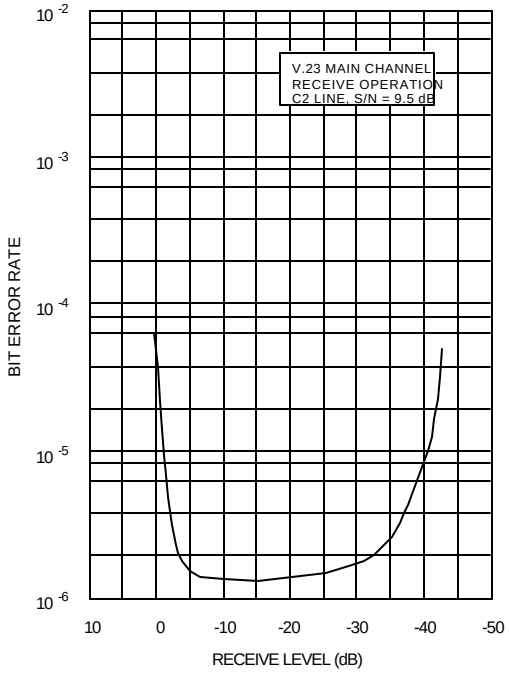
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

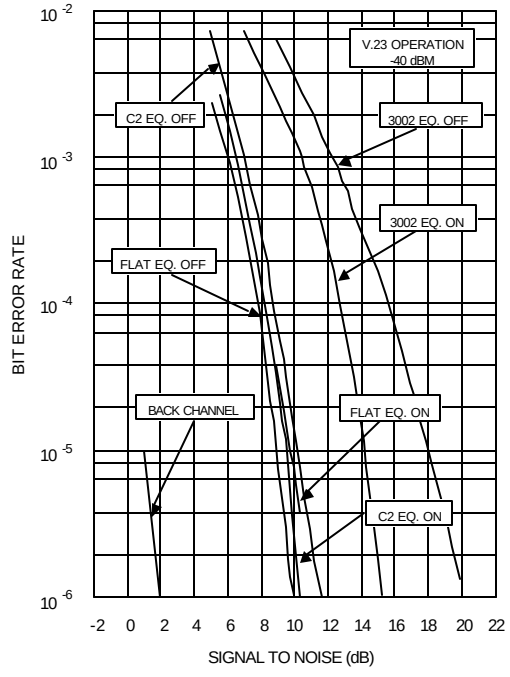
73K321L
BER vs SIGNAL TO NOISE



73K321L
BER vs RECEIVE LEVEL (V.23)



73K321L
BER vs S/N (V.23 ONLY)**

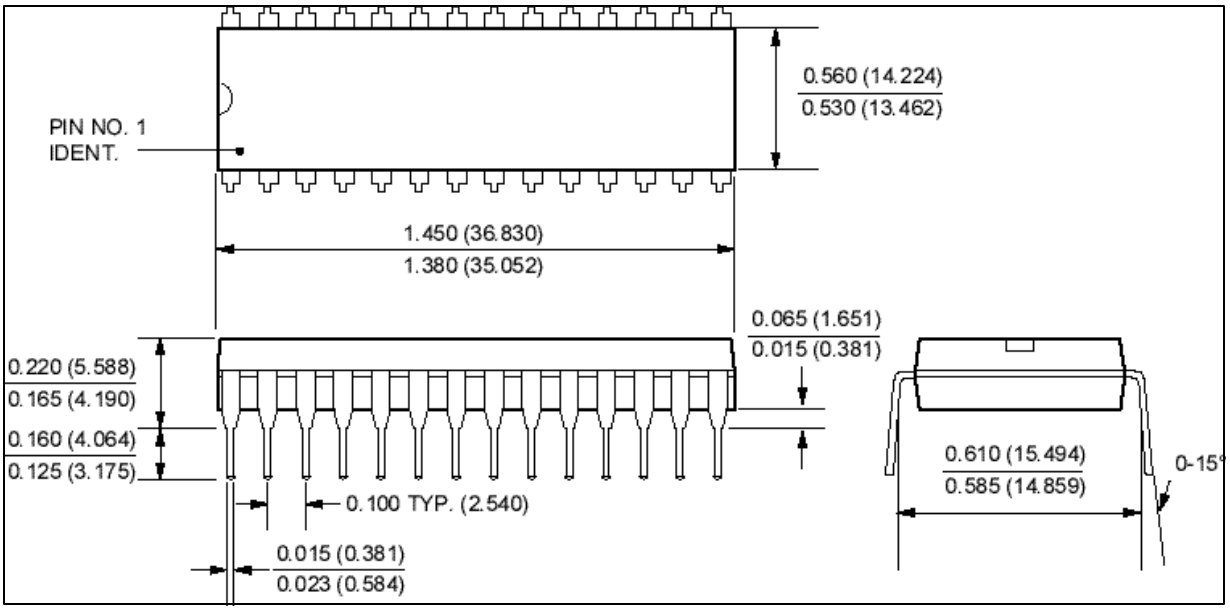


***** = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

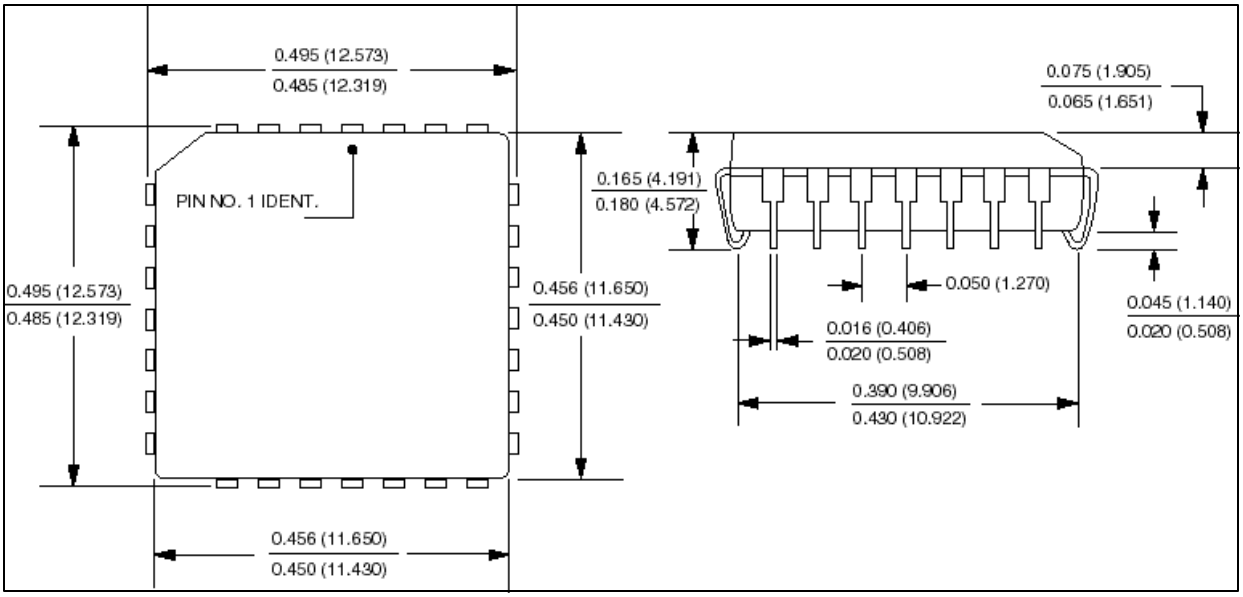
****** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

MECHANICAL SPECIFICATIONS

28-Pin DIP



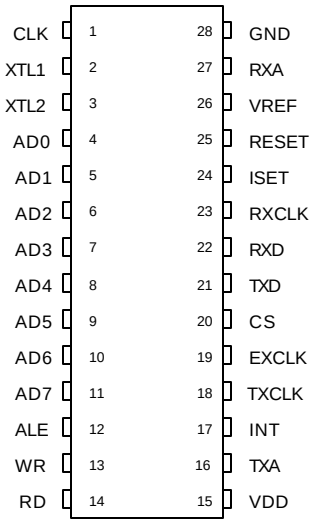
28-Pin PLCC



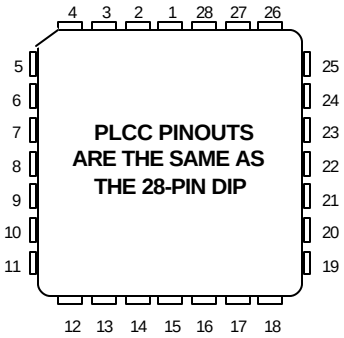
PACKAGE PIN DESIGNATIONS

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



600-Mil
28-Pin DIP
73K321L-IP



28-Pin
PLCC
73K321L-IH

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
73K321L		
28-Pin 5V Supply		
Plastic Dual-In-Line	73K321L-IP	73K321L-IP
Plastic Leaded Chip Carrier	73K321L-IH	73K321L-IH

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