LF2249
12 x 12-bit Digital Mixer

FEATURES

- 40 MHz Data and Computation Rate
- Two 12 x 12-bit Multipliers with Individual Data Inputs
- Separate 16-bit Input Port for Cascading Devices
- Independent, User-Selectable 1–16 Clock Pipeline Delay for Each Data Input
- User-Selectable Rounding of Products
- Fully Registered, Pipelined Architecture
- Three-State Outputs
- Fully TTL Compatible
- Replaces TRW / Raytheon / Fairchild TMC2249
- 120-pin PQFP

DESCRIPTION

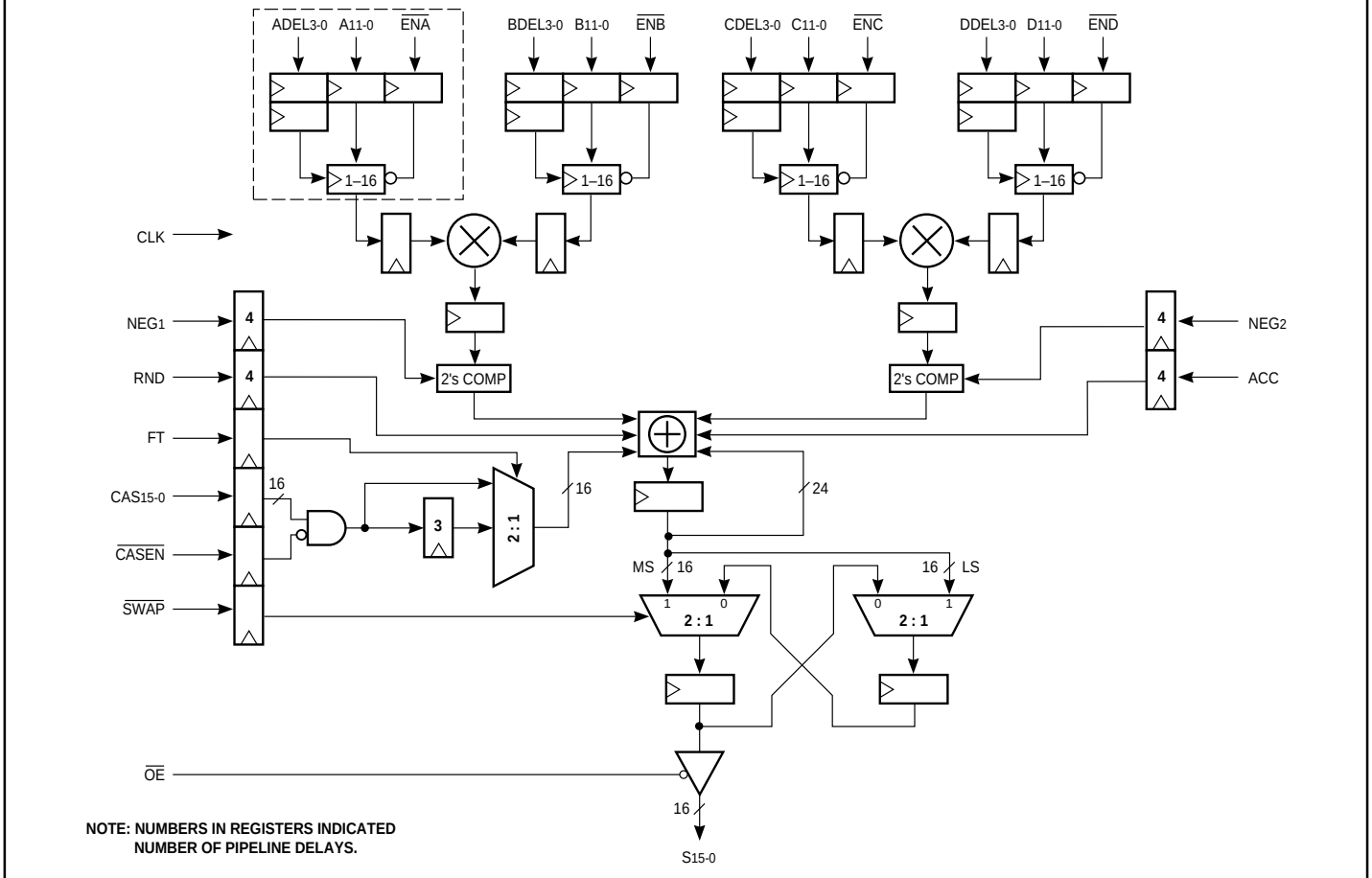
The **LF2249** is a high-speed digital mixer comprised of two 12-bit multipliers and a 24-bit accumulator. All multiplier inputs are user accessible, and each can be updated on every clock cycle. The LF2249 utilizes a pipelined architecture with fully registered inputs and outputs and an asynchronous three-state output enable control for optimum flexibility.

Independent input register clock enables allow the user to hold the data inputs over multiple clock cycles. Each multiplier input also includes a user-selectable 1-16 clock pipeline delay. The output of each multiplier can be independently negated under user control for subtraction of products. The sum of the products can also be internally rounded to 16 bits during the accumulation process.

A separate 16-bit input port connected to the accumulator is included to allow cascading of multiple LF2249s. Access to all 24 bits of the accumulator is gained by switching between upper or lower 16-bit words. The accumulated output data is updated on every clock cycle.

All inputs and outputs of the LF2249 are registered on the rising edge of clock, except for $\overline{OE}$. Internal pipeline registers for all data and control inputs are provided to maintain

LF2249 Block Diagram



synchronous operation between the incoming data and all available control functions. The LF2249 operates at a clock rate of 40 MHz over the full commercial temperature and supply voltage ranges.

Because of its flexibility, the LF2249 is ideally suited for applications such as image switching and mixing, digital quadrature mixing and modulating, FIR filtering, and arithmetic function and waveform synthesis.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A_{11-0}–D_{11-0} — Data Inputs

A_{11-0}–D_{11-0} are 12-bit data input registers. Data is latched into the input registers on the rising edge of CLK. The contents of the input registers are clocked into the top of the corresponding 16-stage pipeline delay (pushing the contents of the register stack down one register position) on the next clock cycle if the pipeline register stack is enabled. The LSBs are A_0-D_0 (Figure 1a).

CAS_{15-0} — Cascade Data Input

CAS_{15-0} is the 16-bit cascade data input port. Data is latched into the register on the rising edge of CLK. The LSB is CAS_0 (Figure 1a).

DETAILED VIEW OF BLOCK DIAGRAM OUTLINED AREA

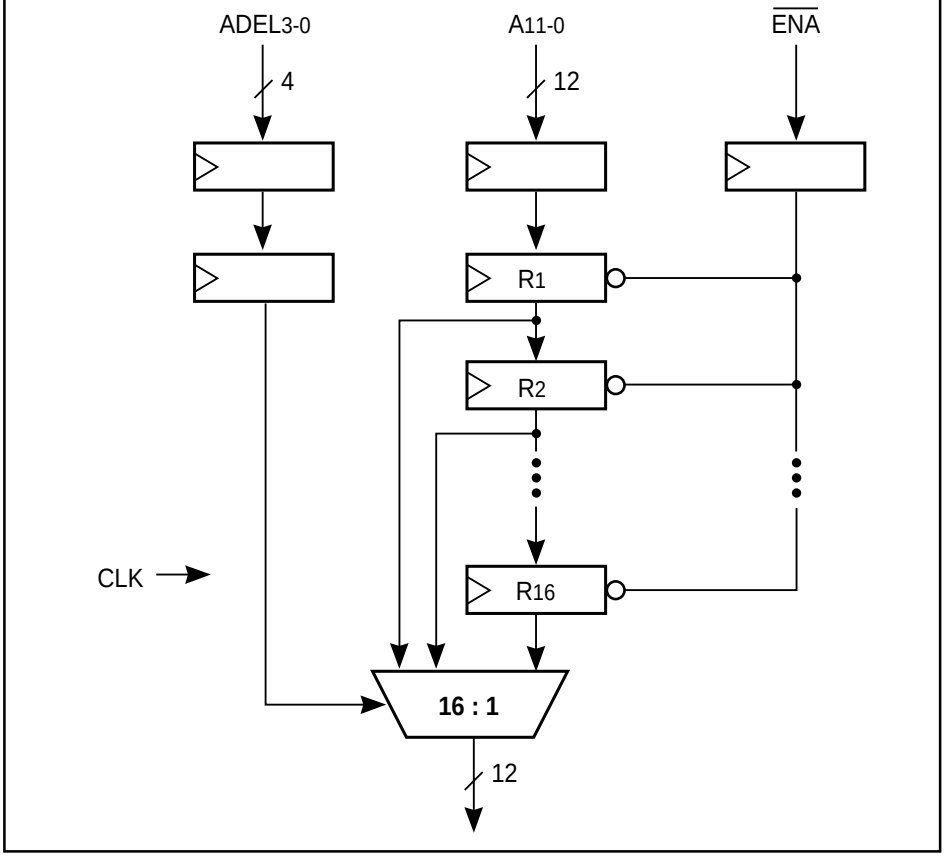


FIGURE 1A. INPUT FORMATS

Data Input

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
(Sign)											

Cascade Input

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
(Sign)															

FIGURE 1B. OUTPUT FORMATS

Sum Output (Upper 16 bits)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
(Sign)															

Sum Output (Lower 16 bits)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Outputs

S_{15-0} — Data Output

The current 16-bit result is available on the S_{15-0} outputs. The output data may be either the upper or lower 16 bits of the accumulator output, depending on the state of $\overline{SWAP}$. The LSB is S_0 (Figure 1b).

Controls

$\overline{ENA}$–$\overline{END}$ — Pipeline Register Enable

Input data in the N (N = A, B, C, or D) input register is latched into the corresponding pipeline register stack on each rising edge of CLK for which $\overline{EN_N}$ is LOW. Data already in the N register stack is pushed down one register position. When $\overline{EN_N}$ is HIGH, the data in the N pipeline register stack does not change, and the data in the N input register will not be stored in the register stack.

$ADEL_{3-0}$–$DDEL_{3-0}$ — Pipeline Delay Select

NDEL (N = A, B, C, or D) is the 4-bit registered pipeline delay select word. NDEL determines which stage of the N pipeline register stack is routed to the multiplier inputs. The minimum delay is one clock cycle (NDEL = 0000), and the maximum delay is 16 clock cycle (NDEL = 1111). Upon power up, the values of ADEL–DDEL and the contents of the pipeline register stacks are unknown and must be initialized by the user.

NEG_1–NEG_2 — Negate Control

The NEG_1 and NEG_2 controls determine whether a subtraction or accumulation of products is performed. When NEG_1 is HIGH, the product *A x B* is negated, causing the product to be subtracted from the accumulator contents. Likewise, when NEG_2 is HIGH, the product *C x D* is negated, causing the product to be subtracted as well. NEG_1 and NEG_2 determine the operation to be performed on the data input during the current clock cycle when ADEL–DDEL = 0000.

$\overline{CASEN}$ — Cascade Enable

When $\overline{CASEN}$ is LOW, data being input on the CAS_{15-0} inputs during that clock cycle will be registered and accumulated internally. When $\overline{CASEN}$ is HIGH, the CAS_{15-0} inputs are ignored.

FT — Feedthrough Control

When FT is LOW and ADEL–DDEL = 0000, data being input on the CAS_{15-0} inputs is delayed three clock cycles to align the data with the data being input on the A_{11-0}–D_{11-0} inputs. When FT is HIGH, the cascade data being input is routed around the three delay registers to simplify the cascading of multiple devices.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. When ACC is HIGH, the emerging products are added to the sum of the previous products.

RND — Rounding Control

When RND is HIGH, the sum of the products of the data being input on the current clock cycle will be rounded to 16 bits. To avoid the accumulation of roundoff errors, rounding is only performed during the first cycle of each accumulation process.

$\overline{SWAP}$ — Output Select

The $\overline{SWAP}$ control allows the user to access all 24 bits of the accumulator output by switching between upper and lower 16-bit words. When $\overline{SWAP}$ is HIGH, the upper 16 bits of the accumulator are always output. When $\overline{SWAP}$ is LOW, the lower 16 bits of the accumulator are output on every other clock cycle. As long as $\overline{SWAP}$ remains LOW, new output data will not be clocked into the output registers.

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output registers is available on the S_{15-0} pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**cc = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**cc = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	(Note 12)			±40	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			100	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			6	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

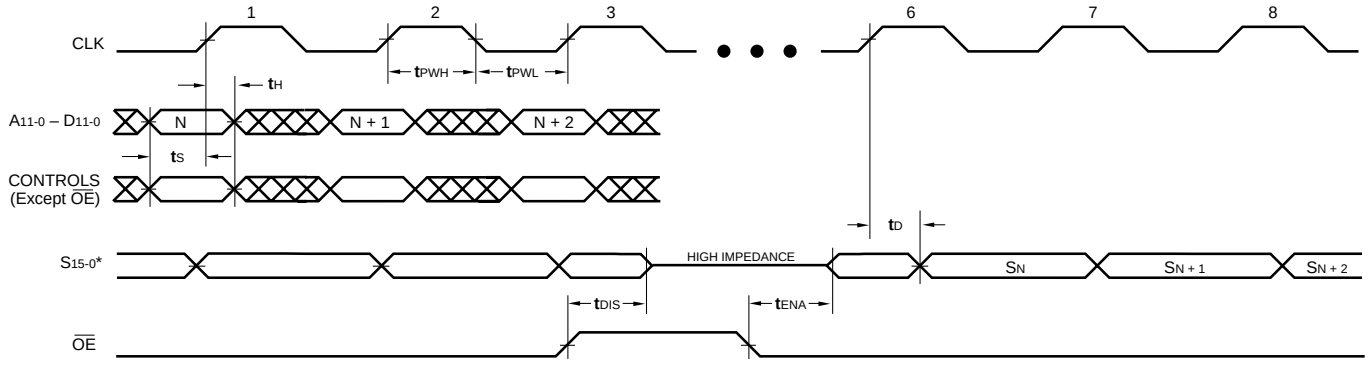
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2249-					
		40*		33		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		33		25	
t_{PWL}	Clock Pulse Width, LOW	15		15		10	
t_{PWH}	Clock Pulse Width, HIGH	10		10		10	
t_S	Input Setup Time	8		8		7	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		17		15		14
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2249-			
		40*		33*	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		33	
t_{PWL}	Clock Pulse Width, LOW	15		15	
t_{PWH}	Clock Pulse Width, HIGH	10		10	
t_S	Input Setup Time	8		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		17		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15

SWITCHING WAVEFORMS



*Assumes ADEL–DDEL = 0000

*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

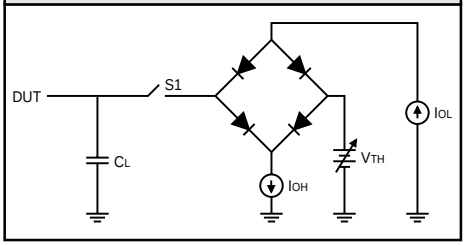
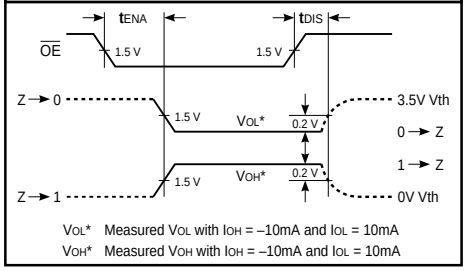
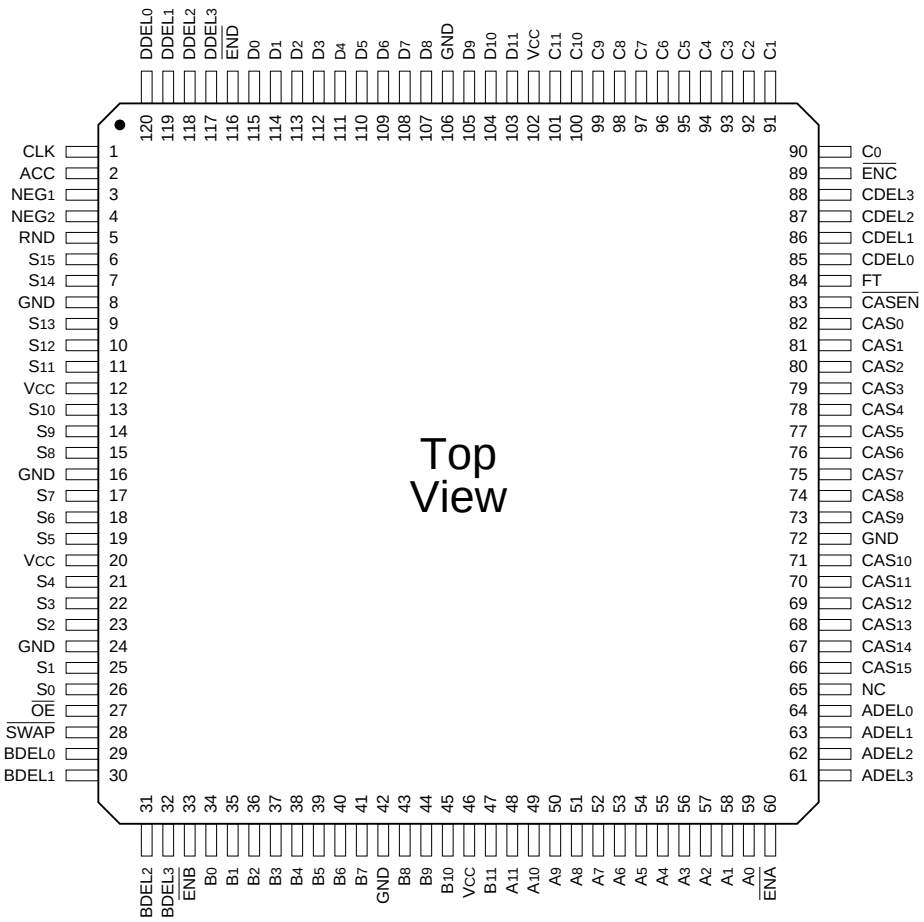


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

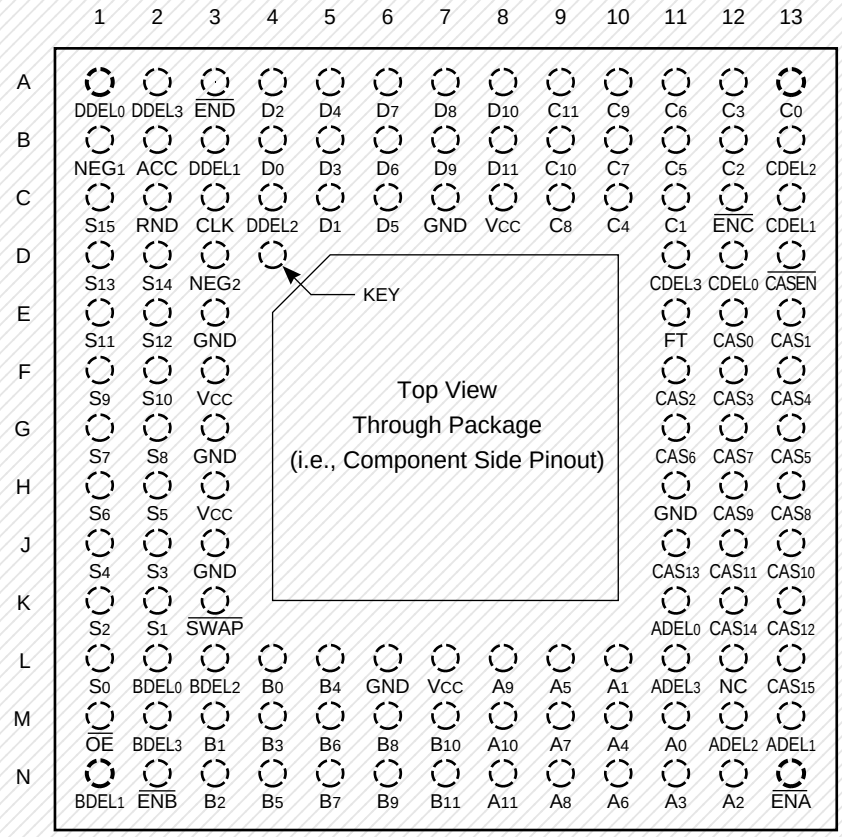
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2249QC33
25 ns	LF2249QC25
	–40°C to +85°C — COMMERCIAL SCREENING

ORDERING INFORMATION

120-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
	–55°C to +125°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT