Freescale Semiconductor
Advance Information

Document Number: MC33981
Rev. 6.0, 5/2007

Single High-Side Switch (4.0 mΩ), PWM clock up to 60kHz

The 33981 is a high-frequency, self-protected 4.0 mΩ $R_{DS(ON)}$ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications.

The 33981 can be controlled by Pulse-Width Modulation (PWM) with a frequency up to 60 kHz. It is designed for harsh environments, and it includes self-recovery features. The 33981 is suitable for loads with high in-rush current, as well as motors and all types of resistive and inductive loads.

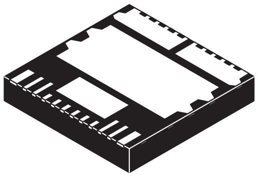
The 33981 is packaged in a 12 x 12 non-leaded power-enhanced Power QFN package with exposed tabs.

Features

- Single 4.0 mΩ $R_{DS(ON)}$ Maximum High-Side Switch
- PWM Capability up to 60 kHz with Duty Cycle from 5% to 100%
- Very Low Standby Current
- Slew Rate Control with External Capacitor
- Overcurrent and Overtemperature Protection, Undervoltage Shutdown and Fault Reporting
- Reverse Battery Protection
- Gate Drive Signal for External Low-Side N-Channel MOSFET with Protection Features
- Output Current Monitoring
- Temperature Feedback
- Pb-Free Packaging Designated by Suffix Code PNA

33981B

HIGH-SIDE SWITCH



Bottom View

PNA (Pb-Free Suffix)
98ARL10521D
16-PIN PQFN (12 X 12)

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33981BPNA/R2	-40°C to 125°C	16 PQFN

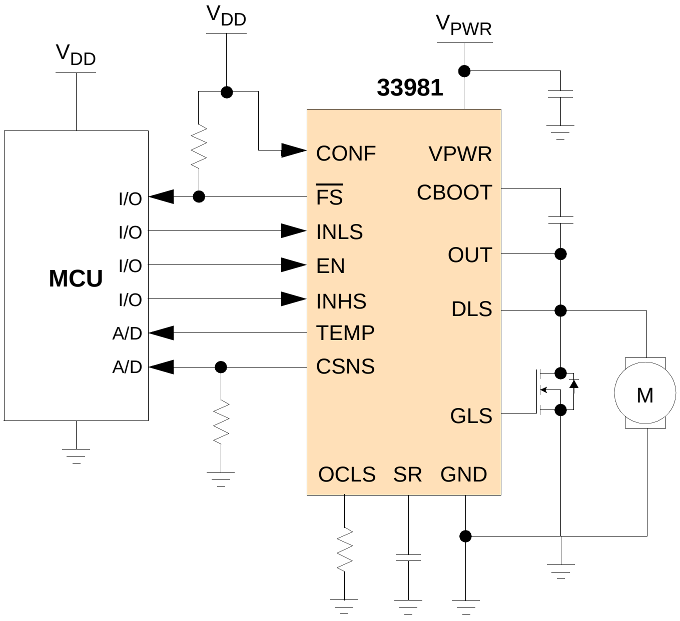


Figure 1. 33981 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

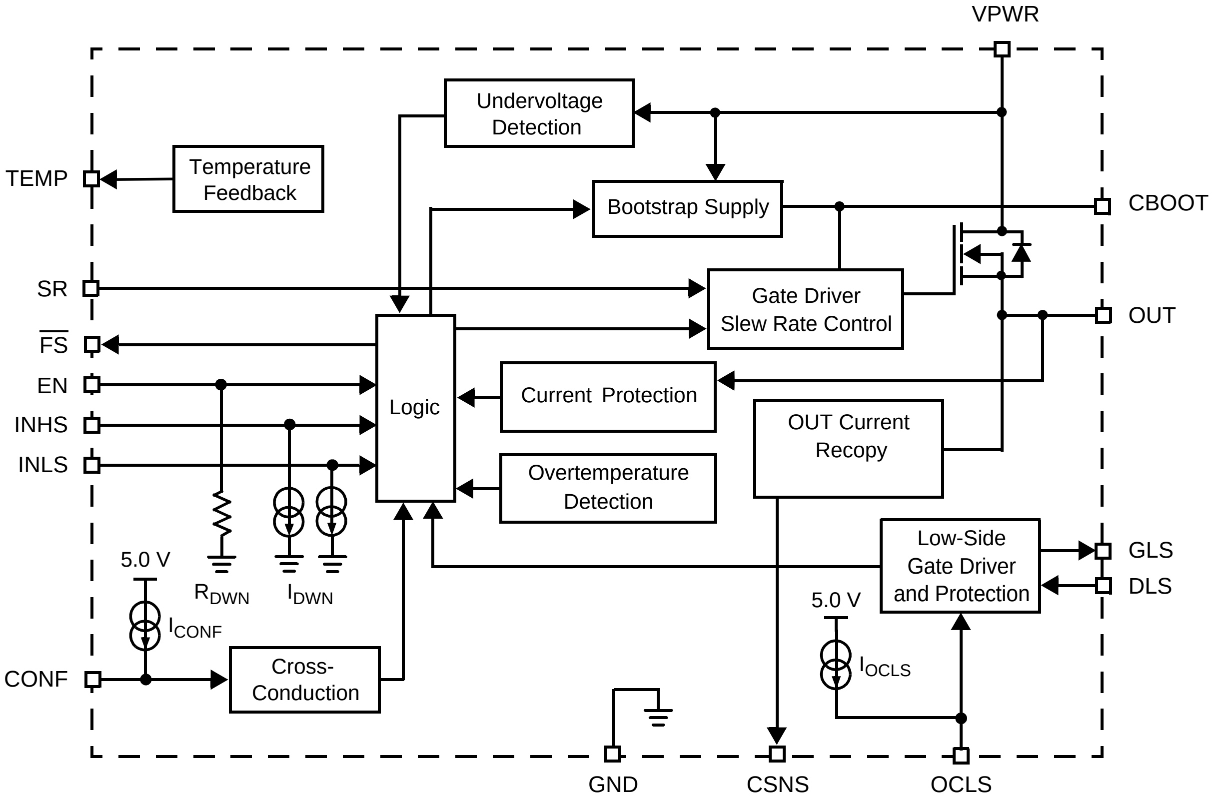


Figure 2. 33981 Simplified Internal Block Diagram

PIN CONNECTIONS

Package Transparent Top View

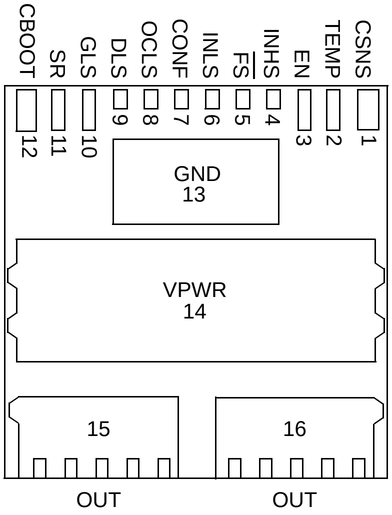


Figure 3. Pin Connections

Table 1. PIN DEFINITIONS

Descriptions of the pins listed in the table below can be found in the Functional Description section located on page 12.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	CSNS	Reports	Output Current Monitoring	This pin is used to generate a ground-referenced voltage for the microcontroller (MCU) to monitor output current.
2	TEMP	Reports	Temperature Feedback	This pin is used by the MCU to monitor board temperature.
3	$\overline{\text{EN}}$	Input	Enable (Active High)	This pin is used to place the device in a low-current sleep mode.
4	INHS	Input	Serial Input High Side	This input pin is used to control the output of the device.
5	$\overline{\text{FS}}$	Reports	Fault Status (Active Low)	This pin monitors fault conditions and is active LOW.
6	INLS	Input	Serial Input Low Side	This pin is used to control an external low-side N-channel MOSFET.
7	CONF	Input	Configuration Input	This input manages MOSFET N-channel cross-conduction.
8	OCLS	Input	Low-Side Overload	This pin sets the V_{DS} protection level of the external low-side MOSFET.
9	DLS	Input	Drain Low Side	This pin is the drain of the external low-side N-channel MOSFET.
10	GLS	Output	Low-Side Gate	This output pin drives the gate of the external low-side N-channel MOSFET.
11	SR	Input	Slew Rate Control	This pin controls the output slew rate.
12	CBOOT	Input	Bootstrap Capacitor	This pin provides the high-pulse current to drive the device.
13	GND	Ground	Ground	This is the ground pin of the device.
14	VPWR	Input	Positive Power Supply	This pin is the source input of operational power for the device.
15, 16	OUT	Output	Output	These pins provide a protected high-side power output to the load connected to the device.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage	V_{PWR}		V
Steady-State		-16 to 41	
Input/Output Pins Voltage (1)	INHS, INLS, CONF, CSNS, $\overline{FS}$, TEMP, EN	-0.3 to 7.0	V
Output Voltage	V_{OUT}		V
Positive		41.0	
Negative		-5.0	
Continuous Output Current (2)	I_{OUT}	40.0	A
CSNS Input Clamp Current	$I_{CL(CSNS)}$	15.0	mA
EN Input Clamp Current	$I_{CL(EN)}$	2.5	mA
SR Voltage	V_{SR}	-0.3 to 54.0	V
C_{BOOT} Voltage	C_{BOOT}	-0.3 to 54.0	V
OCLS Voltage	V_{OCLS}	-5.0 to 7.0	V
Low-Side Gate Voltage	V_{GLS}	-0.3 to 15.0	V
Low-Side Drain Voltage	V_{DLS}	-5.0 to 41.0	V
ESD Voltage (3)	V_{ESD}		V
Human Body Model (HBM)		±2000	
Charge Device Model (CDM)			
Corner Pins (1, 12, 15, 16)		±750	
All Other Pins (2-11, 13-14)		±500	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	TA	-40 to 125	
Junction	TJ	-40 to 150	
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance (4)			°C/W
Junction to Power Die Case	$R_{\theta JC}$	1.0	
Junction to Ambient	$R_{\theta JA}$	20.0	
Peak Pin Reflow Temperature During Solder Mounting (5)	T_{SOLDER}	245	°C

Notes

1. Exceeding voltage limits on INHS, INLS, CONF, CSNS, $\overline{FS}$, TEMP, and EN pins may cause a malfunction or permanent damage to the device.
2. Continuous high-side output rating as long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
4. Device mounted on a 2s2p test board per JEDEC JESD51-2.
5. pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VPWR)					
Battery Supply Voltage Range	V_{PWR}				V
Fully Operational		6.0	–	27.0	
Extended (6)		4.5	–	27.0	
V_{PWR} Supply Current INHS = 1 and OUT Open INLS = 0	$I_{PWR(ON)}$	–	10.0	12.0	mA
V_{PWR} Supply Current INHS = INLS = 0, EN = 5.0 V, OUT Connected to GND	$I_{PWR(SBY)}$	–	10.0	12.0	mA
Sleep State Supply Current (V_{PWR} < 14 V, EN = 0 V, OUT Connected to GND)	$I_{PWR(SLEEP)}$				µA
T_A = 25°C		–	–	5.0	
T_A = 125°C		–	–	50.0	
Undervoltage Shutdown	$V_{PWR(UV)}$	2.0	4.0	4.5	V
Undervoltage Hysteresis	$V_{PWR(UVHYS)}$	0.05	0.15	0.3	V
POWER OUTPUT (IOUT, VPWR)					
Output Drain-to-Source ON Resistance (I_{OUT} = 20 A, T_A = 25°C)	$R_{DS(ON)25}$				mΩ
V_{PWR} = 6.0 V		–	–	6.0	
V_{PWR} = 9.0 V		–	–	5.0	
V_{PWR} = 13.0 V		–	–	4.0	
Output Drain-to-Source ON Resistance (I_{OUT} = 20 A, T_A = 150°C)	$R_{DS(ON)150}$				mΩ
V_{PWR} = 6.0 V		–	–	10.2	
V_{PWR} = 9.0 V		–	–	8.5	
V_{PWR} = 13.0 V		–	–	6.8	
Output Source-to-Drain ON Resistance (I_{OUT} = -20 A, T_A = 25°C)(7) V_{PWR} = - 12 V	$R_{SD(ON)}$	–	–	8.0	mΩ
Output Overcurrent Detection Level 9.0 V < V_{PWR} < 16 V	I_{OCH}	75	100	125	A
Current Sense Ratio 9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V	C_{SR}	–	1/20000	–	–
Current Sense Ratio (C_{SR}) Accuracy 9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V Output Current	C_{SR_ACC}				%
5.0 A		-20	–	20	
15 A, 20 A and 30 A		-15	–	15	
Current Sense Voltage Clamp I_{CSNS} = 15 mA	$V_{CL(CSNS)}$	4.5	6.0	7.0	V

Notes

6. OUT can be commanded fully on, PWM is available at room. Low Side Gate driver is available. Protections and Diagnosis are not available. Min/max parameters are not guaranteed.
7. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (VPWR) (continued)					
Overtemperature Shutdown	T_{SD}	160	175	190	°C
Overtemperature Shutdown Hysteresis (8)	T_{SDHYS}	5.0	–	20	°C
LOW SIDE GATE DRIVER (VPWR, VGLS, VOCLS)					
Low-Side Gate Voltage	V_{GLS}				V
V_{PWR} = 6.0 V		5.0	5.4	6.0	
V_{PWR} = 9.0 V		8.0	8.4	9.0	
V_{PWR} = 13 V		12.0	12.4	13.0	
V_{PWR} = 27 V		12.0	12.4	13.0	
Low-Side Gate Sinked Current V_{GLS} = 2 V, V_{PWR} = 13 V	I_{GLSNEG}	–	100	–	mA
Low-Side Gate Sourced Current V_{GLS} = 2 V, V_{PWR} = 13 V	I_{GLSPOS}	–	100	–	mA
Low-Side Overload Detection Level versus Low-Side Drain Voltage V_{OCLS} - V_{DLS}, (V_{OCLS} ≤ 4.0 ς)	V_{DS_LS}	-50	–	+50	mV
CONTROL INTERFACE (CONF, INHS, INLS, EN, OCLS)					
Input Logic High Voltage (CONF, INHS, INLS)	V_{IH}	3.3	–	–	V
Input Logic Low Voltage (CONF, INHS, INLS)	V_{IL}	–	–	1.0	V
Input Logic Voltage Hysteresis (CONF, INHS, INLS)	V_{INHYS}	100	600	1200	mV
Input Logic Active Pulldown Current (INHS, INLS)	I_{DWN}	5.0	10	20	µA
Enable Pull-down Resistor ($\overline{EN}$)	R_{DWN}	100	200	400	kΩ
Enable Voltage Threshold ($\overline{EN}$)	V_{EN}		2.5		V
Input Clamp Voltage ($\overline{EN}$) I_{EN} < 2.5 mA	V_{CLEN}	7.0	–	14	V
Input Forward Voltage ($\overline{EN}$)	$V_{F(EN)}$	-2.0	–	-0.3	V
Input Active Pullup Current ($\overline{OCLS}$)	I_{OCLSp}	50	100	200	µA
Input Active Pullup Current (CONF)	I_{CONF}	5.0	10	20	µA
$\overline{FS}$ Tri-State Capacitance (8)	C_{FS}	–	–	20	pF
$\overline{FS}$ Low-State Output Voltage $I_{\overline{FS}}$ = -1.6 mA	V_{FSL}	–	0.2	0.4	V
Temperature Feedback T_A = 25°C for V_{PWR} = 14 V	V_{TFEED}	3.35	3.45	3.55	V
Temperature Feedback Derating (8)	DT_{FEED}	-8.5	-8.9	-9.3	mV/°C

Notes

8. Parameter is guaranteed by process monitoring but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE AND POWER OUTPUT TIMING (CBOOT, VPWR)					
Charge Blanking Time (CBOOT) (10)	t_{ON}	10	25	50	µs
Output Rising Slew Rate V_{PWR} = 13 V, from 10% to 90% of $V_{OUT,}$ SR Capacitor = 4.7 nF, R_L= 5.0 Ω	SR_R	8.0	16	35	V/µs
Output Falling Slew Rate V_{PWR} = 13 V, from 90% to 10% of $V_{OUT,}$ SR Capacitor = 4.7 nF, R_L= 5.0 Ω	SR_F	8.0	16	35	V/µs
Output Turn-ON Delay Time (11) V_{PWR} = 13 V, SR Capacitor = 4.7 nF	t_{DLYON}	200	400	700	ns
Output Turn-OFF Delay Time (12) V_{PWR} = 13 V, SR Capacitor = 4.7 nF	t_{DLYOFF}	500	1000	1500	ns
Input Switching Frequency (9)	f_{PWM}	–	20	60	kHz
Output PWM ratio @ 60kHz (13)	R_{PWM}	5.0		95	%
Time to Reset Fault Diagnosis (over load on high side or external low side)	$t_{RSTDIAG}$	100	200	400	µs
Output Over Current Detection Time	t_{OCH}	1.0	10	20	µs

Notes

9. The MC33981 can work down (~100Hz). The fault management reset can not be guaranteed with PWM frequency lower than 5kHz (INHS=0 during 200us typ)
10. Values for CBOOT=100nF. Refer to the paragraph entitled Sleep Mode on page 13. Parameter is guaranteed by design and not production tested.
11. Turn-ON delay time measured from rising edge of INHS that turns the output ON to V_{OUT} = 0.5 V with R_L= 5.0 Ω resistive load.
12. Turn-OFF delay time measured from falling edge of INHS that turns the output OFF to V_{OUT} = V_{PWR} -0.5 V with R_L= 5.0 Ω resistive load.
13. The ratio is measured at V_{out} = 50% V_{PWR} without SR capacitor. The device is capable of 100% duty cycle.

TIMING DIAGRAMS

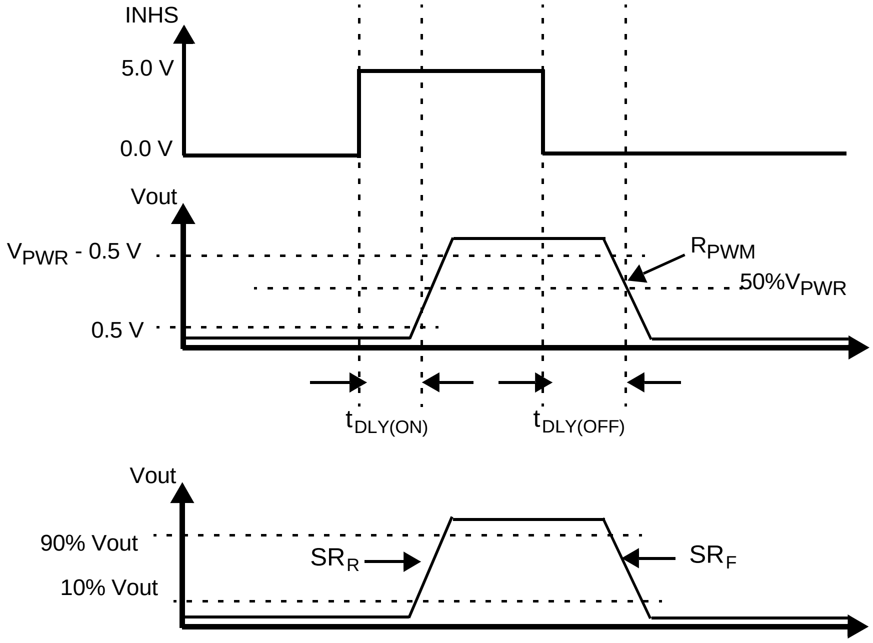


Figure 4. Time Delays Functional Diagrams

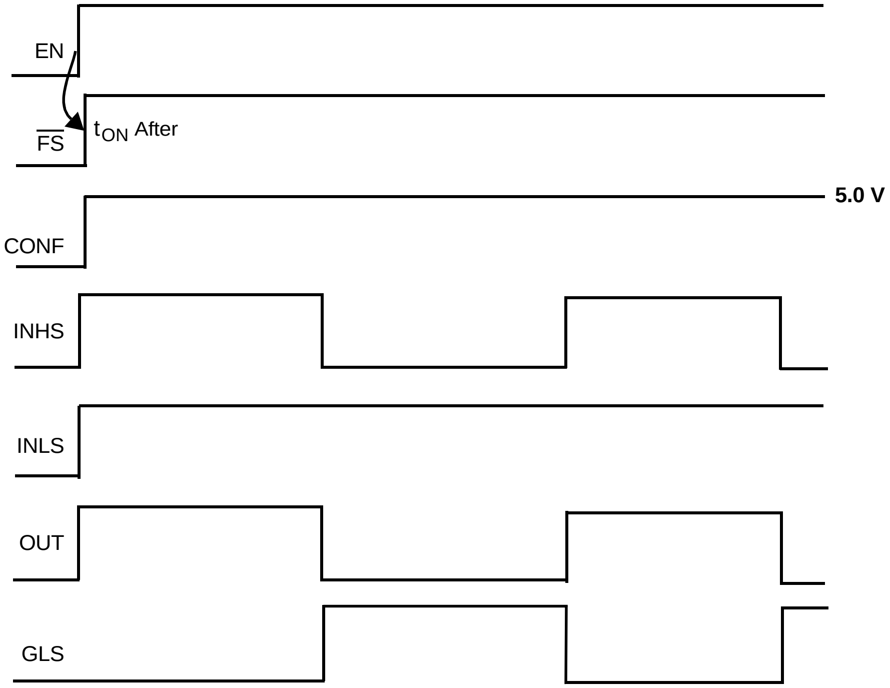


Figure 5. Normal Mode, Cross-Conduction Management

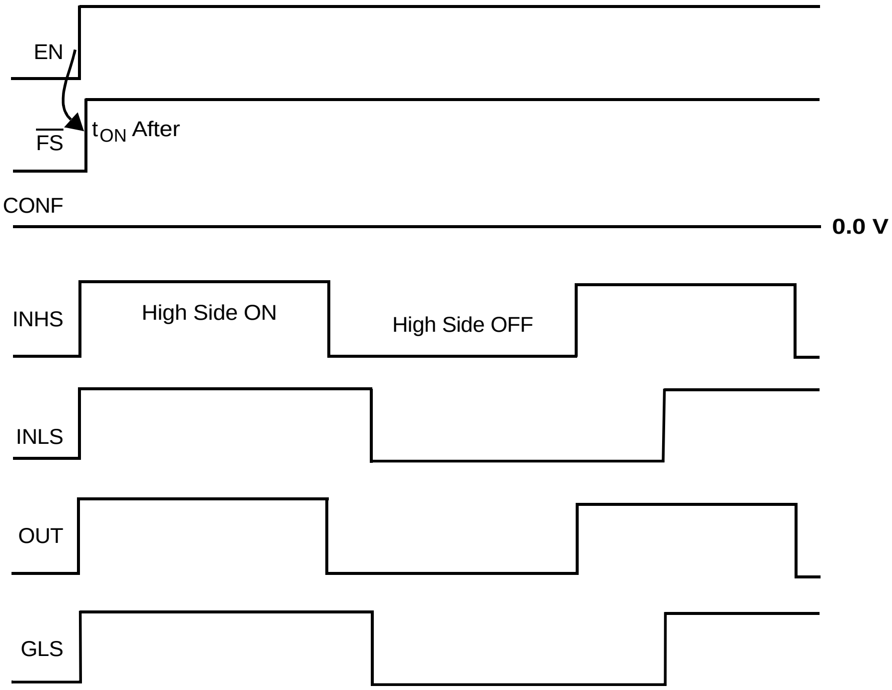


Figure 6. Normal Mode, Independent High Side and Low Side

ELECTRICAL PERFORMANCE CURVES

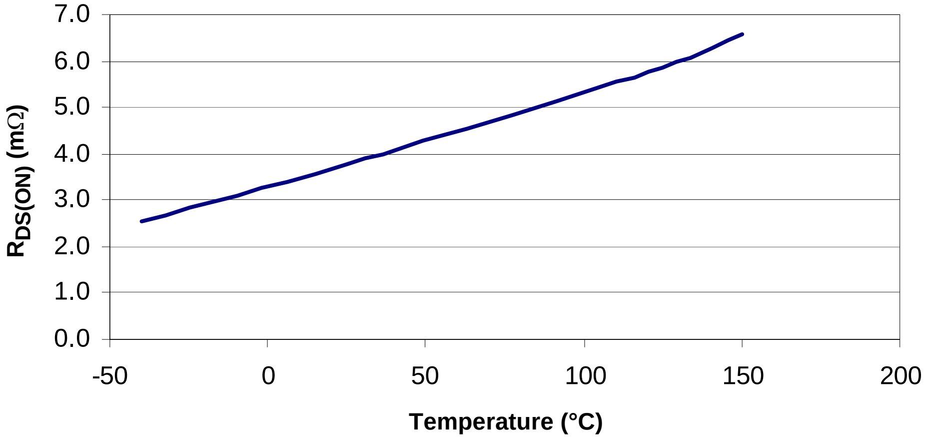


Figure 7. Typical $R_{DS(ON)}$ vs. Temperature at V_{PWR} = 13 V

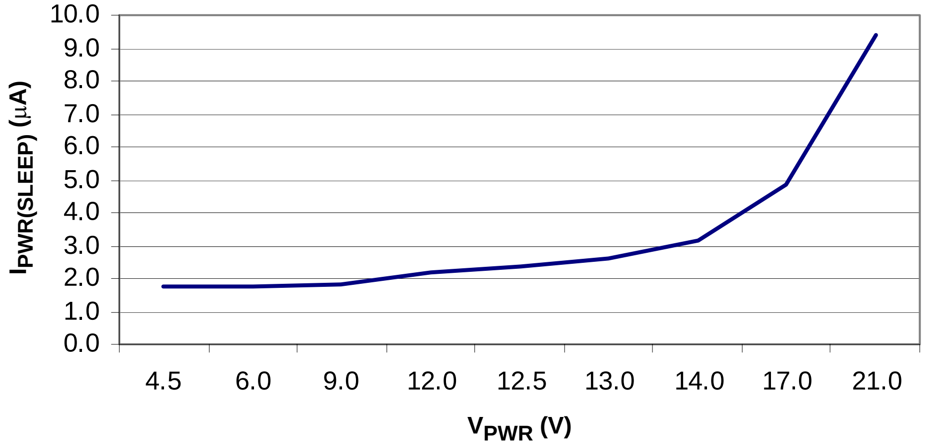


Figure 8. Typical Sleep State Supply Current vs. V_{PWR} at 150°C

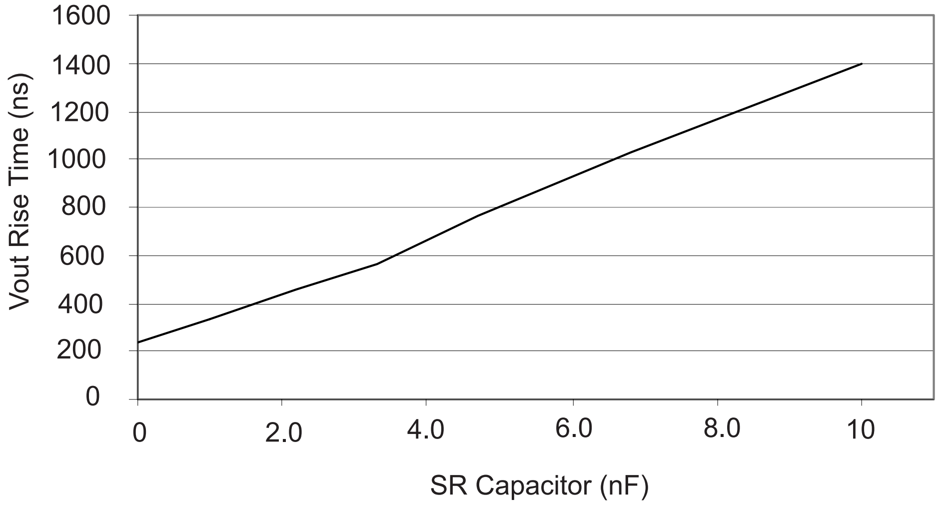


Figure 9. V_{OUT} Rise Time vs. SR Capacitor From 10% to 90% of V_{OUT} at 25°C and V_{PWR} = 13 V

ELECTRICAL PERFORMANCE CURVES

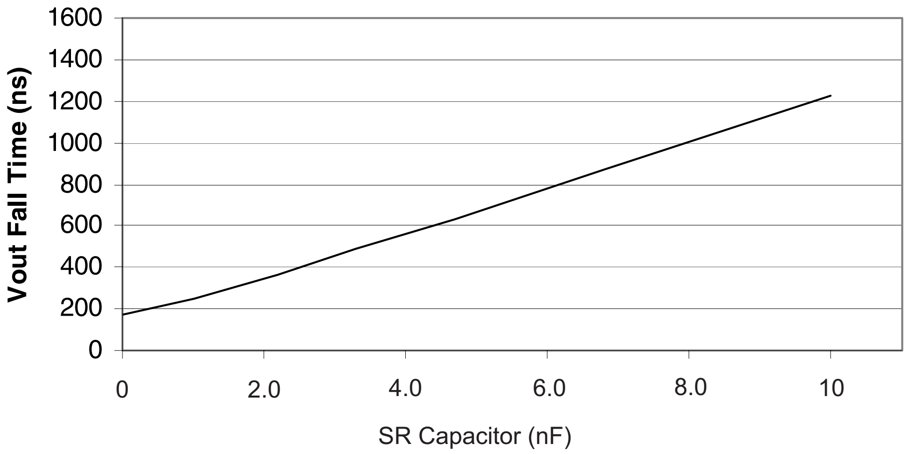


Figure 10. V_{OUT} Fall Time vs. SR Capacitor From 10% to 90% of V_{OUT} at 25°C and V_{PWR} = 13 V

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33981 is a high-frequency self-protected silicon 4.0 mΩ $R_{DS(ON)}$ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33981 can be controlled by pulse-width modulation (PWM) with a frequency up to 60 kHz. It is designed for harsh environments, and it includes self-recovery features.

The 33981 is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads. A dedicated parallel input is available for an external low-side control with protection features and cross-conduction management.

FUNCTIONAL PIN DESCRIPTIONS

OUTPUT CURRENT MONITORING (CSNS)

This pin is used to output a current proportional to the high-side OUT current and is used externally to generate a ground-referenced voltage for the microcontroller (MCU) to monitor OUT current.

TEMPERATURE FEEDBACK (TEMP)

This pin reports an analog value proportional to the temperature of the GND flag (pin 13). It is used by the MCU to monitor board temperature.

ENABLE [ACTIVE HIGH] (EN)

This is an input used to place the device in a low current sleep mode. This pin has an active passive internal pulldown.

INPUT HIGH SIDE (INHS)

The input pin is used to directly control the OUT. This input has an active internal pulldown current source and requires CMOS logic levels.

FAULT STATUS ($\overline{FS}$)

This pin is an open drain-configured output requiring an external pullup resistor to V_{DD} (5.0 V) for fault reporting. When a device fault condition is detected, this pin is active LOW.

INPUT LOW SIDE (INLS)

This input pin is used to directly control an external low-side N-channel MOSFET and has an active internal pulldown current source and requires CMOS logic levels. It can be controlled independently of the INHS depending of CONF pin.

CONFIGURATION INPUT (CONF)

This input pin is used to manage the cross-conduction between the internal high-side N-channel MOSFET and the external low-side N-channel MOSFET. The pin has an active internal pullup current source. When CONF is at 0 V, the two MOSFETs are controlled independently. When CONF is at V_{DD} 5.0 V, the two MOSFETs cannot be on at the same time.

LOW-SIDE OVERLOAD ($\overline{OCLS}$)

This pin sets the V_{DS} protection level of the external low-side MOSFET. This pin has an active internal pullup current source. It must be connected to an external resistor.

DRAIN LOW SIDE (DLS)

This pin is the drain of the external low-side N-channel MOSFET. Its monitoring allows protection features: low side short protection and V_{PWR} short protection.

LOW-SIDE GATE (GLS)

This pin is an output used to drive the gate of the external low-side N-channel MOSFET.

SLEW RATE CONTROL (SR)

A capacitor connected between this pin and ground is used to control the output slew rate.

BOOTSTRAP CAPACITOR (CBOOT)

A capacitor connected between this pin and OUT is used to switch the OUT in PWM mode.

GROUND (GND)

This pin is the ground for the logic and analog circuitry of the device.

POSITIVE POWER SUPPLY (VPWR)

This pin connects to the positive power supply and is the source input of operational power for the device. The V_{PWR} pin is a backside surface mount tab of the package.

OUTPUT (OUT)

Protected high-side power output to the load. Output pins must be connected in parallel for operation.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

The 33981 has 2 operating modes: Sleep and Normal depending on EN input.

SLEEP MODE

Sleep mode is the state of the 33981 when the EN is logic [0]. In this mode, OUT, the gate driver for the external MOSFET, and all unused internal circuitry are off to minimize current draw.

NORMAL MODE

The 33981 will go to the normal operating mode when the EN pin is logic [1]. The INHS and INLS commands will be disabled t_{ON} after the EN transitions to logic [1] to enable the charge of the bootstrap capacitor.

Table 5. Operating Modes

Condition	CONF	$\overline{\text{INHS}}$	$\overline{\text{INLS}}$	OUT	GLS	$\overline{\text{FS}}$	EN	Comments
Sleep	x	x	x	x	x	H	L	Device is in Sleep mode. The OUT and low-side gate are OFF.
Normal	L	H	H	H	H	H	H	Normal mode. High side and low side are controlled independently. The high side and the low side are both on.
Normal	L	L	L	L	L	H	H	Normal mode. High side and low side are controlled independently. The high side and the low side are both off.
Normal	L	L	H	L	H	H	H	Normal mode. Half-bridge configuration. The high side is off and the low side is on.
Normal	L	H	L	H	L	H	H	Normal mode. Half-bridge configuration. The high side is on and the low side is off.
Normal	H	PWM	H	PWM	PWM_bar	H	H	Normal mode. Cross-conduction management is activated. Half-bridge configuration.

H = High level
L = Low level
x = Don't care
PWM_bar = Opposite of pulse-width modulation signal.

PROTECTION AND DIAGNOSTIC FEATURES

UNDERVOLTAGE

The 33981 incorporates undervoltage protection. In case of $V_{PWR}<V_{PWR(UV)}$, the OUT is switched OFF until the power supply rises to $V_{PWR(UV)}+V_{PWR(UVHYS)}$. The latched fault are reset below $V_{PWR(UV)}$.

OVERTEMPERATURE FAULT

The 33981 incorporates over temperature detection and shutdown circuitry on OUT. Overtemperature detection also protects the low-side gate driver (GLS pin). Overtemperature detection occurs when OUT is in the ON or OFF state and GLS is at high or low level.

For OUT, an over temperature fault condition results in OUT turning OFF until the temperature falls below T_{SD}. This cycle will continue indefinitely until the offending load is removed. Figure 12, page 16 and Figure 18, page 20 show an over temperature on OUT.

An over temperature fault on the low-side gate drive results in OUT turning OFF and the GLS going to 0 V until the temperature falls below T_{SD}. This cycle will continue until the offending load is removed. $\overline{\text{FS}}$ pin transition to logic [1] will be disabled typically t_{ON} after to enable the charge of the bootstrap capacitor.

Overtemperature faults force the TEMP pin to 0 V.

OVERCURRENT FAULT ON HIGH SIDE

The OUT pin has an overcurrent high-detection level called I_{OCH} for maximum device protection. If at any time the current reaches this level, OUT will stay OFF and the CSNS pin will go to 0 V. The OUT pin is reset (and the fault is delatched) by a logic [0] at the INHS pin for at least $t_{RST(diag)}$. When INHS goes to 0 V, CSNS goes to 5.0 V.

In Figure 16, page 19, the OUT pin is short-circuited to 0 V. When the current reaches I_{OCH}, OUT is turned OFF within t_{OCH} owing to internal logic circuit.

OVERLOAD FAULT ON LOW SIDE

This fault detection is active when INLS is logic [1]. Low-side overload protection does not measure the current directly but rather its effects on the low-side MOSFET. When

$V_{DLS} > V_{OCLS}$, the GLS pin goes to 0 V and the OCLS internal current source is disconnected and OCLS goes to 0 V. The GLS pin and the OCLS pin are reset (and the fault is delatched) by a logic [0] at the INLS pin for at least $t_{RST(diag)}$. Figure 13, page 17 and Figure 14, page 18 illustrate the behavior in case of overload on Low Side Gate driver.

When connected to an external resistor, the OCLS pin with its internal current source sets the V_{OCLS} level. By changing the external resistance, the protection level can be adjusted depending on low-side characteristics. A 33kΩ resistor gives a V_{DS} level of 3.3 V typical.

This protection circuitry measures the voltage between the drain of the low side (DLS pin) and the 33981 ground (GND pin). For this reason it is key that the low-side source, the 33981 ground, and the external resistance ground connection are connected together in order to prevent false error detection due to ground shifts.

The maximum OCLS voltage being 4.0V, a resistor bridge on DLS must be used to detect a higher voltage across the low side.

CONFIGURATION

The CONF pin manages the cross-conduction between the internal MOSFET and the external low-side MOSFET. With the CONF pin at 0 V, the two MOSFETs can be independently controlled. A load can be placed between the high side and the low side.

With the CONF pin at 5.0 V, the two MOSFETs cannot be on at the same time. They are in half-bridge configuration as shown in the simplified application diagram on page 1. If INHS and INLS are at 5.0 V at the same time, INHS has priority and OUT will be at V_{PWR}. If INHS changes from 5.0 V to 0 V with INLS at 5.0 V, GLS will go to high state as soon as the V_{GS} of the internal MOSFET is lower than 2.0 V typically. A half-bridge application could consist in sending PWM signal to the INHS pin and 5.0 V to the INLS pin with the CONF pin at 5.0 V.

Figure 20, page 22, illustrates the simplified application diagram on page 1 with a DC motor and external low side. The CONF and INLS pins are at 5.0 V. When INHS is at 5.0 V, current is flowing in the motor. When INHS goes to 0 V, the load current recirculates in the external low side.

BOOTSTRAP SUPPLY

Bootstrap supply provides current to charge the bootstrap capacitor through the V_{PWR} pin. A short time is required after the application of power to the device to charge the bootstrap capacitor. A typical value for this capacitor is 100 nF. An internal charge pump allows continuous MOSFET drive. When the device is in the sleep mode, this bootstrap supply is off to minimize current consumption.

HIGH-SIDE GATE DRIVER

The high-side gate driver switches the bootstrap capacitor voltage to the gate of the MOSFET. The driver circuit has a low-impedance drive to ensure that the MOSFET remains OFF in the presence of fast falling dV/dt transients on the OUT pin.

This bootstrap capacitor connected between the power supply and the C_{BOOT} pin provides the high pulse current to drive the device. The voltage across this capacitor is limited to about 13 V typical.

An external capacitor connected between pins SR and GND is used to control the slew rate at the OUT pin. Figure 9, page 10 and Figure 10, page 11 give Vout rise and fall time versus different SR capacitors.

LOW-SIDE GATE DRIVER

The low-side control circuitry is PWM capable. It can drive a standard MOSFET with an $R_{DS(ON)}$ as low as 10.0 mΩ at a frequency up to 60 kHz. The V_{GS} is internally clamped at 12 V typically to protect the gate of the MOSFET. The GLS pin is protected against short by a local over temperature sensor.

THERMAL FEEDBACK

The 33981 has an analog feedback output (TEMP pin) that provides a value in inverse proportion to the temperature of the GND flag (pin 13). The controlling microcontroller can “read” the temperature proportional voltage with its analog-to- digital converter (ADC). This can be used to provide real-time monitoring of the PC board temperature to optimize the motor speed and to protect the whole electronic system. TEMP pin value is VTFEED with a negative temperature coefficient of DT_{FEED}.

REVERSE BATTERY

The 33981 survives the application of reverse battery voltage as low as -16 V. Under these conditions, the output’s gate is enhanced to decrease device power dissipation. No additional passive components are required. The 33981 survives these conditions until the maximum junction rating is reached.

In the case of reverse battery in a half-bridge application, a direct current passes through the external freewheeling diode and the internal high-side.

As Figure 11 shows, it is essential to protect this power line. The proposed solution is an external N-channel low-side with its gate tied to battery voltage through a resistor. A high-side in the V_{PWR} line could be another solution.

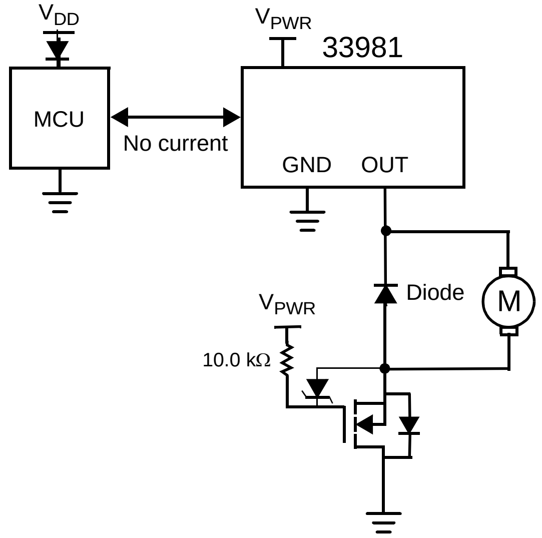


Figure 11. Reverse Battery Protection

GROUND (GND) DISCONNECT PROTECTION

If the DC motor module ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless of the output state at the time of disconnection. A 10k resistor needs to be added between the EN pin and the rest of the circuitry in order to ensure the device turns off in case of ground disconnect and to prevent exceeding this pin's maximum ratings.

FAULT REPORTING

This 33981 indicates the faults below as they occur by driving the $\overline{\text{FS}}$ pin to logic [0]:

- Overtemperature fault
- Overcurrent fault on OUT
- Overload fault on the external low-side MOSFET

The $\overline{\text{FS}}$ pin will return to logic [1] when the over temperature fault condition is removed. The two other faults are latched.

Table 6. Functional Truth Table in Fault Mode

Conditions	CONF	$\overline{\text{INHS}}$	$\overline{\text{INLS}}$	OUT	GLS	$\overline{\text{FS}}$	EN	TEMP	CSNS	OCLS	Comments
Overtemperature on OUT	x	x	x	L	H	L	H	L	x	x	The 33981 is currently in fault mode. The OUT is OFF. TEMP at 0 V indicates this fault. Once the fault is removed 33981 recovers its normal mode.
Overtemperature on GLS	x	x	x	L	L	L	H	L	x	x	The 33981 is currently in fault mode. The OUT is OFF and GLS is at 0 V. TEMP at 0 V indicates this fault. Once the fault is removed 33981 recovers its normal mode.
Overcurrent on OUT	x	H	L	L	x	L	H	x	L	x	The 33981 is currently in fault mode. The OUT is OFF. It is reset by a logic [0] at INHS for at least $t_{RST(diag)}$. When INHS goes to 0 V, CSNS goes to 5.0 V.
Overload on External Low-Side MOSFET	L	L	H	x	L	L	H	x	x	L	The 33981 is currently in fault mode. GLS is at 0 V and OCLS internal current source is off. The external resistance connected between OCLS and GND pin will pull OCLS pin to 0 V. The fault is reset by a logic [0] at INLS for at least $t_{RST(diag)}$.

H = High level
L = Low level
x = Don't care

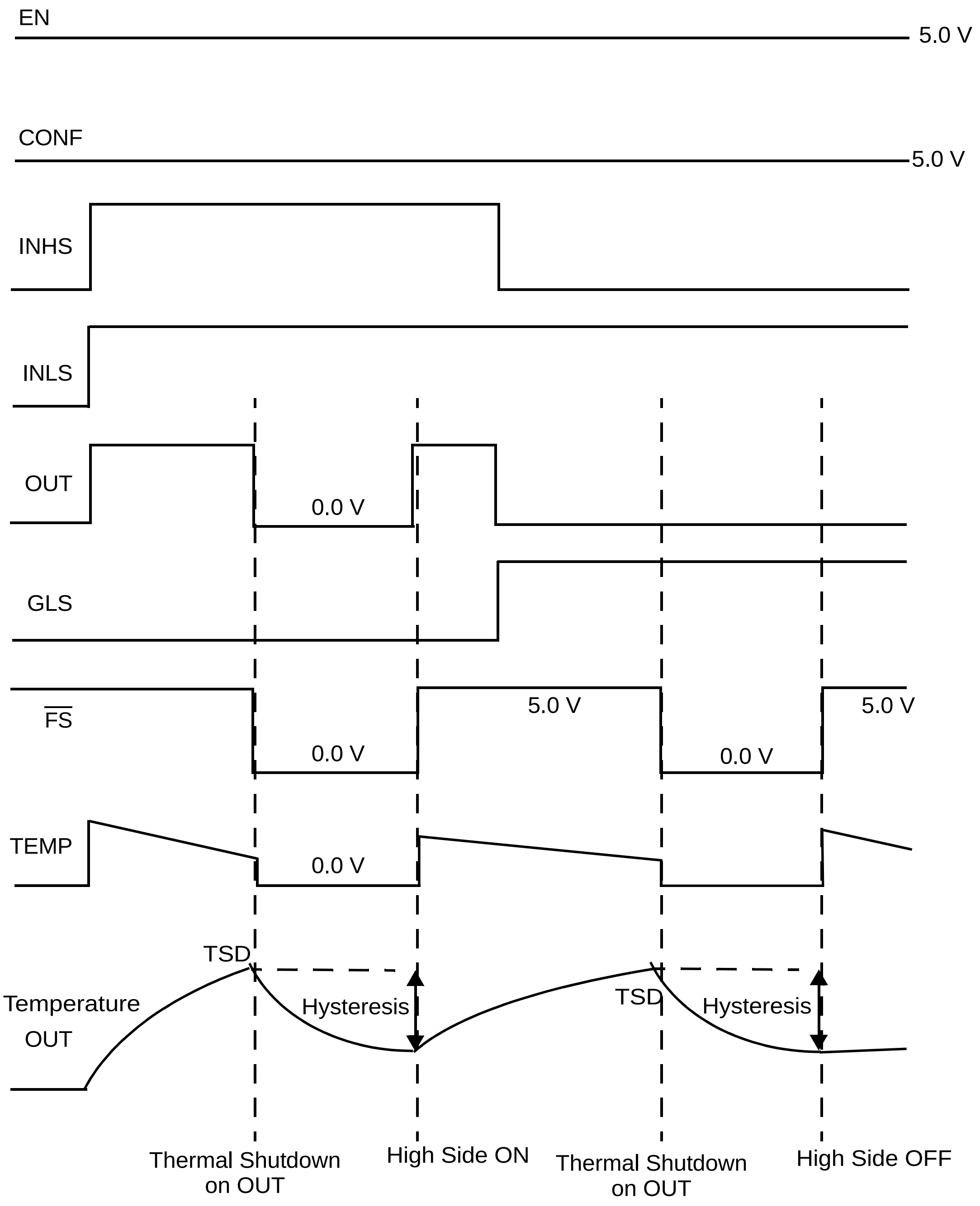


Figure 12. Overtemperature on Output

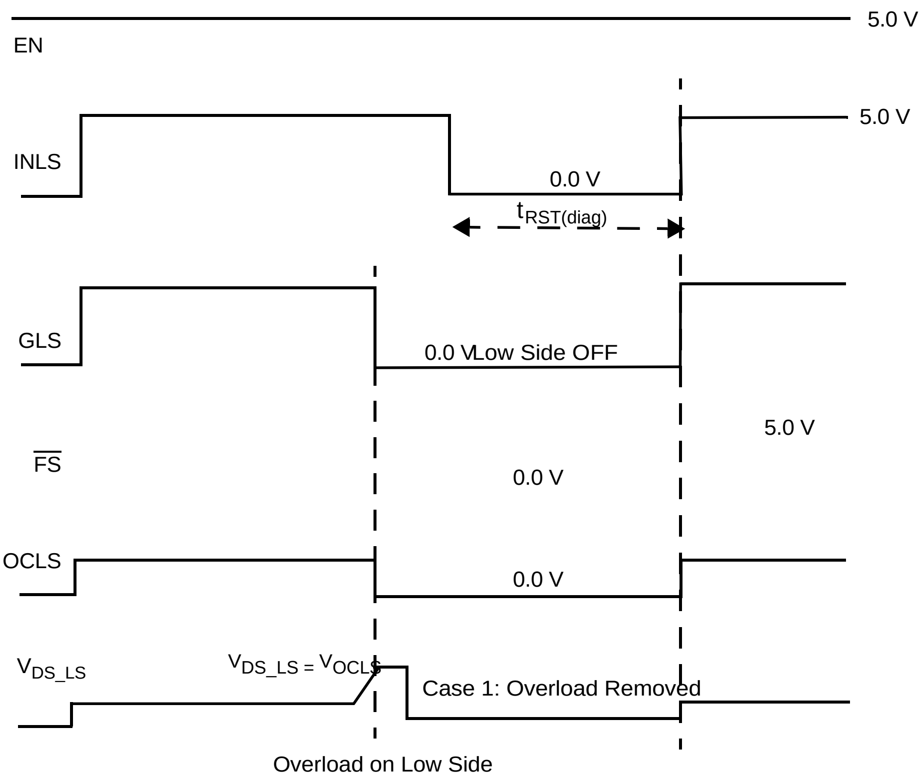


Figure 13. Overload on Low-Side Gate Drive, Case 1

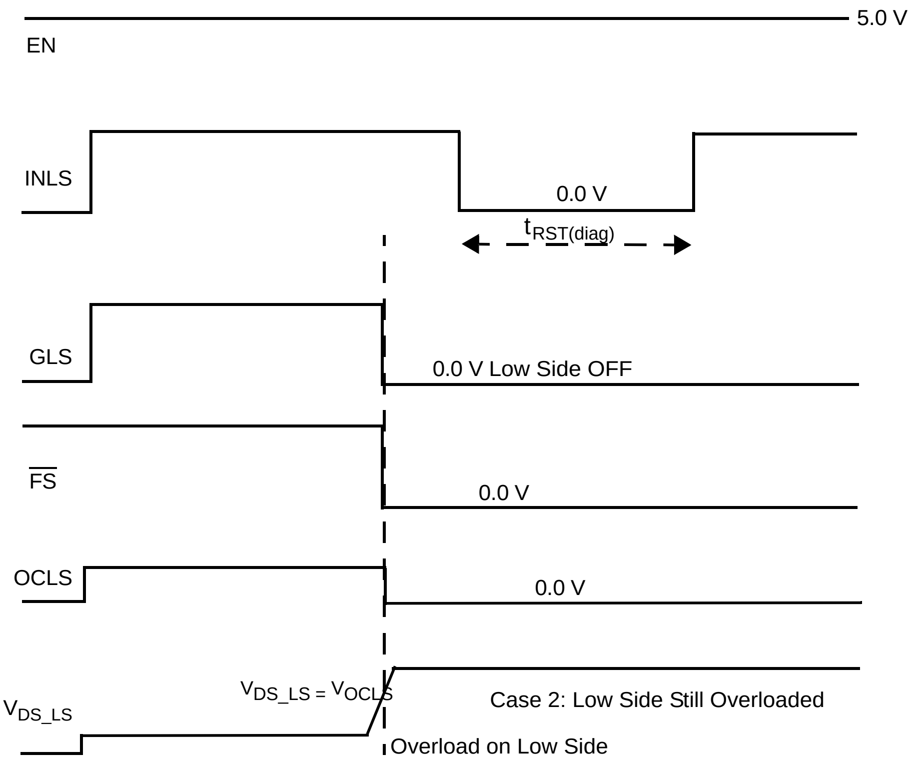


Figure 14. Overload on Low-Side Gate Drive, Case 2

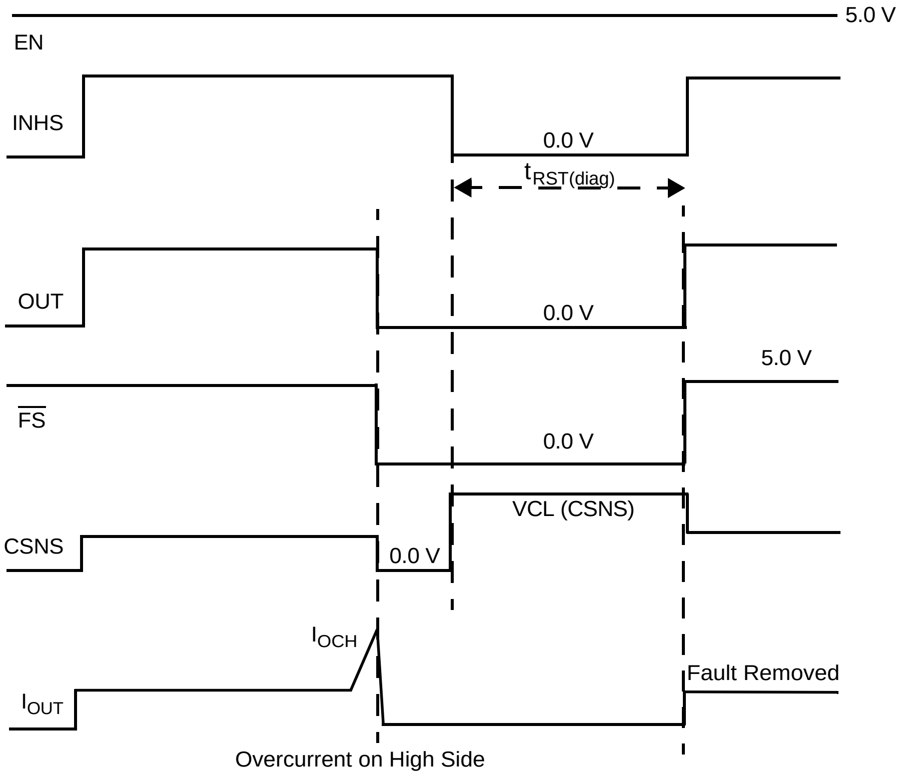


Figure 15. Overcurrent on Output

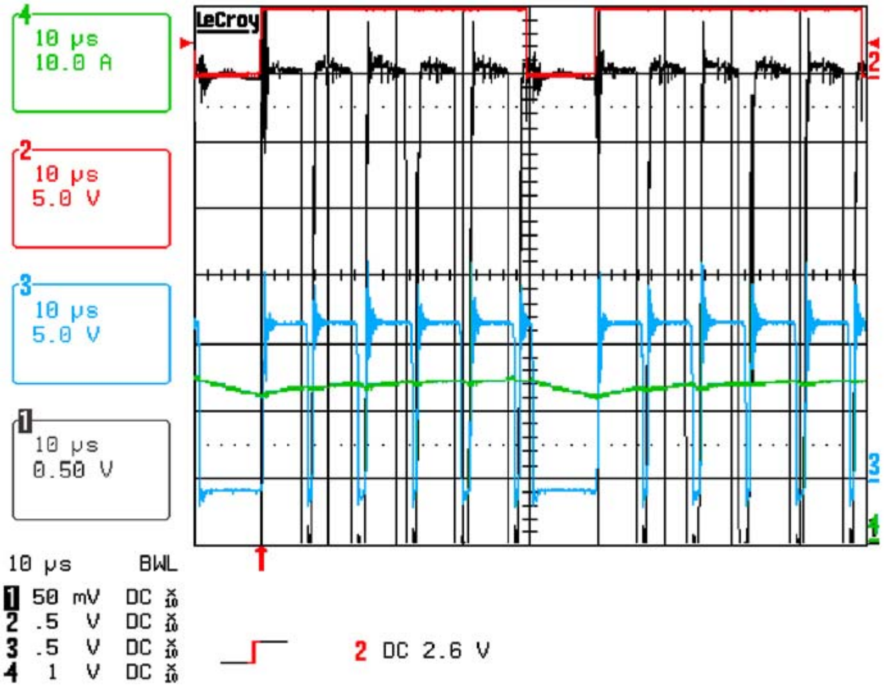


Figure 16. High-Side Overcurrent

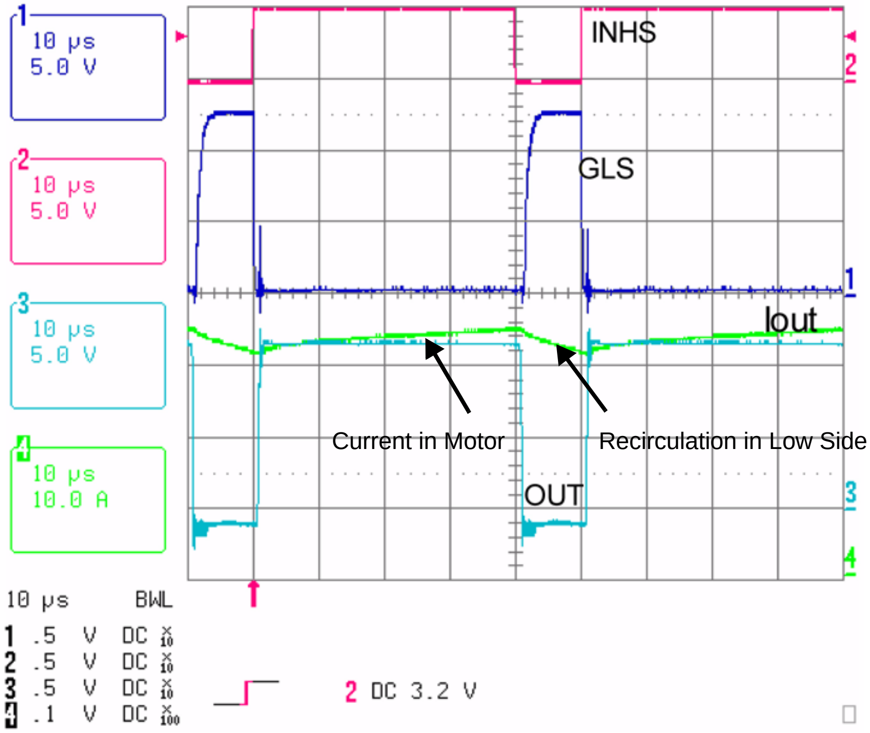


Figure 17. Cross-Conduction with Low Side

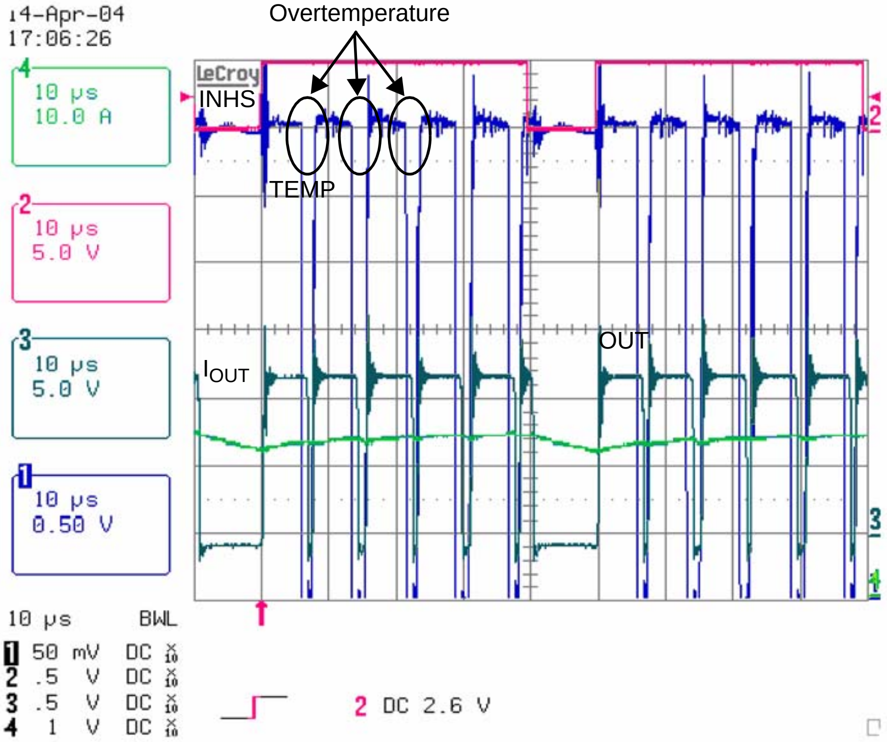


Figure 18. Overtemperature on OUT

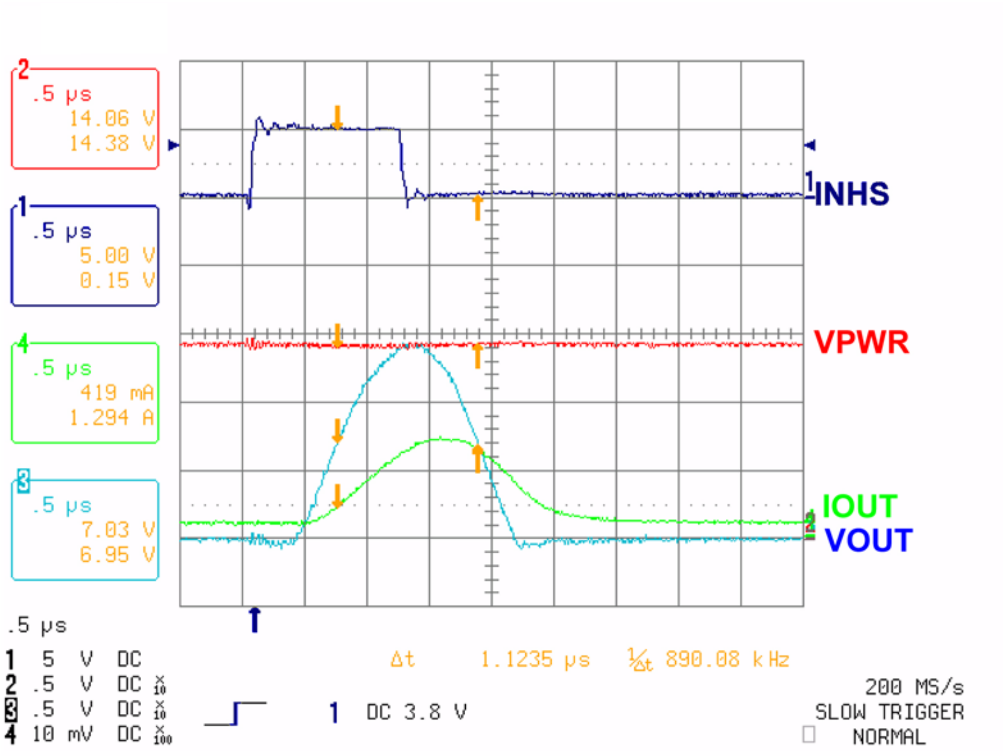


Figure 19. Maximum Operating Frequency for SR Capacitor of 4.7 nF

TYPICAL APPLICATIONS

INTRODUCTION

Figure 20 shows a typical application for the 33981. A brush DC motor is connected to the output. A low-side gate driver is used for the freewheeling phase. Typical values for external capacitors and resistors are given.

.

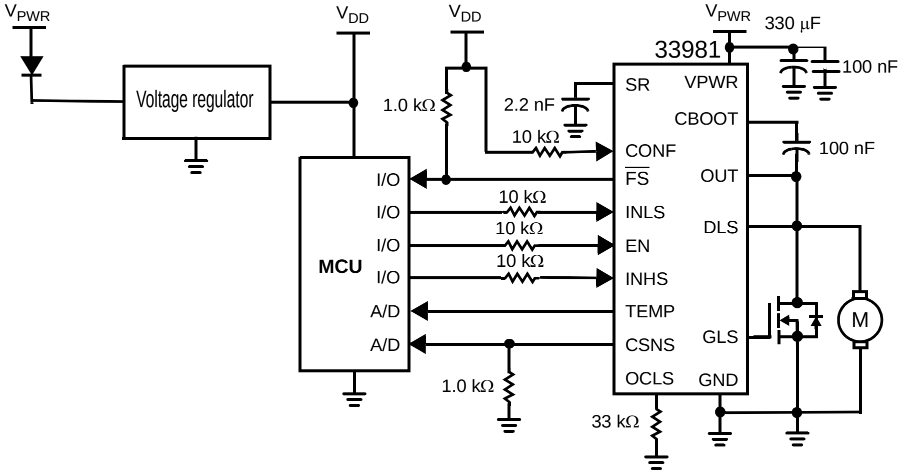


Figure 20. 33981 Typical Application Diagram

EMC AND EMI RECOMMENDATIONS

INTRODUCTION

This section relates the EMC capability for 33981, High Frequency High-Current High-Side Switch. This device is a self-protected silicon switch used to replace electromechanical relays, fuses, and discrete circuits in power management applications.

This section presents the key features of the device and its targeted applications. The automotive standard to measure conducted and radiated emissions is provided. Concrete measurements on the 33981 and improvements to reduce electromagnetic emission are described.

DEVICE FEATURES

This 33981 is a 4.0 mΩ self-protected, high-side switch digitally controlled from a microcontroller (MCU) with extended diagnostics, able to drive DC motors up to 60 kHz.

A bootstrap architecture has been used to provide fast transient gate voltage in order to reach 4.0 mΩ $R_{DS(ON)}$ maximum at room temperature. In parallel, a charge pump is implemented to offer continuous on-state capability. This dual current supply of the high-side MOSFET allows a duty cycle from 5% to 100%. An external capacitor connected between pins SR and GND is used to control the slew rate at the output and, therefore, reduce electromagnetic perturbations.

In standard configuration, the motor current recirculation is handled by an external freewheeling diode. To reduce global power dissipation, the freewheeling diode can be replaced by an external discrete MOSFET in low-side configuration. The IC integrates a gate driver that controls and protects this external MOSFET in the event of short circuit to battery. The product manages the cross conduction between the internal high side and the external low side when used in a half bridge configuration. The two MOSFETs can be controlled independently when the CONF pin is at 0 V. To eliminates fuses, the device is self-protected from severe short-circuits (100 A typical) with an innovative overcurrent strategy.

The 33981 has a current feedback for real-time monitoring of the load current through an MCU analog/digital converter to facilitate closed-loop operation for motor speed control.

The 33981 has an analog thermal feedback that can be used by the MCU to monitor PC board temperature to optimize the motor control and to protect the entire electronic system. Therefore, an over temperature shutdown feature protects the IC against high overload condition.

Figure 21 illustrates the typical application diagram.

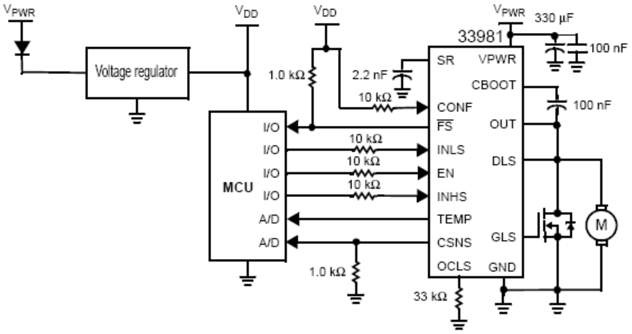


Figure 21. Typical Application Diagram

APPLICATION

Engine cooling, air conditioning, and fuel pump are the targeted automotive applications for the 33981. Conventional solutions are designed with discrete components that are not optimized in terms of component board size, protection, and diagnostics. The 33981 is the right candidate to develop lighter and more compact units.

DC motor speed adjustment allows optimization of energy consumption by reducing supply voltage, hence the mean voltage, applied to the motor. The commonly used control technique is pulse wide modulation (PWM) where the average voltage is proportional to the duty cycle. Most applications require a PWM frequency of at least 20 kHz to avoid audible noise. Figure 22 illustrates typical waveforms when switching the 33981 at 20 kHz with a duty cycle of 80%. The output voltage (OUT) and current in the motor (I_{MOTOR}) waveforms are represented.

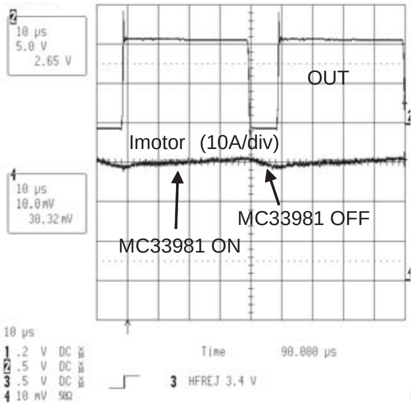


Figure 22. Current and Voltage waveforms

HOW TO MEASURE ELECTROMAGNETIC EMISSION ACCORDING TO THE CISPR25

One EMC standard in the automotive world (at system level) is the CISPR25, edited by the International Electrotechnical Commission. This standard describes the measurement method to measure both conducted and radiated emission.

CONDUCTED EMISSION MEASUREMENT

Conducted emission is the emission produced by the device on the battery cable. The test bench is described by CISPR25 (see Figure 23, Test Bench for Conducted Emission, on page 23).

The Line Impedance Stabilization Network (LISN), also called Artificial Network (AN), in a given frequency range (150 kHz to 108 MHz) provides a specified load impedance for the measurement of disturbance voltages and isolates the equipment under test (EUT) from the supply in that frequency range.

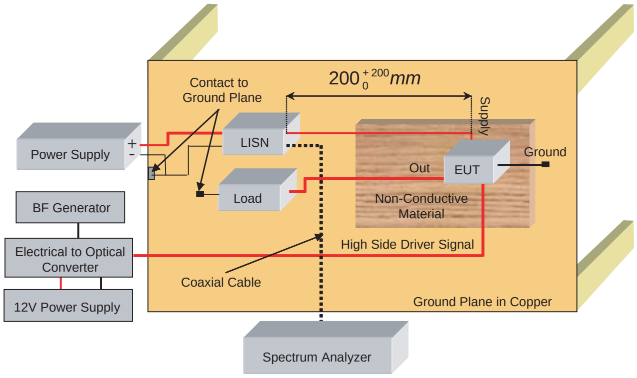


Figure 23. Test Bench for Conducted Emission

The EUT must operate under typical loading and other conditions just as it must in the vehicle so maximum emission state occurs. These operating conditions must be clearly defined in the test plan to ensure that both supplier and customer are performing identical tests.

For the testing described in this application note, the out pin of the 33981 was connected to an inductive load (0.47 Ω + 1.0 mH) switching at 20 kHz with a duty cycle of 80%. The output current was 17 A continuous.

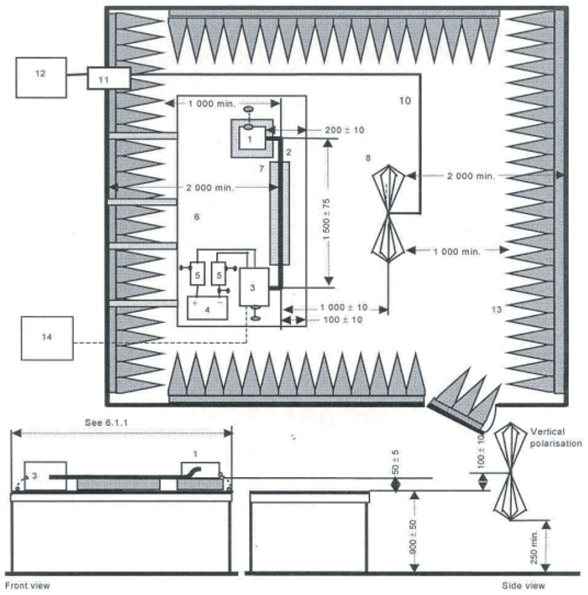
The ground return of the EUT to the chassis must be as short as possible. The power supply is 13.5 V.

RADIATED EMISSION MEASUREMENT

The radiated emission measurement consists of measuring the electromagnetic radiation produced by the equipment under test. CISPR 25 gives the schematic test bench described in Figure 24, Test Bench for Radiated Emission, on page 24.

To measure radiated emission over all frequency ranges, several antenna types must be used:

- 0.15 MHz to 30 MHz: 1.0 m vertical monopole in vertical polarization.
- 30 MHz to 200 MHz: a biconical antenna used in vertical and horizontal polarization.
- 200 MHz to 1,000 MHz: a log-periodic antenna used in vertical and horizontal polarization.



Key

1	EUT (grounded locally if required in test plan)	8	Biconical antenna
2	Test harness	–	–
3	Load simulator (placement and ground connection)	10	High quality double-shielded coaxial cable (50 Ω)
4	Power supply (location optional)	11	Bulkhead connector
5	Artificial Network (AN)	12	Measuring instrument
6	Ground plane (bonded to shielded enclosure)	13	RF absorber material
7	Low relative permittivity support ($\varepsilon\rho \leq 1.4$)	14	Stimulation and monitoring system

Figure 24. Test Bench for Radiated Emission

EMC RESULTS AND IMPROVEMENTS

The 33981 OUT is connected to an inductive load (0.47 Ω + 1.0 mH) switching at 20 kHz with duty = 80%. The current in the load was 17 A continuous.

BOARD SETUP

The initial configuration of our 33981 board is represented in Figure 25.

No SR capacitor is used. Therefore, the obtained switching times are the maximum values. A capacitor of 1000 mF is connected between VPWR and GND.

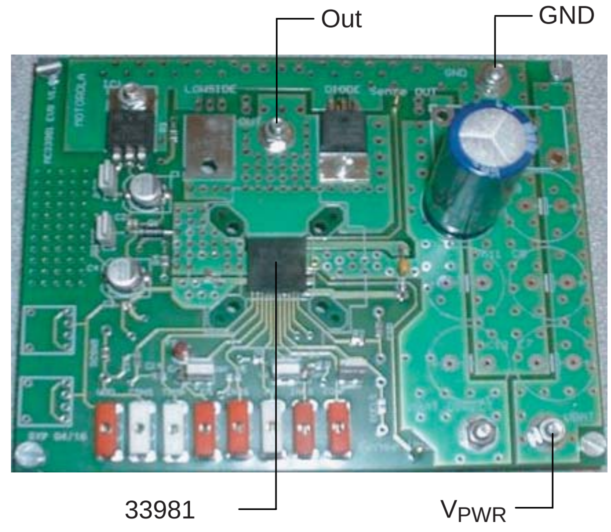


Figure 25. 33981 Initial Configuration

CONDUCTED MEASUREMENTS

TEST SETUP

To perform a conducted emission measurement in accordance with the CISPR 25 standard, the test bench in Figure 26, Conducted Emission Test Setup, on page 24 was developed.

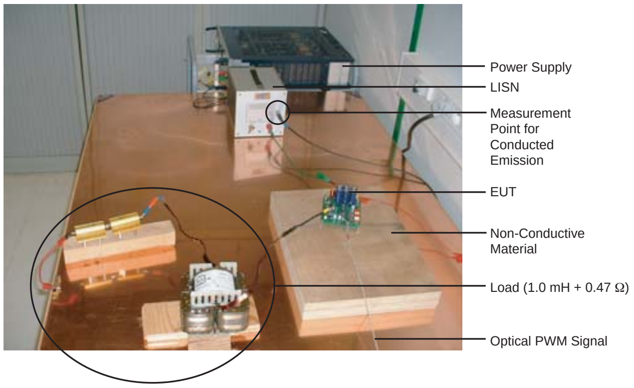


Figure 26. Conducted Emission Test Setup

EFFECTS OF SOME PARAMETERS

The conducted emissions level rise with the duty cycle. When the duty increases the di/dt on the VPWR line is higher. The device has to deliver more current and provide more energy. Figure 27 describes the effect of duty cycle increase on the V_{PWR} current waveform. The conducted emission level rises with the output frequency. This is due to the increasing number of commutations.

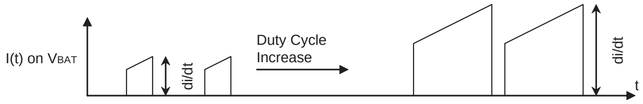


Figure 27. VPWR Current

HOW TO REDUCE ELECTROMAGNETIC EMISSION

By adjusting the slew rate of the device during turn ON and turn OFF with SR capacitor, the electromagnetic emissions can be reduced.

Conductive emission tests were performed (taking care of the board filtering and routing that have a big impact on EMC performances).

An optimized solution was found by adding the following external components to the initial board:

- PI filter on the V_{PWR}: 2 x 3 mF and 3.5 uH
- RC IN filter between V_{PWR} and GND: a 2.0 Ω resistor in series with a 100 nF capacitor
- RC Out filter between OUT and GND: a 4.7 Ω resistor in series with a 100 nF capacitor
- Capacitor C1 of 10 nF between V_{PWR} and GND
- Capacitor C2 of 10 nF between OUT and GND
- Capacitor C3 of 10 nF between OUT and V_{PWR}
- Capacitor SR of 3.3 nF

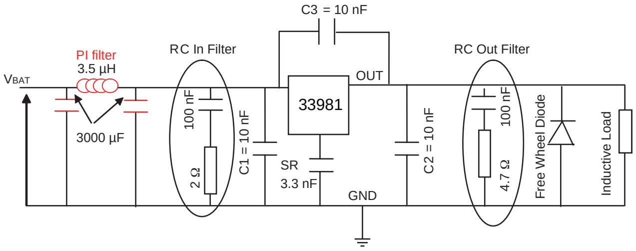


Figure 28. 33981 with Filter

The EMC enhanced board with adapted value filter is represented in Figure 29, Enhanced Board, on page 25.

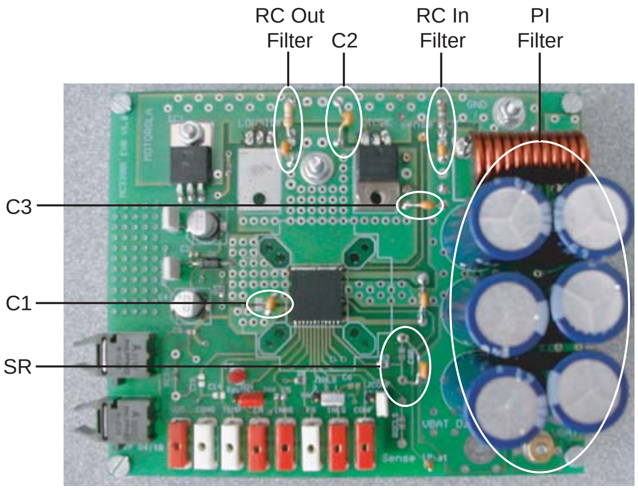


Figure 29. Enhanced Board

The chart in Figure 30 shows the spectrum of the enhanced board and the initial board. The improvement is appreciatively 15 dB to 20 dB in the all frequency range. The enhanced board is now in accordance with the Class 3 limits of the CISPR25 standard for conducted emission.

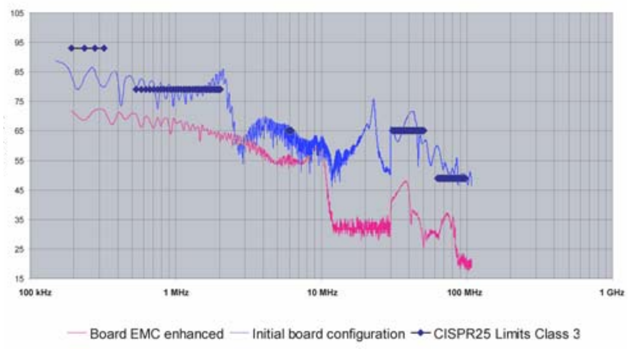


Figure 30. Conducted Emission Spectrum for 33981

RADIATED MEASUREMENTS

This test was performed in order to evaluate the characteristic of the device relating to radiated emission. Measurements have been done in accordance with the

CISPR 25 standard as shown in Figure 31. The tested board was the EMC enhanced board.

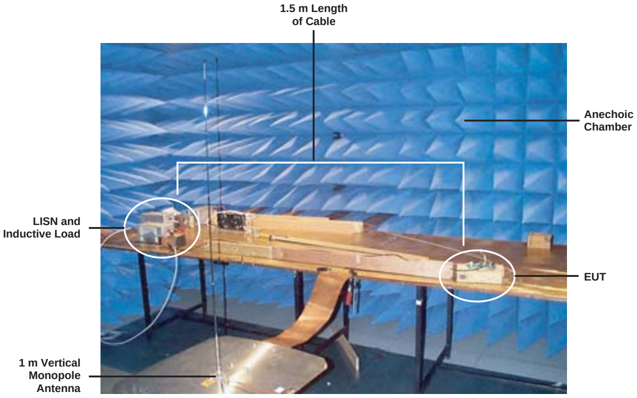


Figure 31. Radiated Emission Test Set Up

The results of these measurements are represented in Figure 32. The enhanced board is in accordance with the Class 3 limits of the CISPR25 standard for radiated emission.

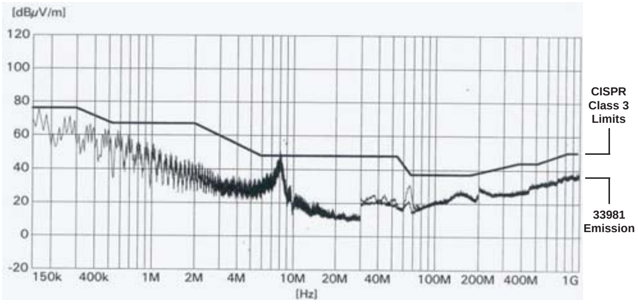


Figure 32. Radiated Emission Spectrum for 33981

CONCLUSION

This document explains how to measure conducted and radiated emission in accordance with the automotive CISPR25 standard. Measurements were performed on the 33981 in real application conditions when driving an inductive load. An optimized filtering solution was put in place to have the tested system in accordance with the Class 3 limits. The same method can be used with other PC boards.

POWER DISSIPATION

INTRODUCTION

This section relates to the power dissipation capability for 33981, High Frequency High-Current High-Side Switch. This device is a self-protected silicon switch used to replace electromechanical relays, fuses, and discrete circuits in power management applications.

This section presents the key features of the device and its targeted applications. The theoretical calculations for power dissipation and die junction temperatures are determined in this document for inductive loads. A concrete example with DC motor driven by the 33981 is analyzed in section DC Motor 200 W.

DEVICE FEATURES

This 33981 is a 4.0 mΩ self-protected, high-side switch digitally controlled from a microcontroller (MCU) with extended diagnostics, able to drive DC motors up to 60 kHz.

A bootstrap architecture has been used to provide fast transient gate voltage in order to reach 4.0 mΩ $R_{DS(ON)}$ maximum at room temperature. In parallel, a charge pump is implemented to offer continuous on-state capability. This dual current supply of the high-side MOSFET allows a duty cycle from 5% to 100%. An external capacitor connected between pins SR and GND is used to control the slew rate at the output and, therefore, reduce electromagnetic perturbations.

In standard configuration, the motor current recirculation is handled by an external freewheeling diode. To reduce global power dissipation, the freewheeling diode can be replaced by an external discrete MOSFET in low-side configuration. The IC integrates a gate driver that controls and protects this external MOSFET in the event of short circuit to battery. The product manages the cross conduction between the internal high side and the external low side when used in a half bridge configuration. The two MOSFETs can be controlled independently when the CONF pin is at 0 V. To eliminates fuses, the device is self-protected from severe short-circuits (100 A typical) with an innovative overcurrent strategy.

The 33981 has a current feedback for real-time monitoring of the load current through an MCU analog/digital converter to facilitate closed-loop operation for motor speed control.

The 33981 has an analog thermal feedback that can be used by the MCU to monitor PC board temperature to optimize the motor control and to protect the entire electronic system. Therefore, an over temperature shutdown feature protects the IC against high overload condition.

Figure 33 illustrates the typical application diagram.

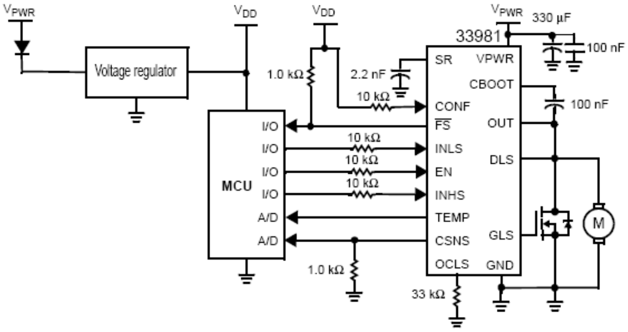


Figure 33. Typical Application Diagram

APPLICATION

Engine cooling, air conditioning, and fuel pump are the targeted automotive applications for the 33981. Conventional solutions are designed with discrete components that are not optimized in terms of component board size, protection, and diagnostics. The 33981 is the right candidate to develop lighter and more compact units.

The adjustment of the DC motor speed allows optimizing of energy consumption. It is realized by chopping the supply voltage, hence the mean voltage, applied to the motor. The commonly used control technique is pulse wide modulation (PWM) where the average voltage is proportional to the duty cycle. Most applications require a PWM frequency of at least 20 kHz to avoid audible noise. Figure 34 illustrates typical waveforms when switching the 33981 at 20 kHz with a duty cycle of 80%. The output voltage (OUT) and current in the motor (I_{MOTOR}) waveforms are represented.

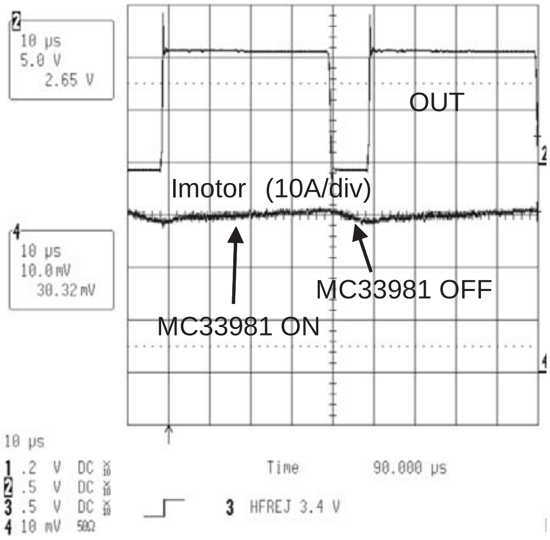


Figure 34. Current and Voltage waveforms

POWER DISSIPATION

The 33981 power dissipation is the sum of two kinds of losses:

- On-State losses when device is fully ON,
- Switching losses when the device switches ON and OFF.

The analysis that follows assumes an inductive load and assumes that the current is constant in the load.

The case being considered in this paper is inductive load and the hypothesis is that the current is constant in the load.

ON-STATE LOSSES

The mean on-state loss periods in the 33981 can be calculated as follows:

$Pon\_state = a \cdot R_{DS(ON)} \cdot I_{OUT}^2$ where 'a' is the duty cycle.

The critical parameter is the on resistance ($R_{DS(ON)}$) that increases with temperature. The 33981 has a maximum $R_{DS(ON)}$ at 25ºC of 4.0 mΩ and its deviation with temperature is only 1.7 as shown in Figure 35.

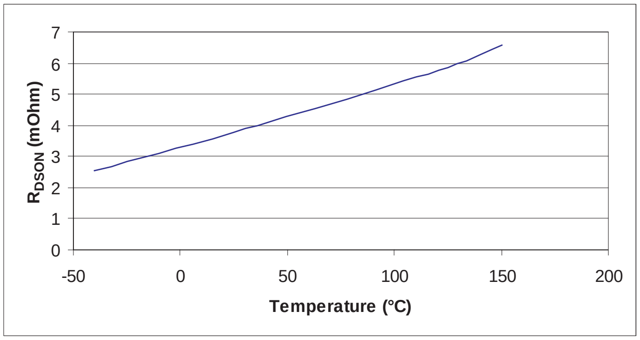


Figure 35. $R_{DS(ON)}$ vs. Temperature

SWITCHING LOSSES

The mean switching losses in the 33981 can be calculated as follows:

$Pswitching = (t_{ON} \,.\, F_{REQ} \,.\, V_{PWR} \,.\, I_{OUT}) / 2 + (t_{OFF} \,.\, F_{REQ} \,.\, V_{PWR} \,.\, I_{OUT}) / 2$

where t_{ON}/t_{OFF} is the turn on/off time.

The switching time is a critical parameter. The 33981 provides adjustable slew rates through an external capacitor (SR) that slow down the rise and fall times to reduce the electromagnetic emissions. However, this adjustment will have an impact on power dissipation. Figure 36 gives the positive (SR_R) and negative (SR_F) slew rate versus different values of SR. This is illustrated in Figure 37.

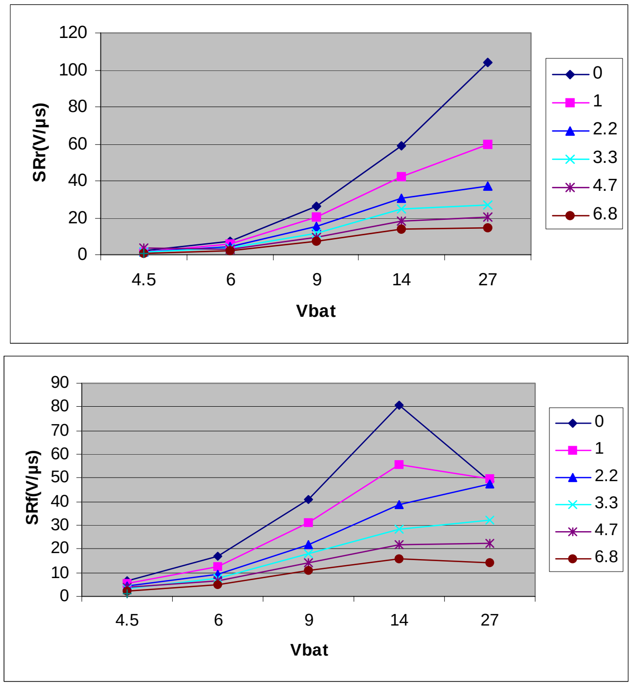


Figure 36. Positive and Negative Slew Rate vs. SR Capacitor

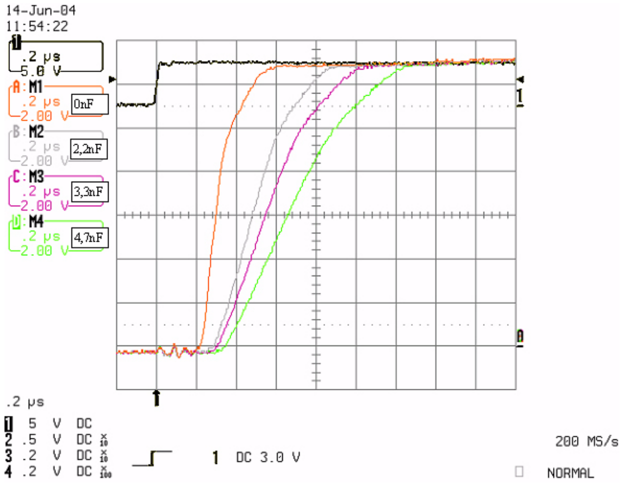


Figure 37. OUT switching vs. SR Capacitor

JUNCTION TEMPERATURE

The junction temperature of the 33981 can be calculated knowing the power dissipation and the thermal characteristics of the PC board with this formula:

$$T_J = T_A + (\text{Pon\_state} + \text{Pswitching}).\ R_{THJA}$$

where T_J is the junction temperature, T_A the ambient temperature, and R_{THJA} the thermal impedance junction to ambient.

RECIRCULATION PHASE

In standard configuration, the motor current recirculation is handled by an external freewheeling diode. With the 33981, the freewheeling diode can be replaced by an external low-side discrete MOSFET.

The power dissipation during the recirculation phase is calculated as follows for the diode and the low-side MOSFET respectively:

$$\text{Pdiode} = (1\text{-a})\ .\ V_F\ .\ I_{OUT}$$

where ‘a’ is the duty cycle

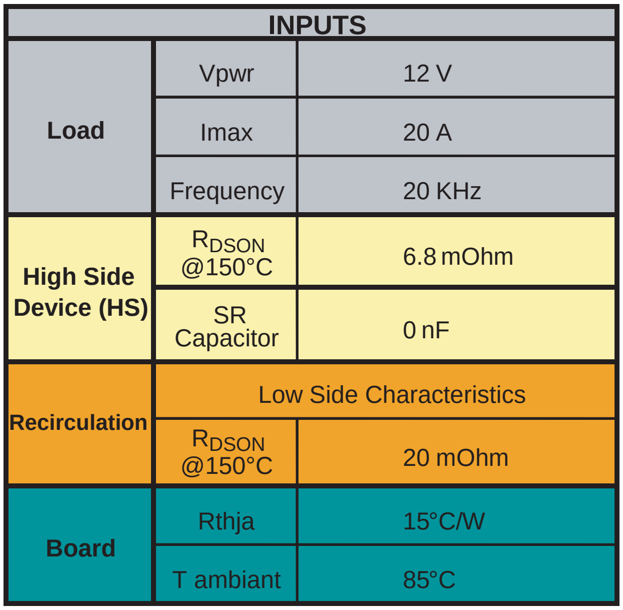
$$\text{Pmosfet\_ls} = (1\text{-a})\ .\ R_{DS(ON)\_ls}\ .\ I_{OUT}^2$$

where $R_{DS(ON)\_ls}$ is the on resistance of the low side.

APPLICATIONS EXAMPLES

EXCEL TOOL

An excel tool has been created with all the above formulas to calculate the dissipated power and the junction temperature knowing the application conditions. An example of the interface is given in Figure 38. The parameters to enter concern the load, the high-side device, the recirculation, and the board. They are V_{PWR}, DC current in the load (Imax for 100% of duty cycle), PWM frequency, 33981 $R_{DS(ON)}$ at 150ºC, SR capacitor, low-side $R_{DS(ON)}$ at 150ºC, ambient temperature, and thermal impedance.



INPUTS		
Load	Vpwr	12 V
	Imax	20 A
	Frequency	20 KHz
High Side Device (HS)	RDSON @150°C	6.8 mOhm
	SR Capacitor	0 nF
Recirculation	Low Side Characteristics	
	RDSON @150°C	20 mOhm
Board	Rthja	15°C/W
	T ambiant	85°C

Figure 38. Excel Tool

The calculations are done with the maximum $R_{DS(ON)}$ for the 33981 and the low side. The current is also considered constant in the load. The model taken for the V_F of the diode is $(0.4 + 0.01\ .\ I_{OUT})$ Volts.

The listed conditions in Figure 38 are the ones chosen for the entire document.

DC MOTOR 200 W

A concrete example is the 33981. A 200 W DC motor, a frequency of 20 kHz, and an ambient temperature of 85ºC are chosen. The 33981 is evaluated using the following board. The thermal impedance of the board is in the range of 15ºC/W.

Figure 39. 33981 Evaluation Board

POWER DISSIPATION

Figure 40 illustrates the power dissipation in the 33981. The conditions are listed in Figure 38. Maximum power dissipation of 3.1 W is obtained with a duty of 95%.

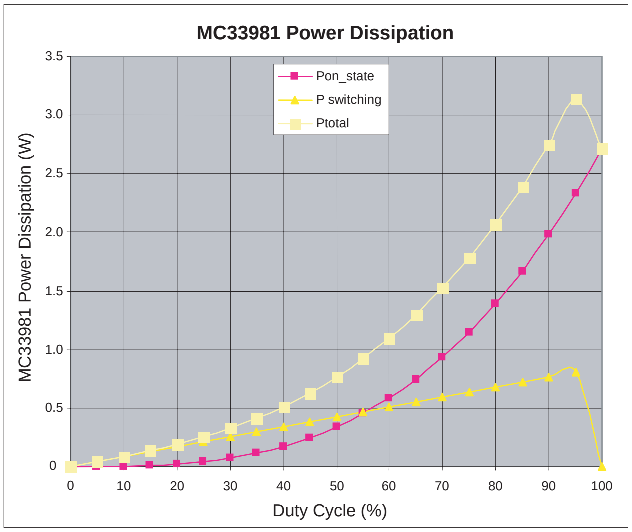


Figure 40. Power Dissipation (Pon and Pswitching) vs. Duty Cycle

INFLUENCE OF SR CAPACITOR

The SR capacitor value has an impact on these switching losses. Figure 41 illustrates the percentage of the switching losses versus the total power dissipation for the same load conditions as Figure 38. The higher the SR capacitor value, the higher the switching losses. They can be more than 50% of the total power dissipation in the 33981 with a 4.7 nF capacitor and is a basic applications trade-off. A compromise should be found between the power dissipation and the electromagnetic capability (EMC) performance.

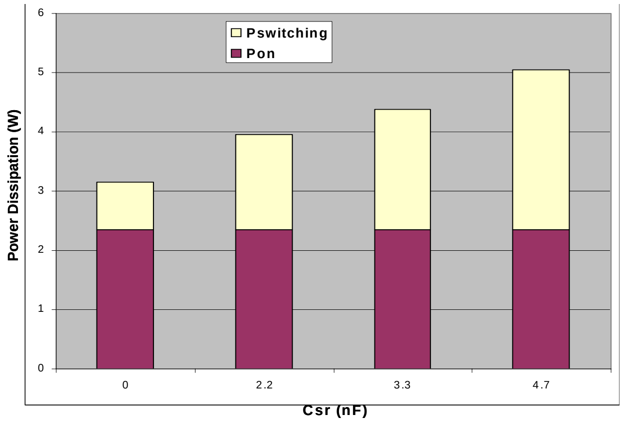


Figure 41. Power Switching vs. SR Capacitor

RECIRCULATION PHASE

Figure 42 illustrates the power dissipation for the two recirculation approaches, diode or low-side MOSFET. The power dissipation gain for the entire system when using the low side instead of the diode can reach up to 1.5 W with a duty cycle of 50%.

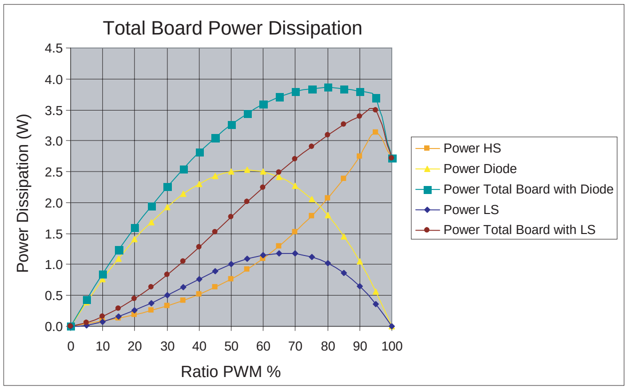


Figure 42. Total Board Power Dissipation

JUNCTION TEMPERATURE

The junction temperature of the 33981 versus duty cycle for the condition listed in Figure 38, is given in Figure 43. The maximum obtained junction temperature is 132ºC with a duty cycle of 95%. This value is far from the 150ºC maximum guaranteed junction.

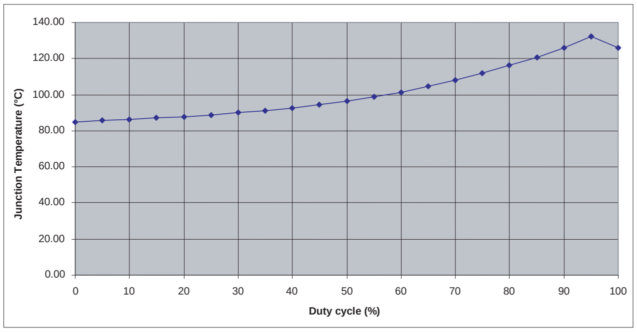


Figure 43. Junction Temperature vs. Duty Cycle

CONCLUSION

Knowing the application conditions, this document explained how to calculate power dissipation during on-state and switching phases and the junction temperature for the 33981 when controlling a DC motor. A concrete example with a 200 W DC motor was given in section DC Motor 200 W. The same principle can be used for other DC motor and other environmental conditions.

PACKAGING

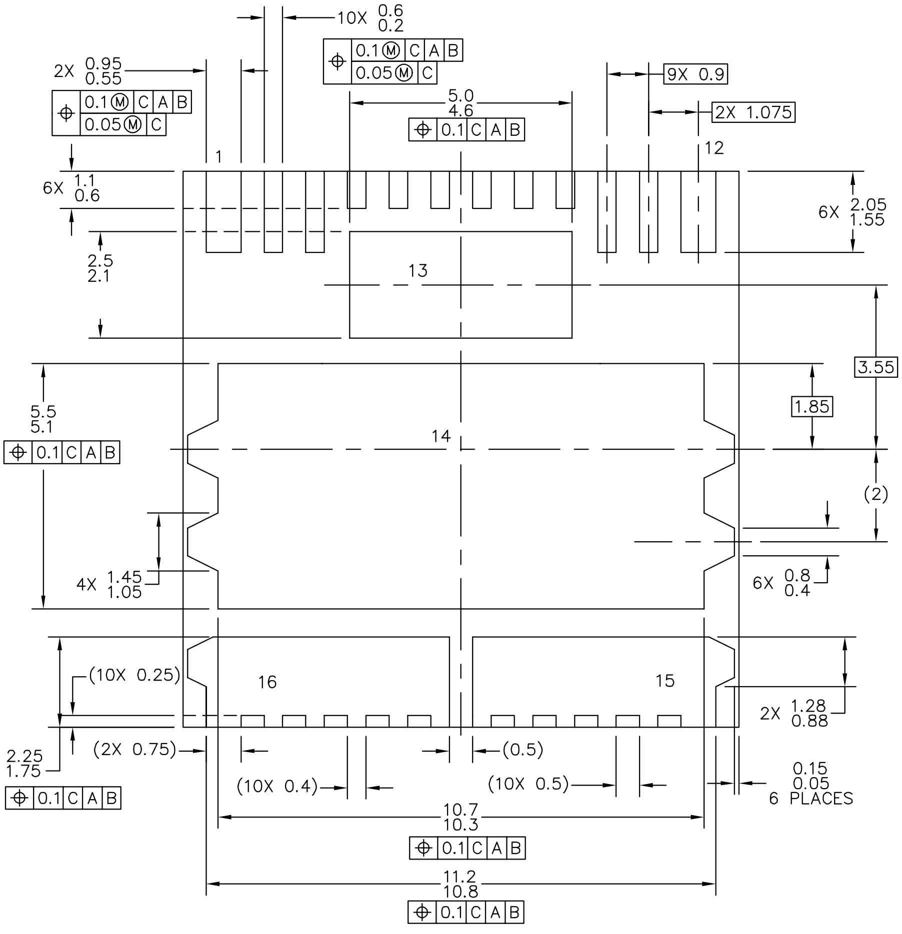
SOLDERING INFORMATION

The 33981 is not designed for immersion soldering. The maximum peak temperature during the soldering process should not exceed 245^{o}C. Pin soldering limit is for 10 seconds maximum duration. Exceeding these limits may cause malfunction or permanent damage to the device.

PACKAGING DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using “98ARL10521D”.

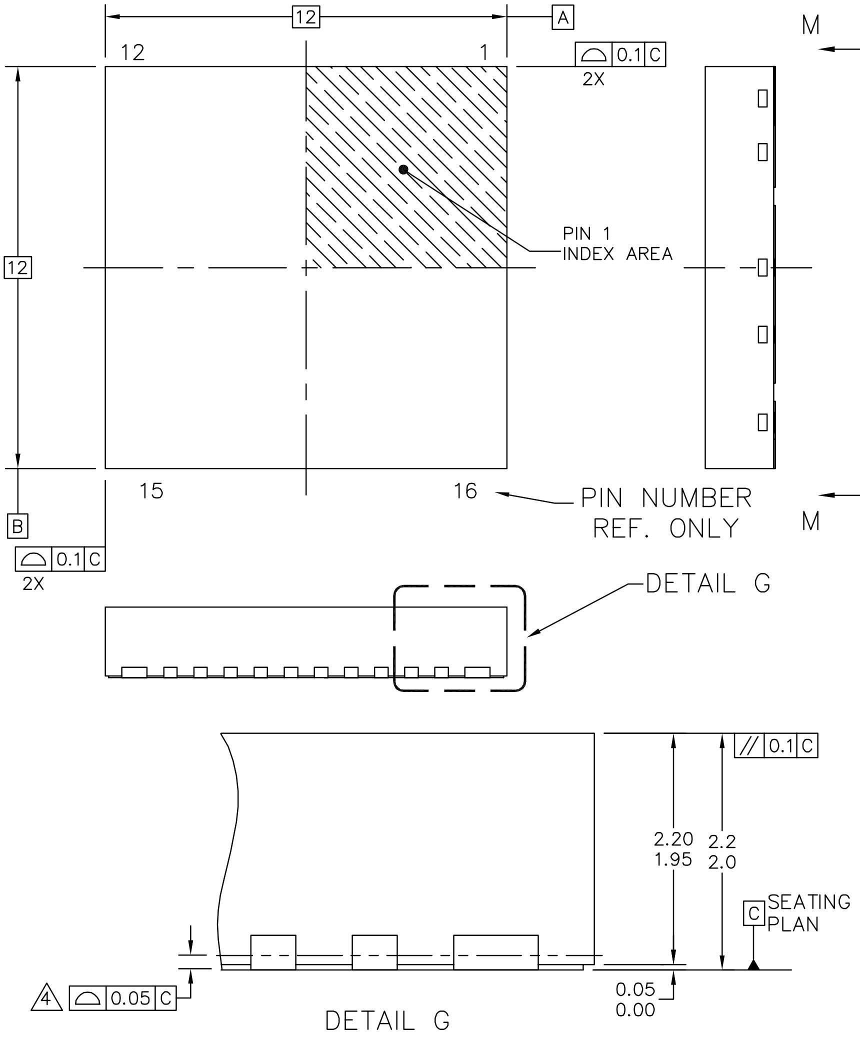
PNA SUFFIX
16-PIN PQFN
PLASTIC PACKAGE
98ARL10521D
ISSUE C



VIEW M–M

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 16 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10521D	REV: C
	CASE NUMBER: 1402–02	27 APR 2005
	STANDARD: NON–JEDEC	

PNA SUFFIX
16-PIN PQFN
PLASTIC PACKAGE
98ARL10521D
ISSUE C



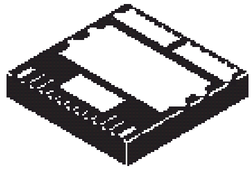
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 16 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10521D	REV: C
	CASE NUMBER: 1402-02	27 APR 2005
	STANDARD: NON-JEDEC	

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

33981

**16-PIN
PQFN**



**PNA SUFFIX
98ARL10521D
16-PIN PQFN
12 MM X 12 MM**

Note For package dimensions, refer to the 33981 device datasheet.

INTRODUCTION

This thermal addendum is provided as a supplement to the 33981 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

PACKAGING AND THERMAL CONSIDERATIONS

This package is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R\theta_{JAmn}$.

For *m*, *n* = 1, $R\theta_{JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R\theta_{JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R\theta_{J21}$ and $R\theta_{J22,}$ respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

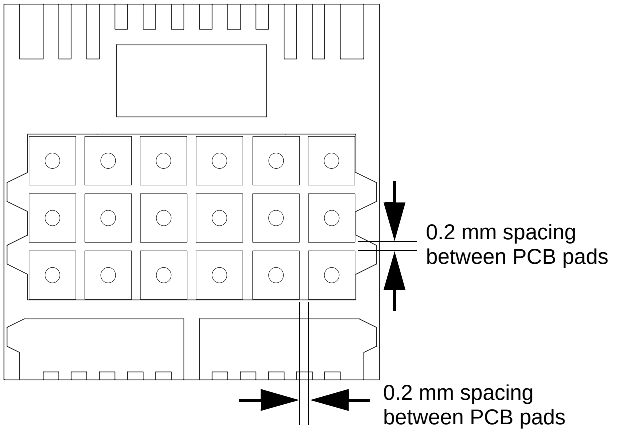
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

STANDARDS

Table 7. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$P_{\theta JAmn}$ (1), (2)	22	18	41
$P_{\theta JBmn}$ (2), (3)	7.0	4.0	27
$P_{\theta JAmn}$ (1), (4)	62	48	81
$P_{\theta JCmn}$ (5)	<1.0	0.0	1.0

Notes
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



Note: Recommended via diameter is 0.5 mm. PTH (plated through hole) via must be plugged / filled with epoxy or solder mask in order to minimize void formation and to avoid any solder wicking into the via.

Figure 44. Surface mount for power PQFN with exposed pads

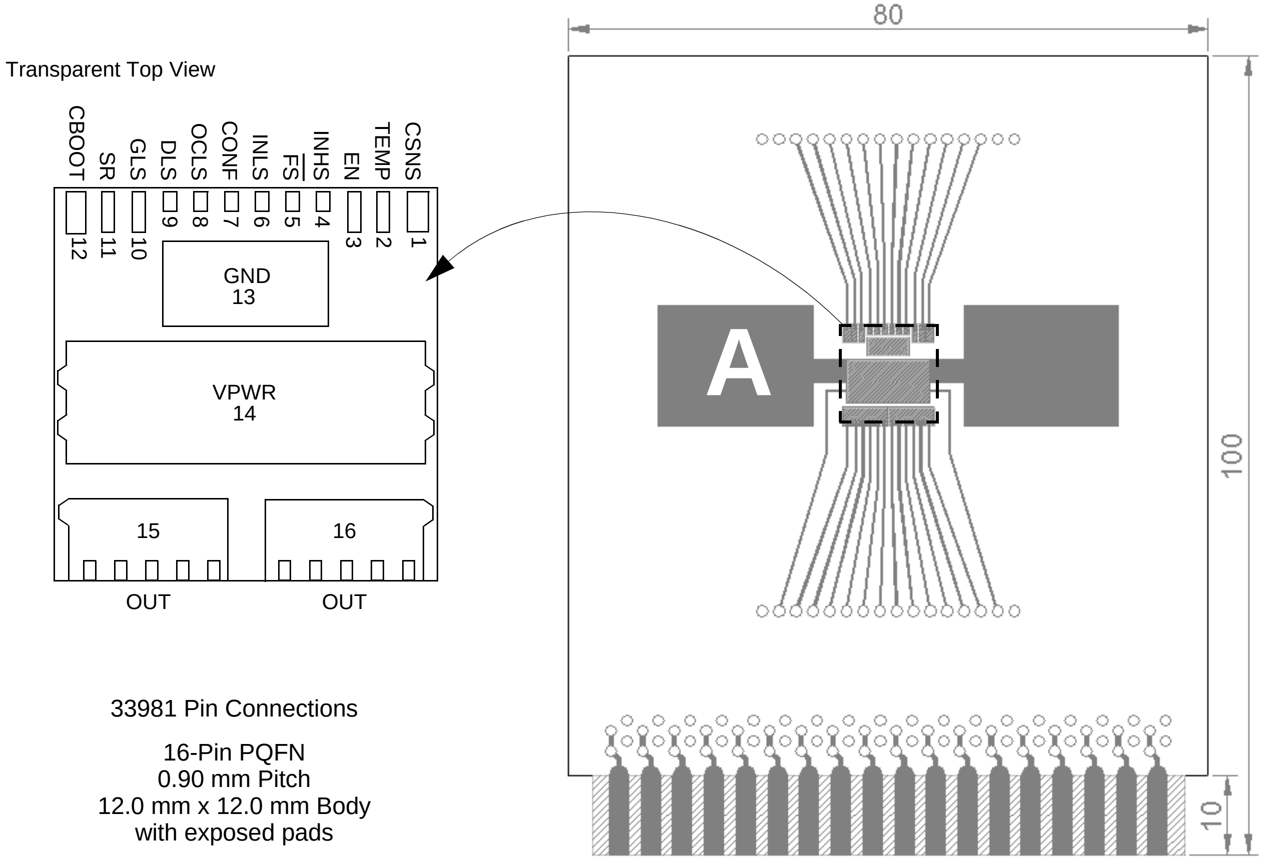


Figure 45. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 8. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		$m = 1$, $n = 1$	$m = 1$, $n = 2$ $m = 2$, $n = 1$	$m = 2$, $n = 2$
$R_{\theta JAmn}$	0	66	51	84
	300	47	37	73
	600	43	34	70

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

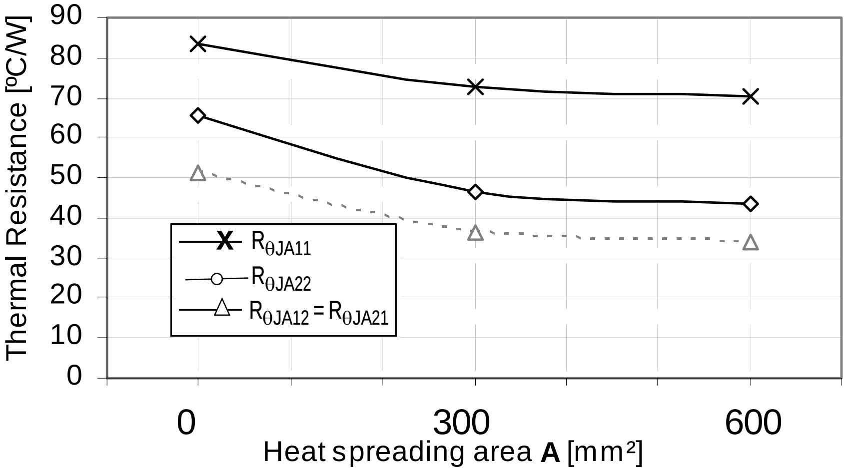


Figure 46. Device on Thermal Test Board $R_{\theta JA}$

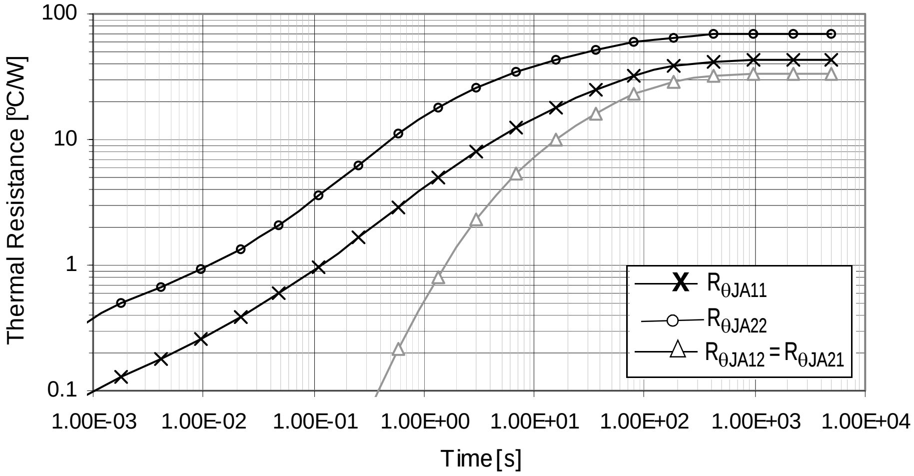


Figure 47. Transient Thermal Resistance $R_{\theta JA}$,
1W Step response,Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	1/2006	• Implemented Revision History page • Made content updates and changes • Converted to Freescale format • Added Thermal Addendum
4.0	3/2006	• Made minor content changes to pages 6 and 7. • Updated to Product Preview status
5.0	7/2006	• Changed Part Number from PC33981PNA to MC33981BPNA (page 1) • Changed Electrical Characteristics, Maximum Ratings, Table 2, Maximum Ratings, Electrical Ratings, OCLS Voltage, from “-5.0 to 5.0” to “-5.0 to 7.0” (page 4). • Changed Electrical Characteristics, Static Electrical Characteristics, Table 3, Static Electrical Characteristics, Low Side Gate Driver (VPWR, VGLS, VOCLS), Low-Side Overload Detection Level versus Low-Side Drain Voltage Minimum, from “-75” to “-50” and Maximum from “+75” to “+50” (page 6). • Changed Electrical Characteristics, Dynamic Electrical Characteristics, Table 4, Dynamic Electrical Characteristics, Control Interface and Power Output Timing (CBOOT, VPWR), Input Switching Frequency, Minimum from “20” to “-” and Typical from “-” to “20” (page 7). • Updated to Advanced status
6.0	5/2007	• Changed CSNS Input Clamp Current in MAXIMUM RATINGS • Changed Figure 11, Reverse Battery Protection • Removed unnecessary line in Figure 14, Overload on Low-Side Gate Drive, Case 2 • Corrected label in Figure 28, 33981 with Filter

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2007. All rights reserved.

freescale™
semiconductor