High Performance Current Mode PWM Controllers

PL384XAQ8

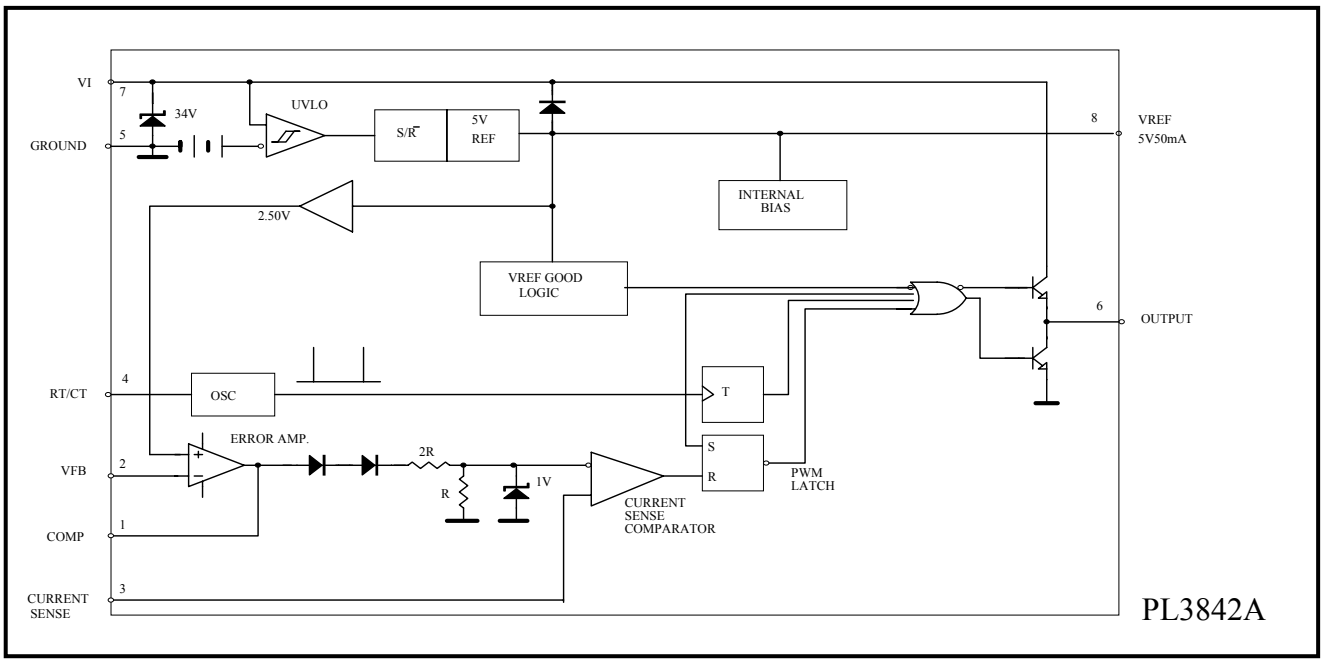
Description

The PL384XAQ8 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, under voltage lockout featuring start-up current less than 1.0mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-channel MOSFETs, is low in the off-state.
Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The PL3842A and PL3844A have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The corresponding thresholds for the PL3843A and PL3845A are 8.5V and 7.9V. The PL3842A and PL3843A can operate to duty cycles approaching 100%. A range of the zero to <50% is obtained by the PL3844A and PL3845A by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

Features

- Trimmed oscillator for precise frequency control
- Oscillator frequency guaranteed at 250 kHz
- Current mode operation to 500kHz
- Automatic feed forward compensation
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up and operating current

Block Diagram(toggle flip flop used only in PL3844A and PL3845A)

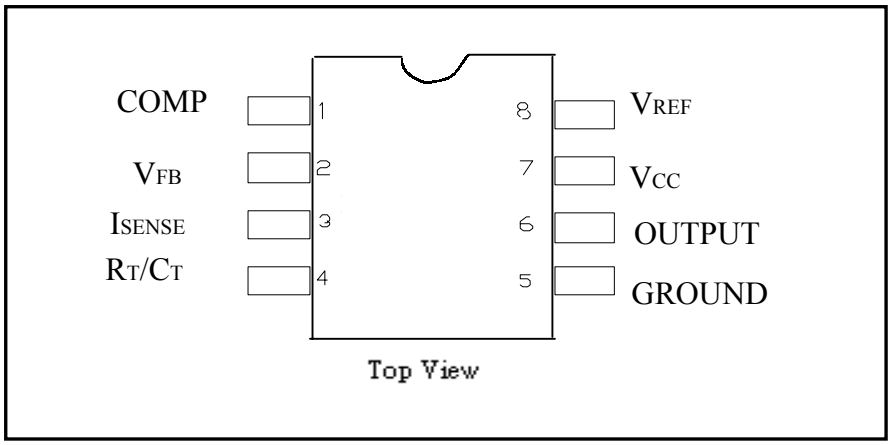


Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	Supply Voltage (low impedance source)	30	V
V_I	Supply Voltage (Ii<30mA)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	-0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
Ptot	Power Dissipation at Tamb≤ 25℃	1.25	W
Tstg	Storage Temperature Range	-65 to +150	℃
T_J	Junction Operating Temperature	-40 to +150	℃
T_L	Lead Temperature (soldering 10s)	300	℃

Note : All voltages are with respect to pin 5, all currents are positive into the specified terminal.

Pin Connection (top view)



Pin Functions

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

Thermal Data

Symbol	Description	Value	Unit
$R_{th, j\text{-}amb}$	Thermal Resistance, junction to ambient	150	℃/W

Electrical Characteristics (〔note 1〕Unless otherwise stated, these specifications apply for $0 \le T_{amb} \le 70℃$, V_i=15V(note 5), R_T=10k, C_T=3.3nF)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Reference Section						
Output Voltage	Tj=25℃, I_O=1mA	V_{REF}	4.9	5.0	5.1	V
Line Regulation	12V ≤ V_I ≤ 25V	ΔV_{REF}	-	2	20	mV
Load Regulation	1mA ≤ I_O ≤ 20mA	ΔV_{REF}	-	3	25	mV
Temperature Stability	(Note 2)	$\Delta V_{REF} / \Delta T$	-	0.2	-	mV/℃
Total Output Variation	Line, Load, Temperature		4.82	-	5.18	V
Output Noise Voltage	10Hz ≤ f ≤10kHz, Tj=25℃ (note 2)	e_N	-	50	-	μV
Long Term Stability	Tamb=125℃, 1000 Hrs (note 2)		-	5	25	mV
Output Short Circuit		I_{SC}	-30	-100	-180	mA
Oscillator Section						
Frequency	Tj=25℃ TA= 0 to 70 ℃ Tj=25℃ (R_T=6.2k, C_T=1nF)	fosc	49 48 225-	52 - 250	55 56 275	kHz kHz kHz
Frequency Change with Volt	V_{CC}=12V to 25V	Δfosc/ΔV	-	0.2	1.0	%
Frequency Change with Temp	T_A= 0 to 70 ℃	Δfosc/ΔT	-	0.5	1.0	%
Oscillator Voltage Swing	Peak to peak	Vosc	-	1.6	-	V
Discharge Current (Vosc=2V)	T_J=25℃ T_A= 0 to 70 ℃	I_{dischg}	7.8 7.6	8.3 -	8.8 8.8	mA mA
Error Amp Section						
Input Voltage	$V_{PIN\,1}$=2.5V	V_2	2.42	2.50	2.58	V
Input Bias Current	V_{FB}=5V	Ib	-	-0.1	-2	μA
A_{VOL}	2V ≤ Vo ≤ 4V		65	90	-	dB
Unity Gain Bandwidth	T_J = 25℃	BW	0.7	1	-	MHz
Power Supply Rejec. Ratio	V_I = 12V to 25V	PSRR	60	70	-	dB
Output Sink Current	$V_{PIN\,2}$ = 2.7V, $V_{PIN\,1}$ = 1.1V	I_O	2	12	-	mA
Output Source Current	$V_{PIN\,2}$ = 2.3V, $V_{PIN\,1}$ = 5V	I_O	-0.5	-1	-	mA
V_{OUT} High	$V_{PIN\,2}$ = 2.3V, R_L = 15kΩ to ground		5	6.2	-	V
V_{OUT} Low	$V_{PIN\,2}$ = 2.7V, R_L = 15kΩ to Pin 8		-	0.8	1.1	V
Current Sense Section						
Gain	(note 3 & 4)	G_V	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\,1}$ = 5V (note 3)	V_3	0.9	1	1.1	V
Supply Voltage Rejection	12V ≤ V_I ≤ 25V	SVR	-	70	-	dB
Input Bias Current		Ib	-	-2	-10	μA
Delay to Output			-	150	300	ns
Output Section						
Output Low Level	I_{SINK} = 20mA	V_{OL}	-	0.1	0.4	V
	I_{SINK} = 200mA		-	1.6	2.2	V
Output High Level	I_{SOURCE} = 20mA	V_{OH}	13	13.5	-	V
	I_{SOURCE} = 200mA		12	13.5	-	V
UVLO Saturation	V_{CC} = 6V, I_{SINK} = 1mA	V_{OLS}	-	0.1	1.1	V
Rise Time	Tj=25℃, C_L=1nF (note 2)	tr	-	50	150	ns
Fall Time	Tj=25℃, C_L=1nF (note 2)	tf	-	50	150	ns

Electrical Characteristics (continued)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Undervoltage Lockout Section						
Start Threshold	PL3842A/PL3844A		14.5	16	17.5	V
	PL3843A/PL3845A		7.8	8.4	9.0	V
Min Operating Voltage After Turn-on	PL3842A/PL3844A PL3843A/PL3845A		8.5 7.0	10 7.6	11.5 8.2	V
PWM Section						
Maximum Duty Cycle	PL3842A/PL3843A		94	96	100	%
	PL3844A/PL3845A		47	48	50	%
Minimum Duty Cycle			-	-	0	%
Total Standby Current						
Start-up Current	V_I=6.5V for PL3843A/45A	Ist	-	0.17	0.3	mA
	V_I=14V for PL3842A/44A		-	0.17	0.3	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3}$ = 0V	I_I	-	12	17	mA
Zener Voltage	I_I = 25 mA	V_{IZ}	30	38	-	V

Notes: 1. Max. package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain Tj as close to Tamb as possible.

2.These parameters, although guaranteed, are not 100% tested in production.

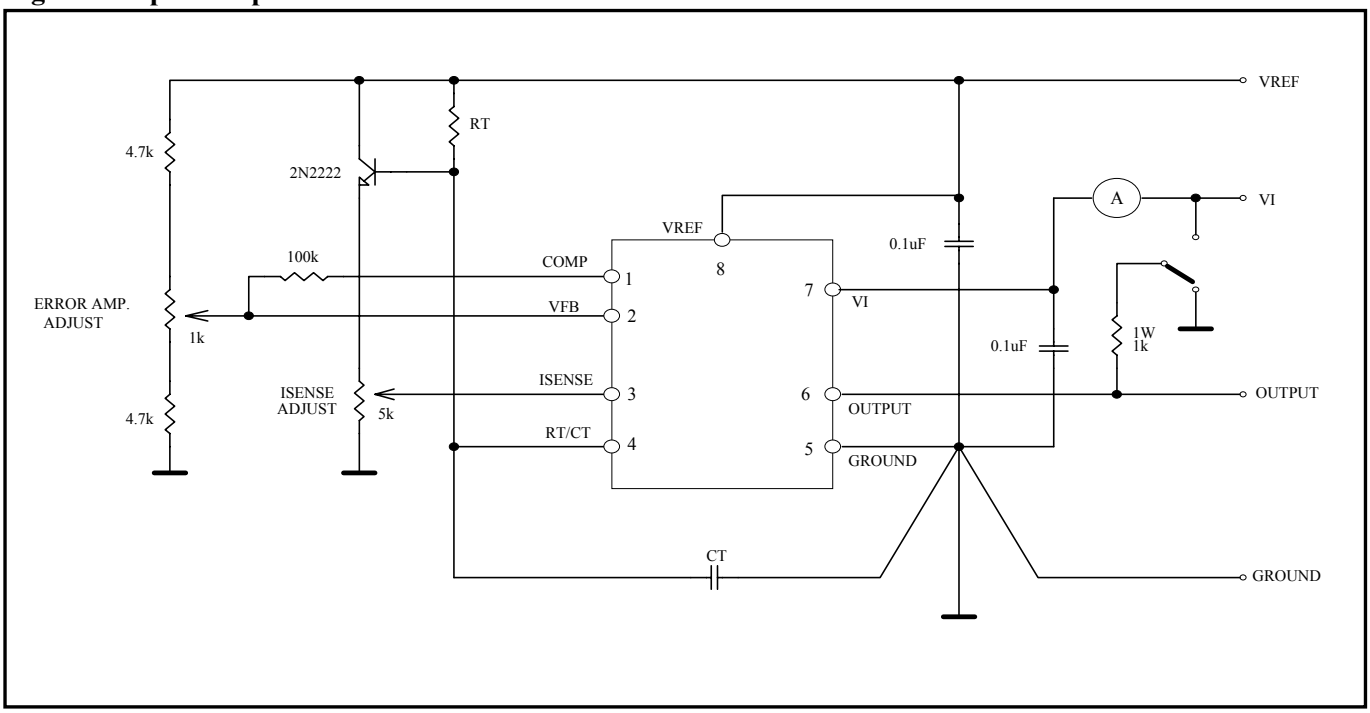
3.Parameter measured at trip point of latch with $V_{PIN\ 2}$= 0 .

4.Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}, \quad 0 \le V_{PIN\ 3} \le 0.8V$$

5. Adjust V_I above the start threshold before setting at 15V.

Figure 1: Open Loop Test Circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 2:Timing Resistor vs Oscillator Frequency

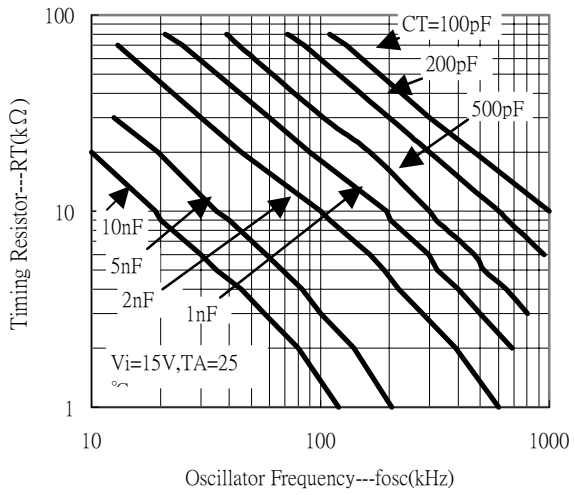


Figure 3:Output Dead-Time vs Oscillator Frequency

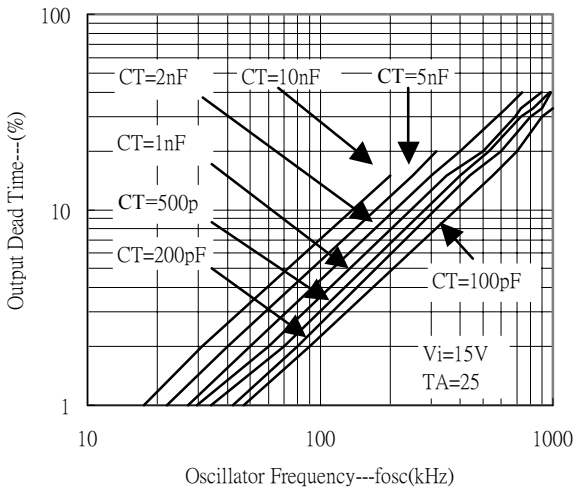


Figure 4:Oscillator Discharge Current vs Temperature

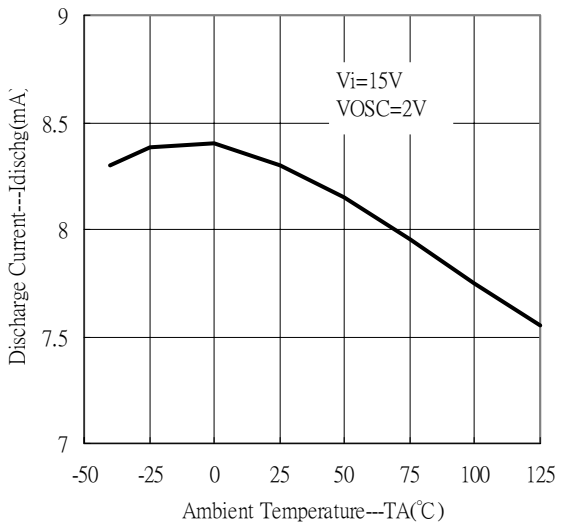


Figure 5:Maximum Output Duty Cycle vs Timing Resistor

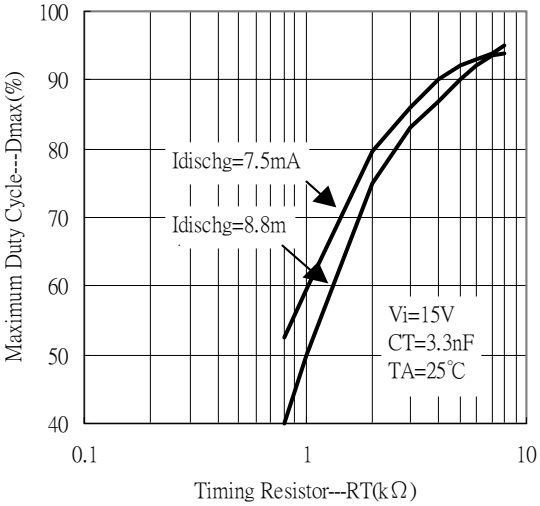


Figure 6:Error Amp Open-Loop Gain vs Frequency

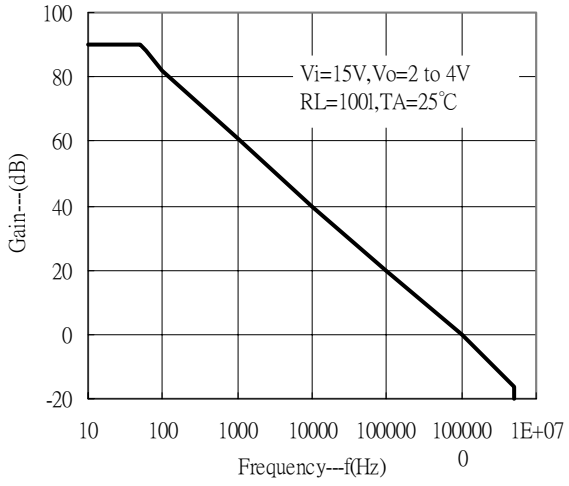


Figure 7:Error Amp Phase vs Frequency

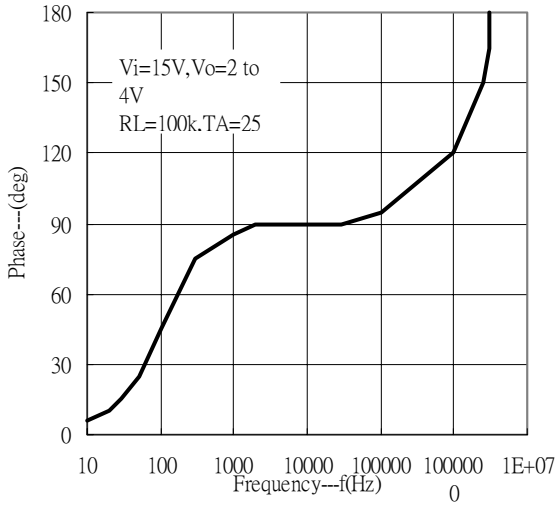


Figure 8:Current Sense Input Threshold vs Error Amp Output Voltage

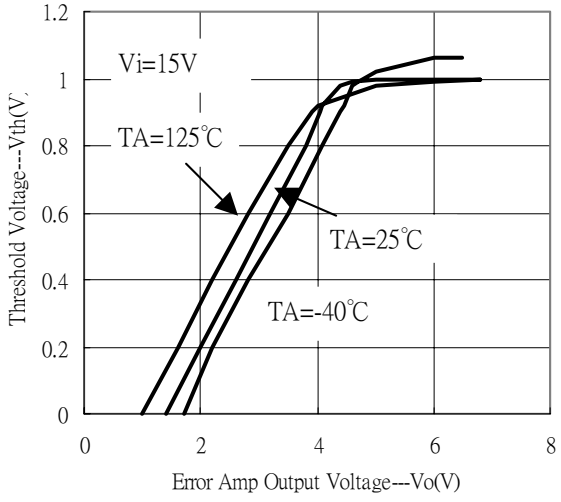


Figure 9:Reference Short Circuit Current vs Temperature

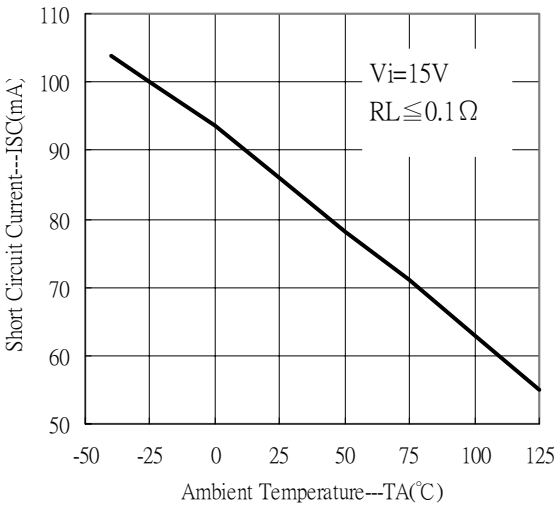


Figure 10.Oscillator and Output Waveforms

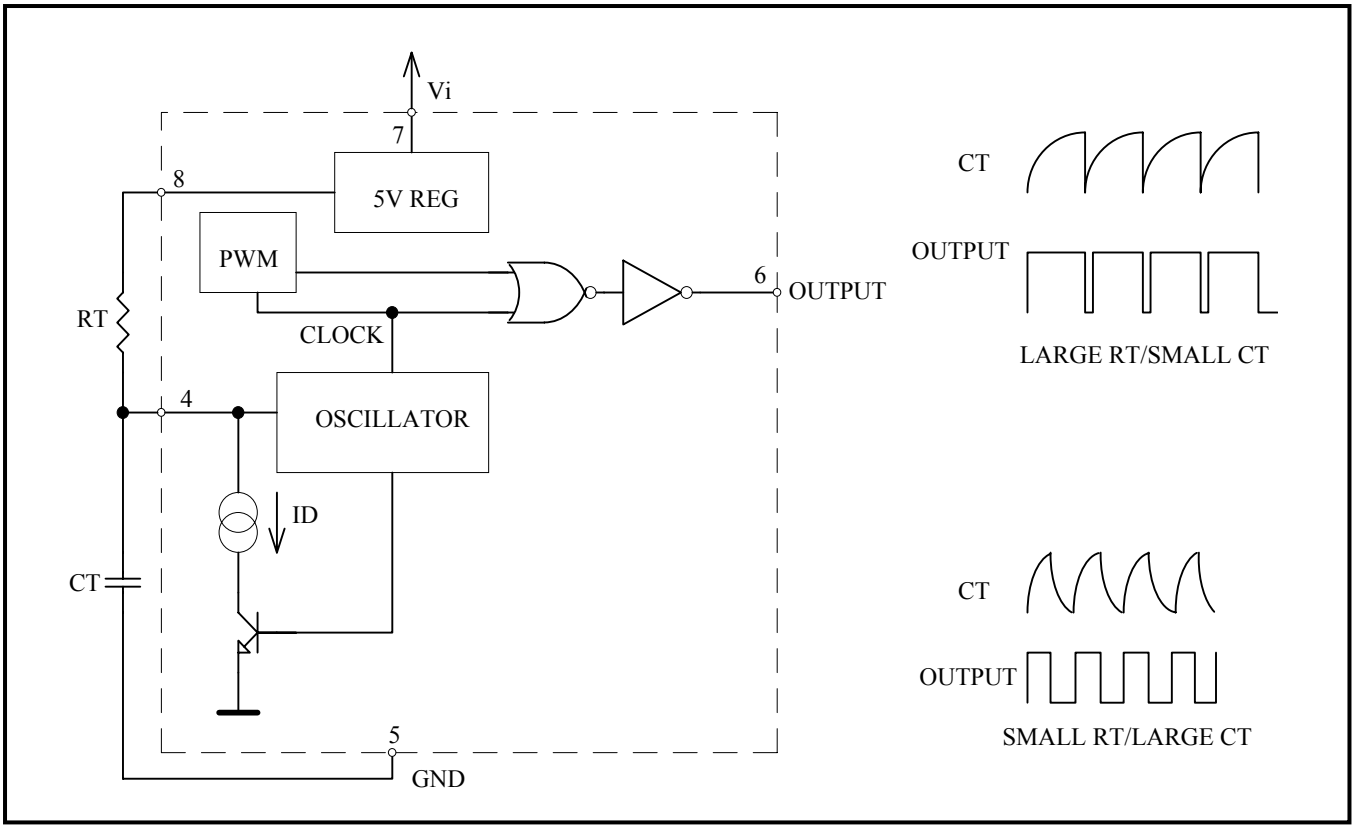


Figure 11:Error Amp Configuration

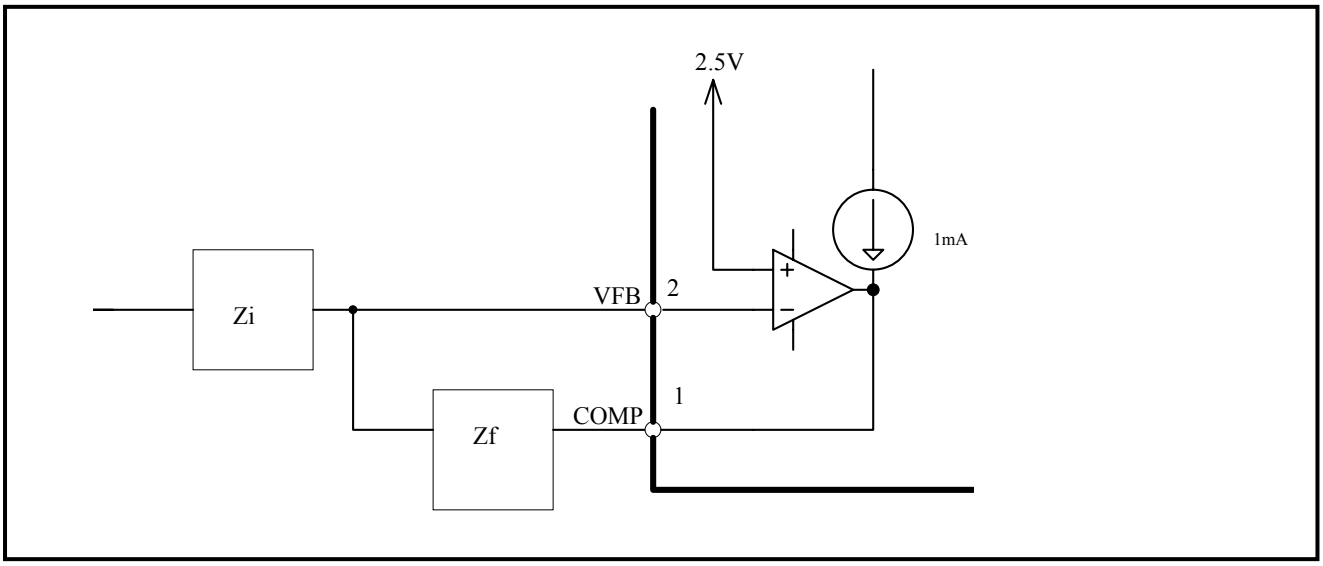
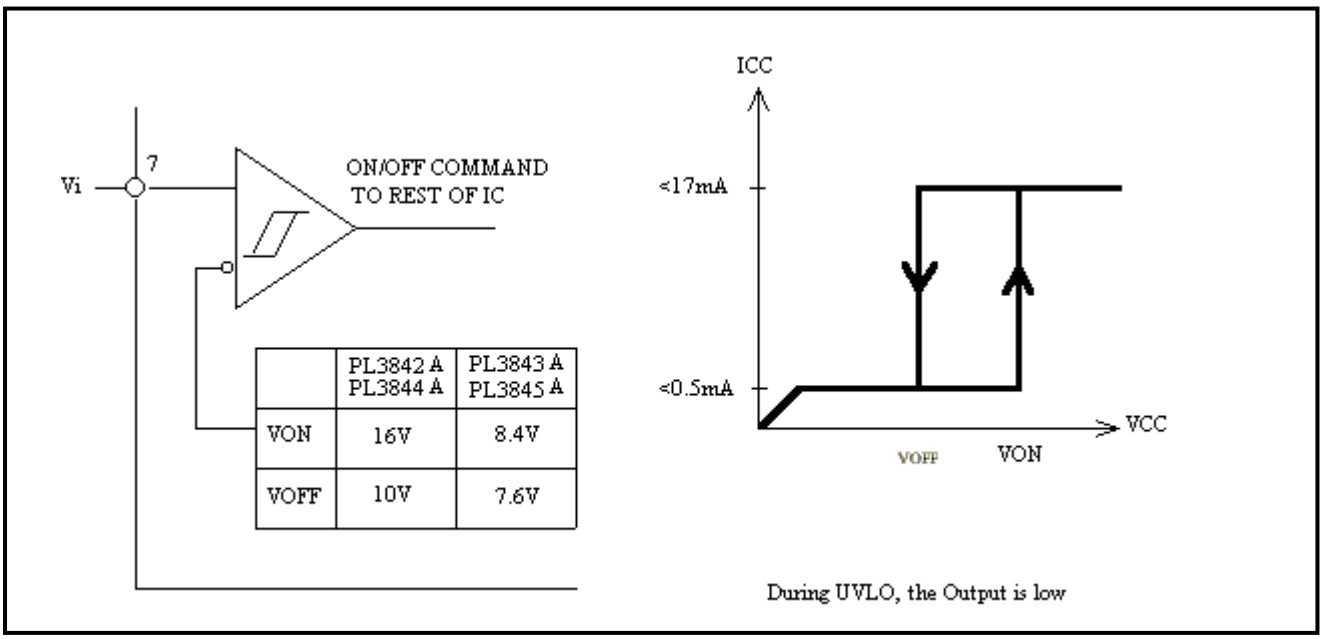
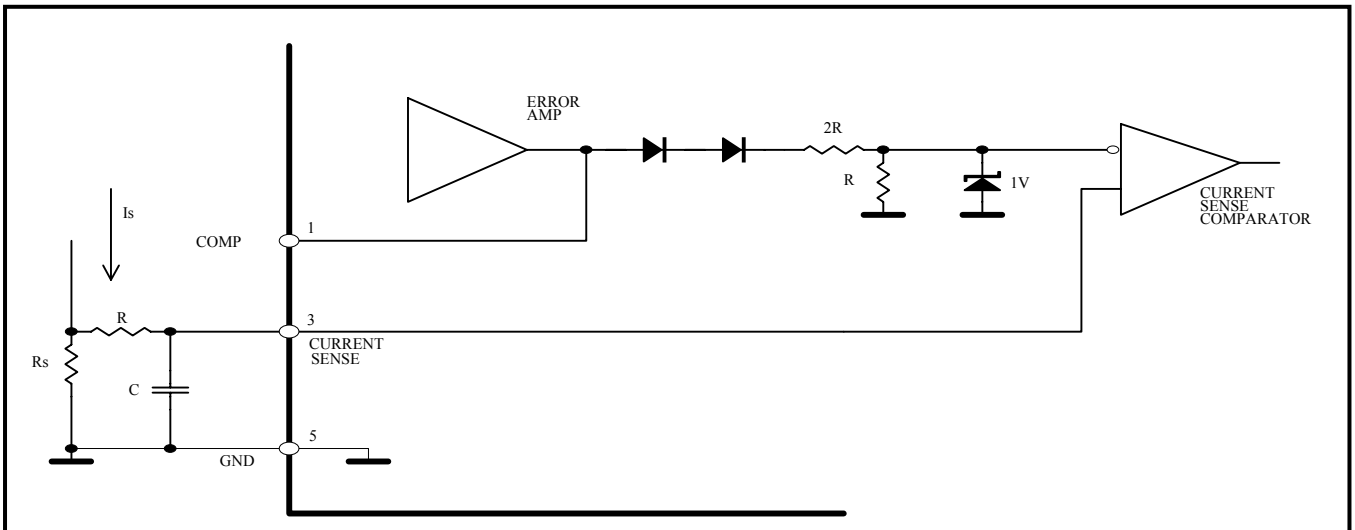


Figure 12:Under Voltage Lockout



	PL3842 A PL3844 A	PL3843 A PL3845 A
VON	16V	8.4V
VOFF	10V	7.6V

Figure 13:Current Sense Circuit



Peak Current (i_S) is determined by the formula

$I_{S\,max} \approx 1.0V/Rs$

A small RC filter may be required to suppress switch transients.

Figure 14:Slope Compensation Techniques.

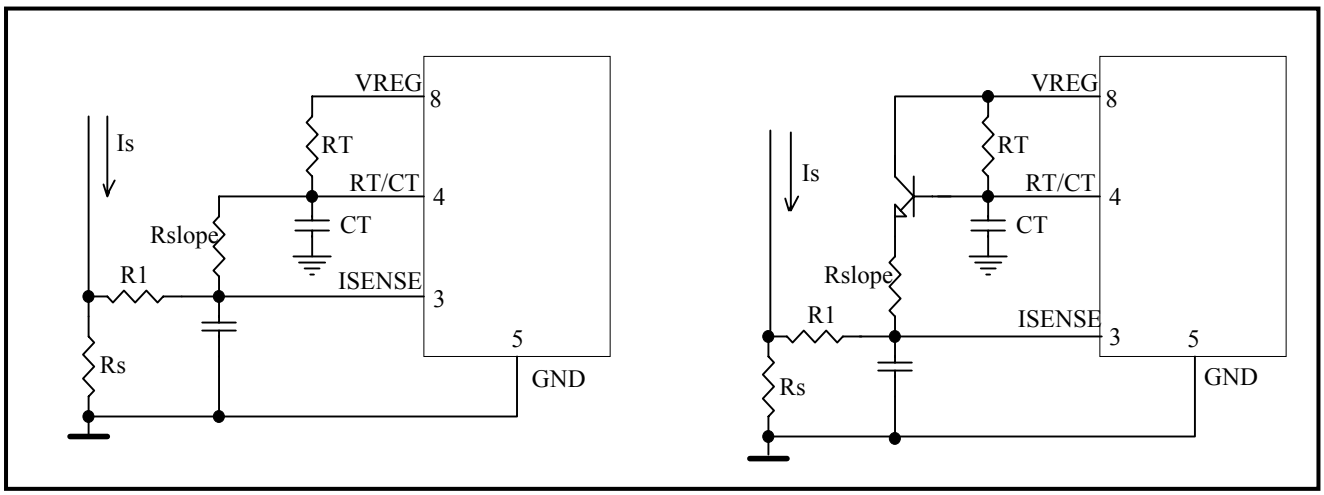


Figure 15:Isolated MOSFET Drive and Current Transformer Sensing

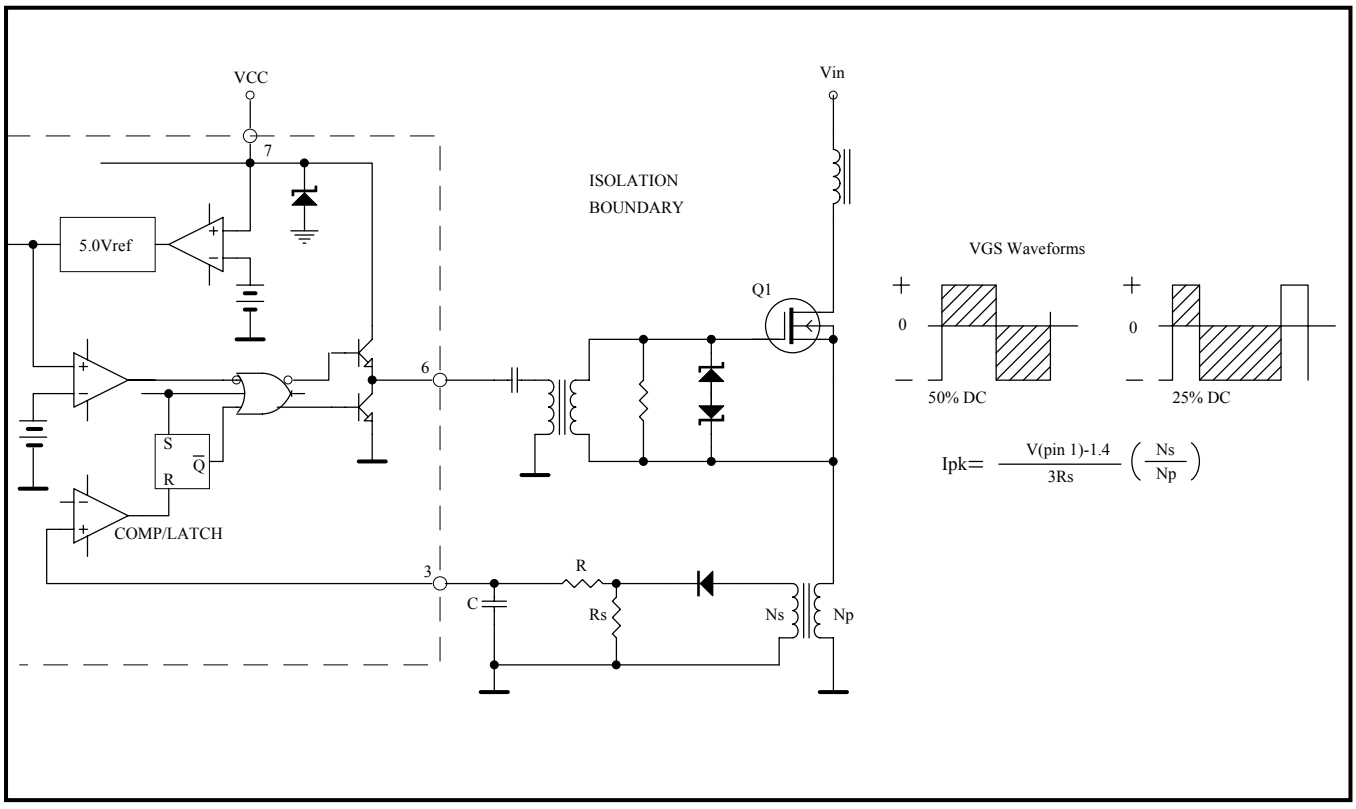
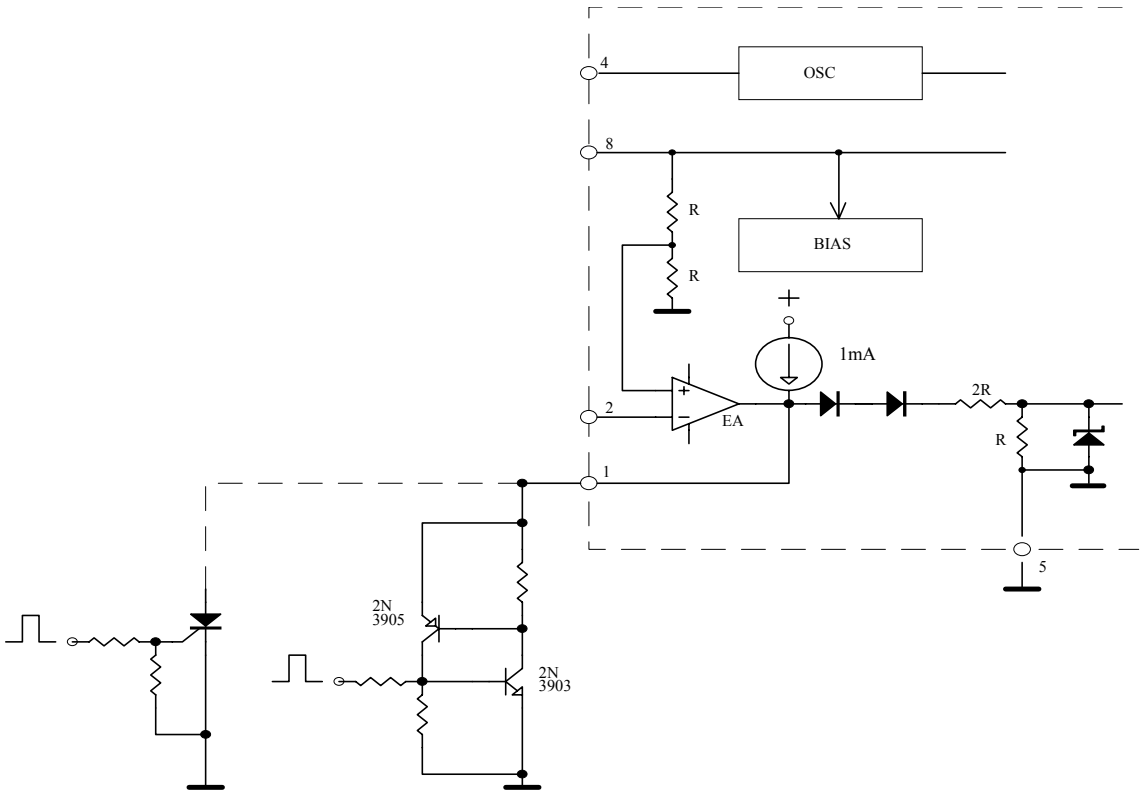
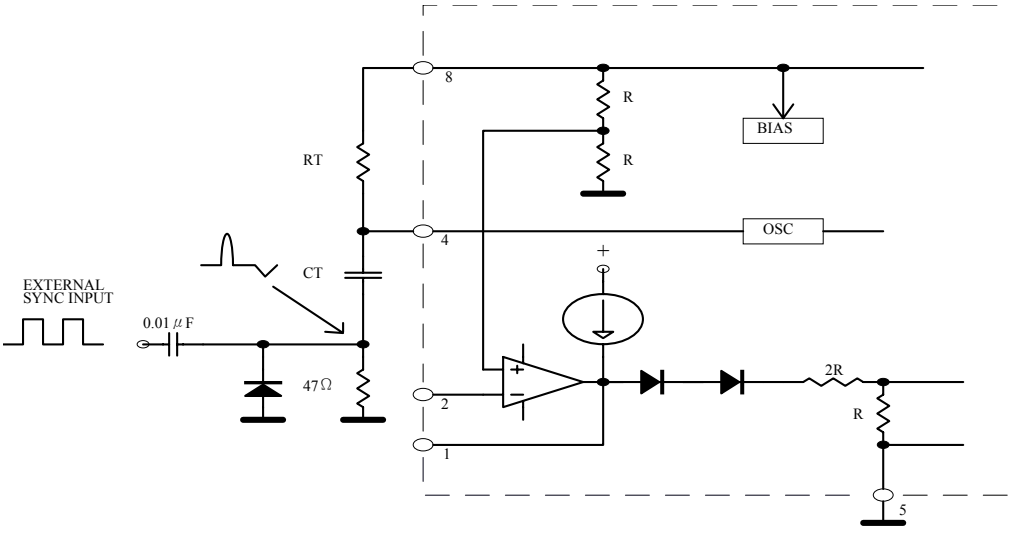


Figure 16:Latched Shutdown



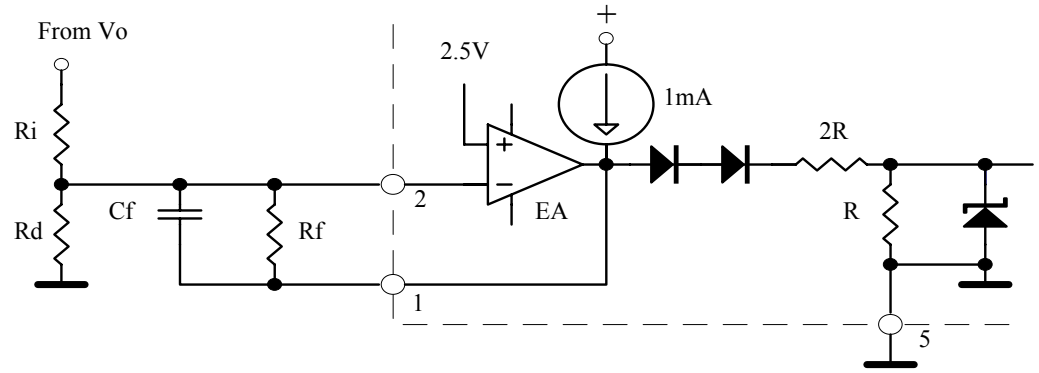
SCR must be selected for a holding current of less than 0.5mA at TA(min).
The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

Figure 17:External Clock Synchronization

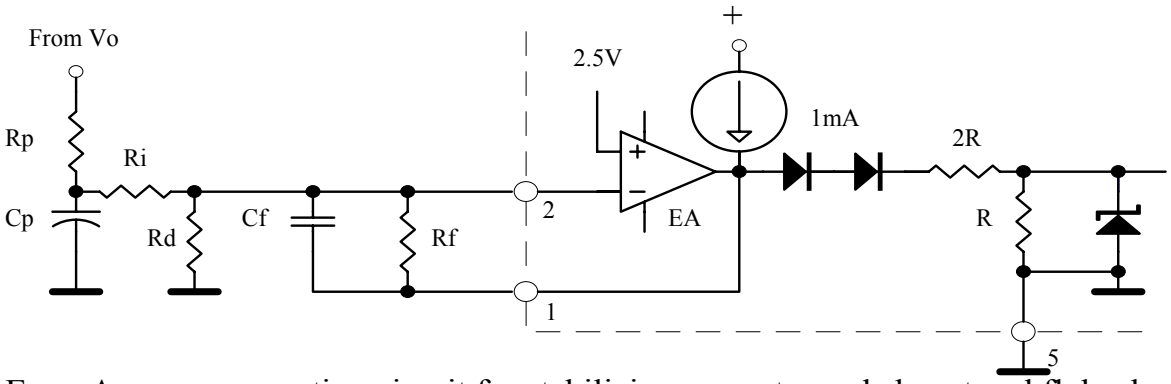


The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300mV below ground.

Figure 18: **Error Amplifier Compensation**



Error Amp compensation circuit for stabilizing any current -mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current--mode boost and flyback

Figure 19:External Duty Cycle Clamp and Multi Unit Synchronization

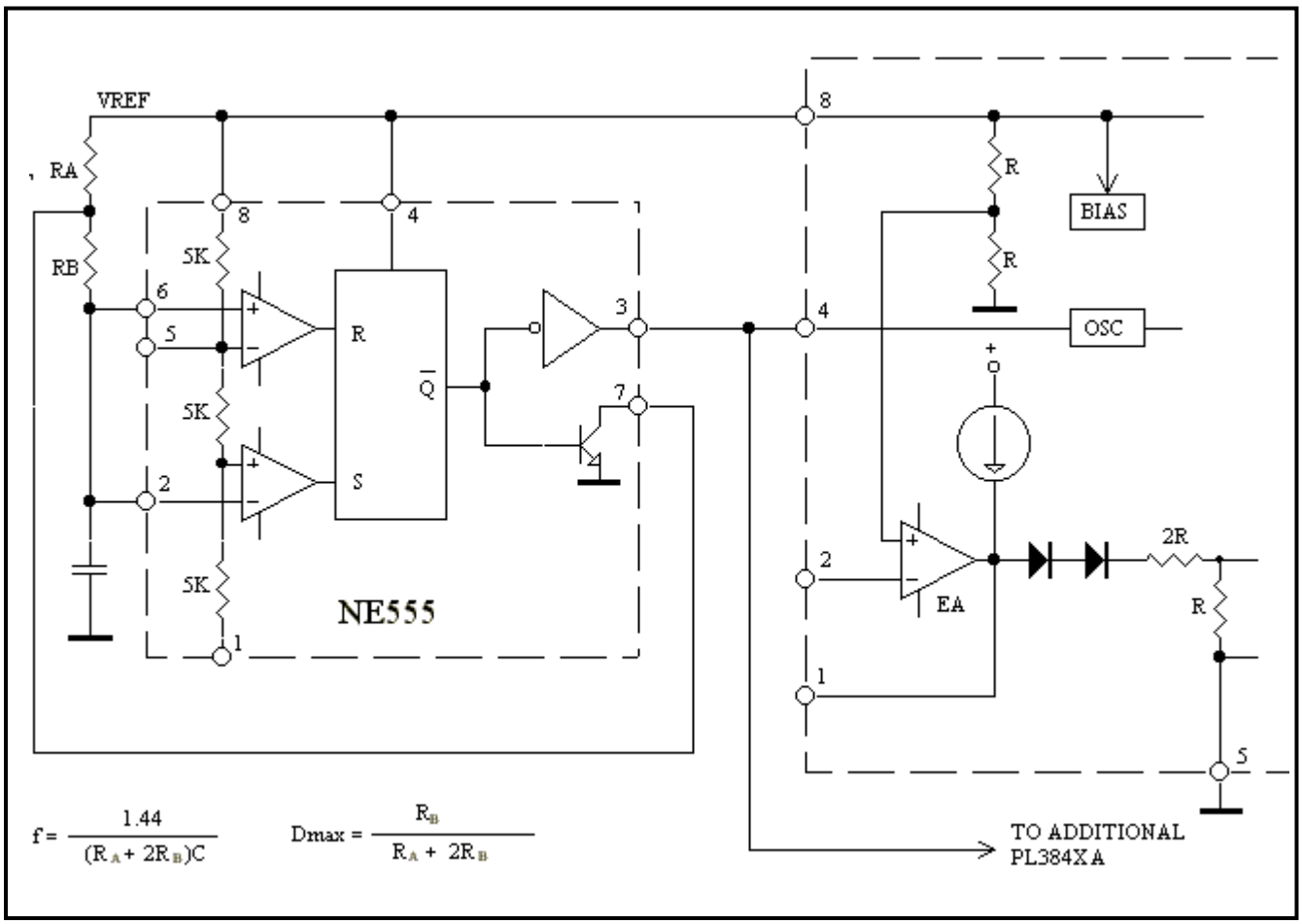


Figure 20:Soft-Start Circuit

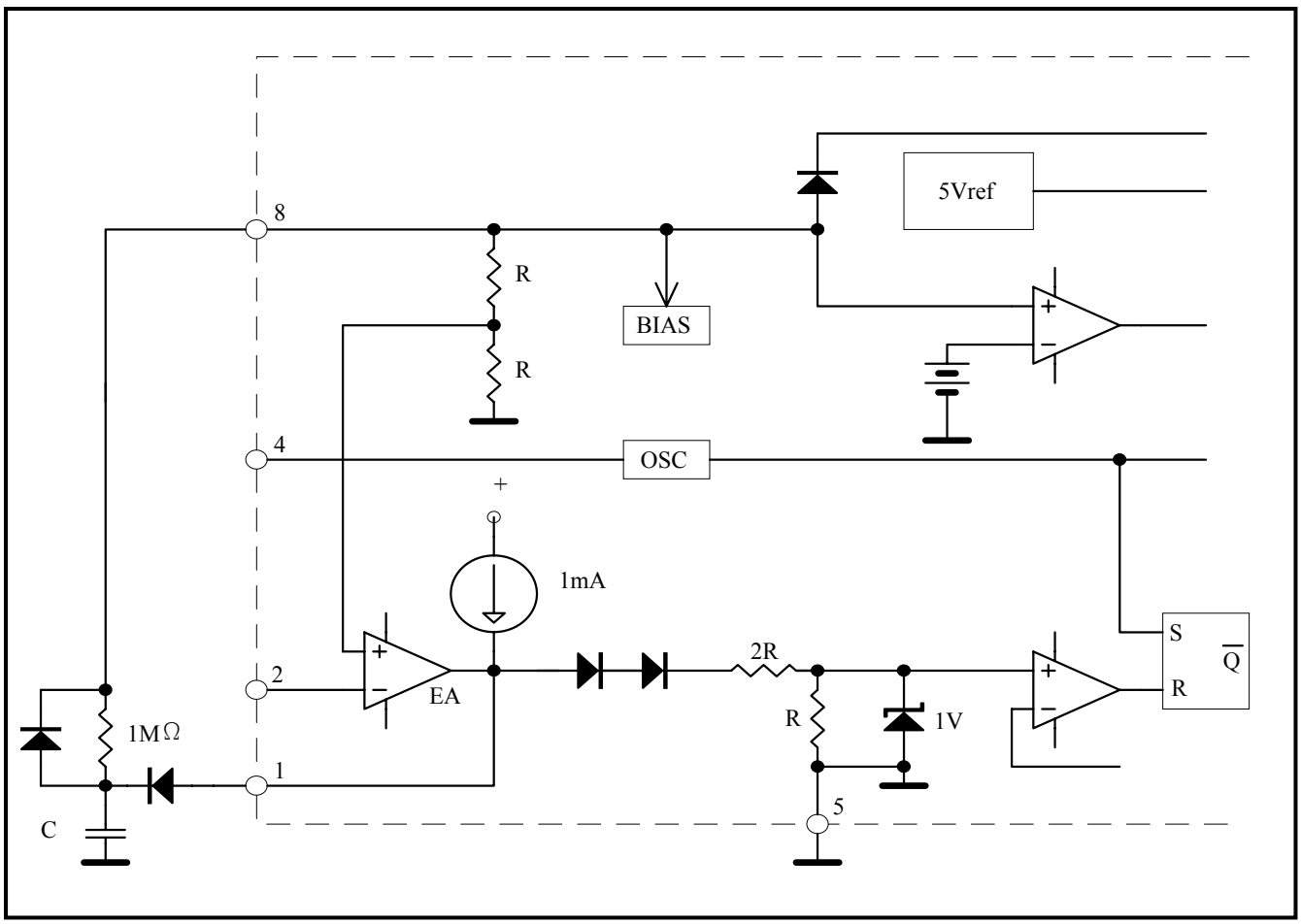
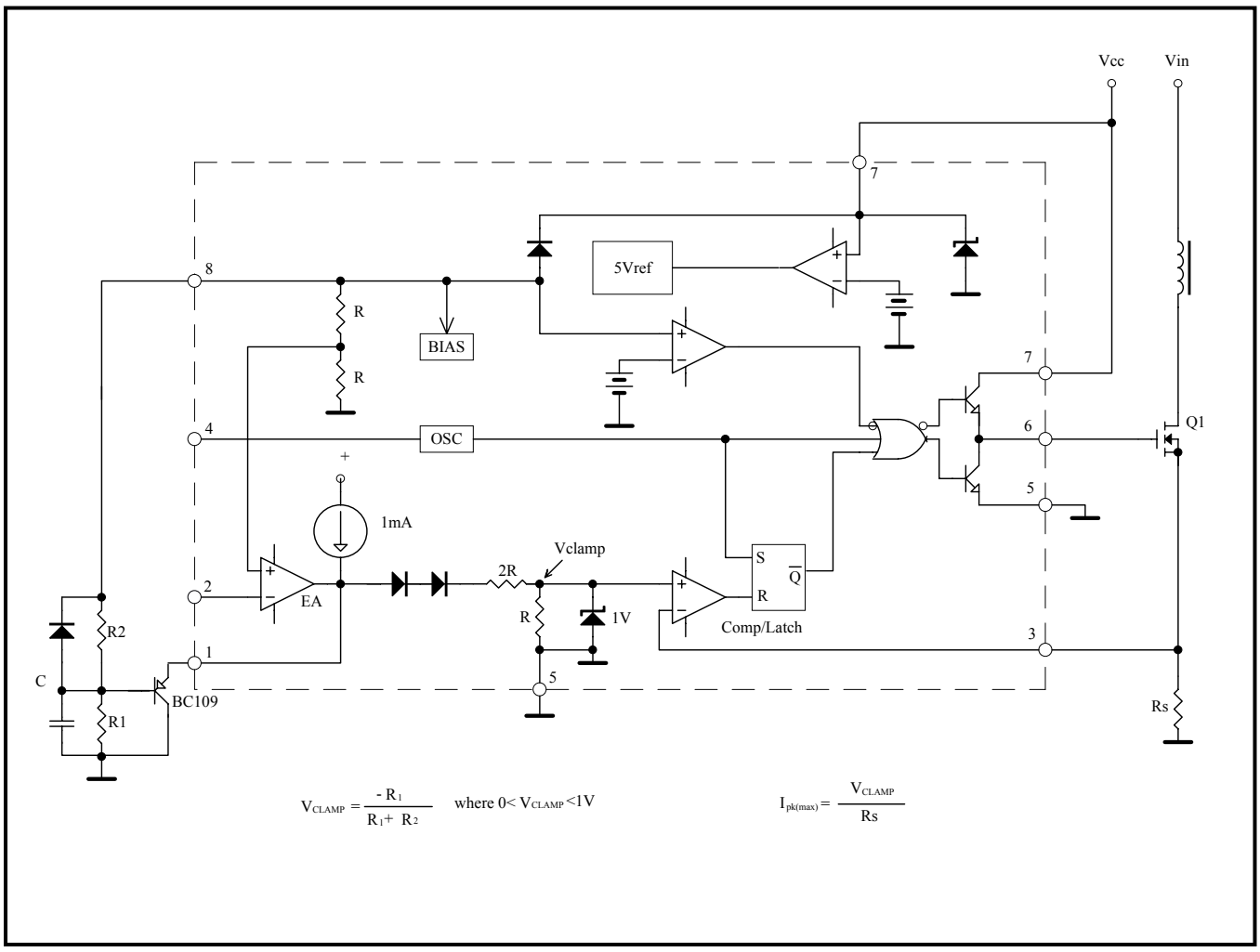
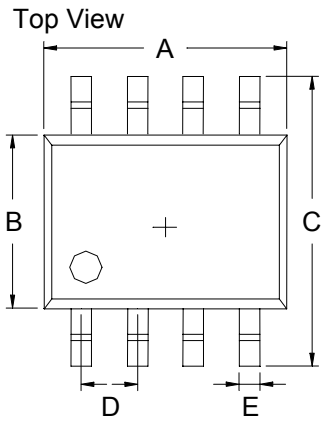
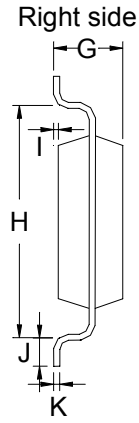


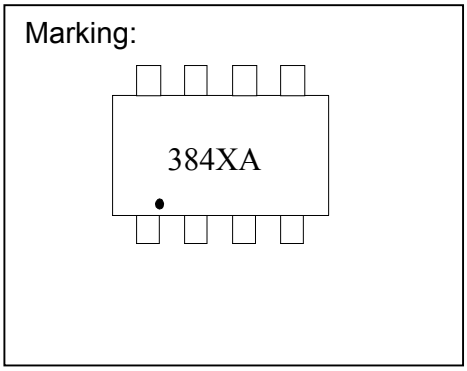
Figure 21:Soft-Start and Error Amplifier Output Duty Cycle Clamp.

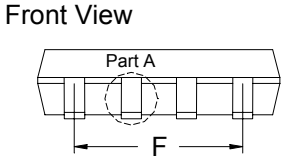


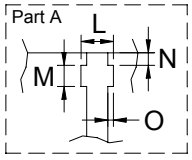
SO-8 Dimension











8-Lead SO-8 Plastic Package
CYStek Package Code: Q8

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0