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KESRX05

260 to 470MHz ASK Receiver with Power Down

Preliminary Information

DS5023 Issue 1.9 August 1999

Features

- In-band Interference Rejection 20dB max.
- −103dBm Sensitivity (IF BW = 470kHz)
- AGC around LNA and Mixer
- Low Supply voltage (3 to 6V)
- 2-Stage Power Down for Low Current Applications
- Interface for Ceramic IF Filters up to 15MHz
- All Pins Meet 2kV Human Body Model ESD Protection Requirement
- Compliant to ETS 300-220 and FCC Part 15

Applications

- Remote Keyless Entry
- Security, tagging
- Remote Controlled equipment

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0·5V to +7V
Storage temperature, T_{stg}	−55°C to 150°C
Junction temperature, T_j	−55°C to 150°C
RF input power	+20dBm from 50Ω

Ordering Information

KESRX05B/KG/QP1S (anti-static tubes)
KESRX05B/KG/QP1T (tape and reel)

The KESRX05 is a single chip ASK (Amplitude Shift Key) Receiver IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control, RF tagging and local paging systems.

The receiver offers an exceptionally high level of integration and performance to meet the local oscillator radiation requirements of regulatory authorities world wide. Functionally the device works in the same way as the KESRX01 with the added features of low supply voltage, in-band interference rejection (anti-jamming detector), a 2-stage power down to enable receiver systems to be implemented with less than 1mA supply, and a wide IF bandwidth and drive stage to interface to an external ceramic IF bandpass filter at intermediate frequencies from 0·2MHz to 15MHz.

The KESRX05 is an ideal receiver for difficult reception areas where high level interferers would jam the wanted signal. The anti-jamming circuit allows operation to be possible with interfering signals which are more than 20dB stronger than the wanted signal, without the cost penalties of increased IF selectivity and frequency accuracy.

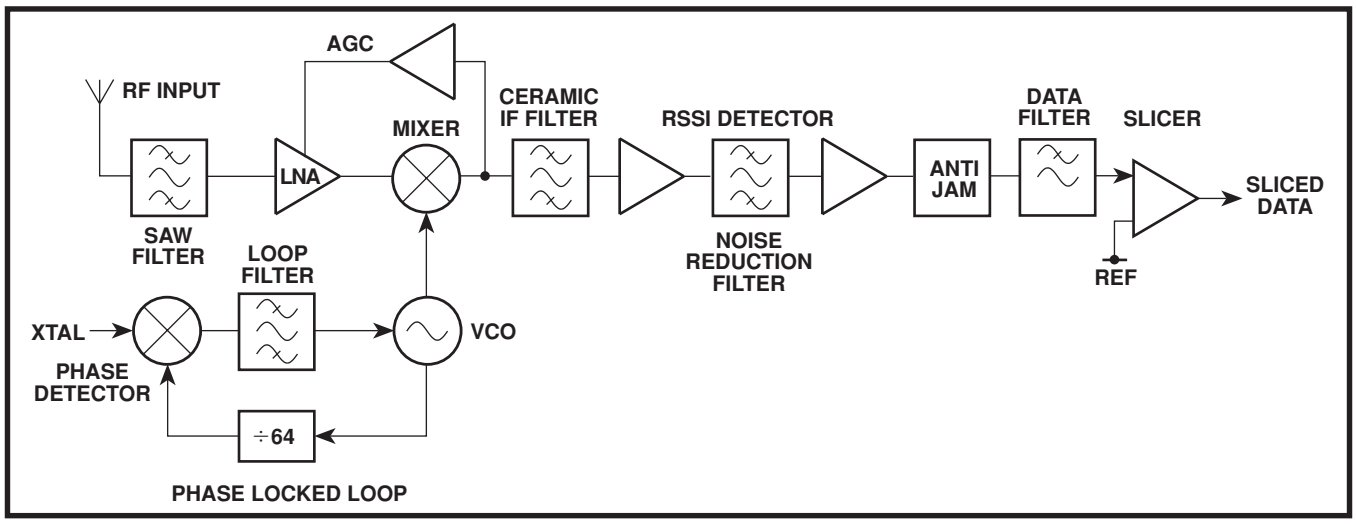


Figure 1 Typical system application

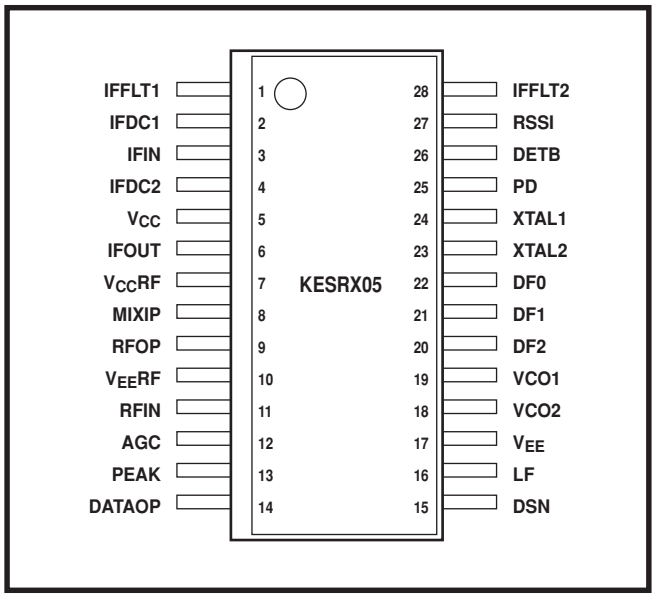


Figure 2 Pin connections (top view)

DESCRIPTION

The single conversion superheterodyne receiver approach is now generally considered the way forward for ISM band type applications because of lower cost, superior selectivity, lower radiation, and flexibility over other techniques. For power-conscious, hand-held applications KESRX05 provides improved performance and flexibility on a lower 3·0V supply and a power down feature allows faster switch-on times for use in a pulsed power saving mode.

Although this is a relatively simple receiver, the flexibility of using an external IF filter allows the designer to choose both the selectivity and the IF in order to optimise the performance for a wide range of applications and locations world wide.

The KESRX05, with its anti-jamming detector circuit, is an ideal ASK/ OOK receiver for difficult reception areas caused by interference such as amateur radio repeater stations and wireless stereo headphones. Operation is possible with interfering signals which are more than 20dB stronger than the wanted signal (IF bandwidth = 470kHz.), without the cost penalities of increased IF selectivity and frequency accuracy.

Figure 1 is the system block diagram, with an external ceramic IF filter, SAW fillter and noise reduction filter.

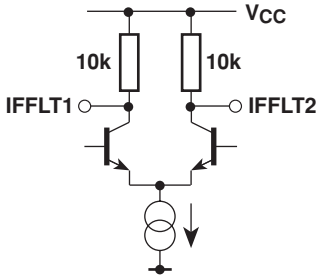
Pin	Name	Function	Schematic
1	IFFLT1	**Noise reducing IF filter** A simple LC noise reduction filter (L5 and C7) is connected between pins 1 (IFFLT1) and 28 (IFFLT2) to reduce the noise contribution from the earlier stages of the logathrimic amplifier. The LC filter helps to reduce the bandwidth of the log amplifier from approximately 45MHz to typically 1MHz, preventing wideband noise from being detected as a signal. To reduce the Q of the simple LC circuit, an external damping resistor in parallel with L5, C7. However, the preferred method to a damping resistor is to lower the Q of L5 or increase the tolerances of L5 and C7. For further information refer to the IF Amp /RSSI Detector section of the Functional Description.	

Table 1 Pin descriptions **Cont…**

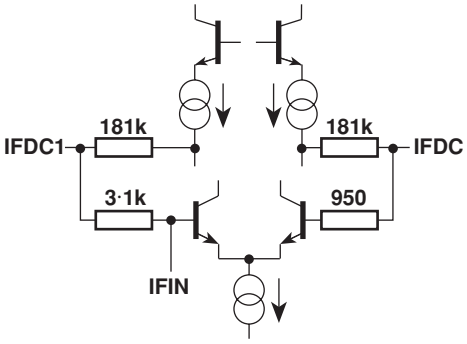
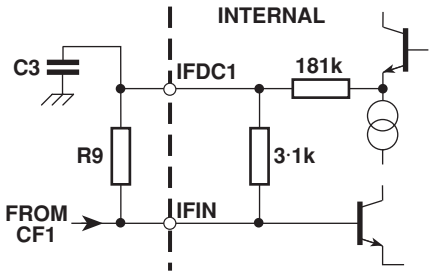
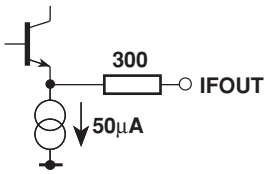
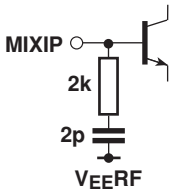
Pin	Name	Function	Schematic
2	IFDC1	**Log Amplifier DC Blocking Capacitor** Capacitors C3 and C4 provide DC blocking within the high gain stage of the log amplifier. The log amplifier has a small gain of greater than 80dB between pins 3 (IFIN) and 27 (RSSI output) Capacitors C3 and C4 eliminate DC offsets, allowing the amplification of AC signals only. For further information, refer to the IF Amp/RSSI Detector section of the Functional Description.	
3	IFIN	**Log Amp Input (IFamplifier input)** The bandwidth of KESRX05 is set by the external ceramic filter CF1. Impedance matching from the output of the ceramic filter to the input of the log amplifier is achieved by an external shunt resistor R9 in parallel with an internal resistor. For further information please refer to the IF Interface section of the Functional Description.	 **Matching circuit for CF1**
4	IFDC2	Log amplifier DC stability capacitor	See pin 2
5	V_{CC}	Positive supply	
6	IFOUT	**IF output** The IF output drive is a voltage drive with a low output impedance of 300Ω via an internal series resistor. The IFOUT pin is designed for direct connection to an external 10·7MHz FM ceramic filter with a typical input impedance of 300Ω. For further information refer to the IF Interface section of the Functional Description.	
7	V_{CC}RF	Positive supply for RF circuits	
8	MIXIP	**Mixer input** To a first order approximation the input impedance of the mixer at UHF frequencies is set by the internal bias resistor and capacitor network. Effects of internal and external stray parasitics ignored. For further information refer to the AC Electrical Characteristics.	

Table 1 Pin descriptions (continued)

Cont…

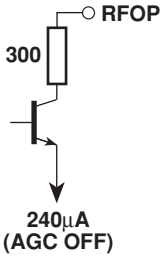
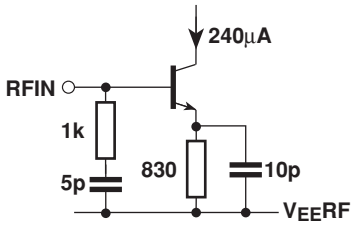
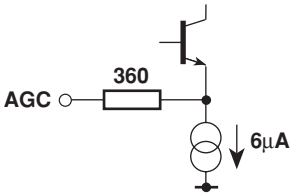
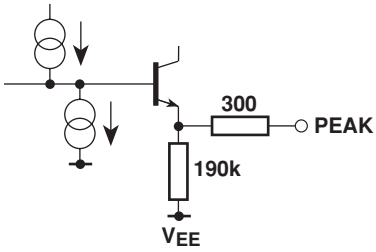
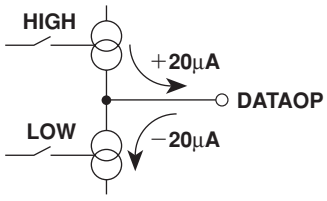
Pin	Name	Function	Schematic
9	RFOUT	**Output from internal RF amplifier** The RF amplifier has a high output impedance. The internal 300Ω resistor is used to improve the ESD protection of RFOUT. For further information refer to the AC Electrical Characteristics.	
10	V_{EE}RF	Negative supply for RF circuits	
11	RFIN	**nternal input RF amplifier** To a first order approximation the input impedance of the RF amplifier at UHF frequencies is set by the internal bias resistor and capacitor network. Effects of internal and external stray parasitics ignored. For further information please refer to the AC Electrical Characteristics.	
12	AGC	**RF AGC time constant** The attack and decay time constant of the AGC is set by the internal series resistor, current sink and the external capacitor C8. Increasing the decay time constant of the AGC circuit will impair the time to good data of the receiver from power up PD0 to PD2. For further information please refer to the IF Amp/ RSSI Detector section of the Functional Description.	
13	PEAK	**Data signal peak detector output** The peak detector output is designed to be a low impedance output. The peak detector monitors the peak of the signal at pin 20 (DF2). For further information please refer to the Baseband section of the Functional Description.	
14	DATAOP	**Sliced data output** The data output is the inverted sense of the input signal at pin 20 (DF2) and is designed as a high impedance output via two internal sink and source current generators	

Table 1 Pin descriptions (continued)

Cont…

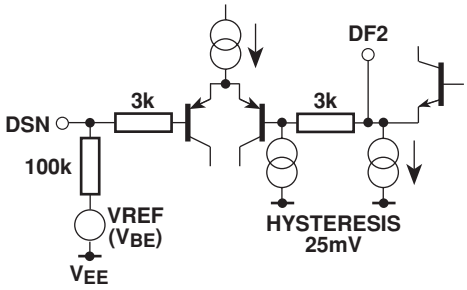
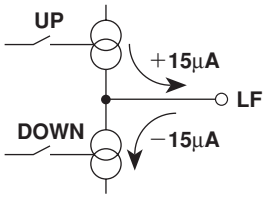
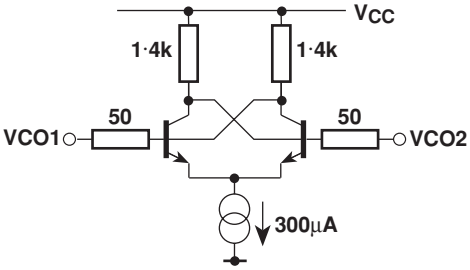
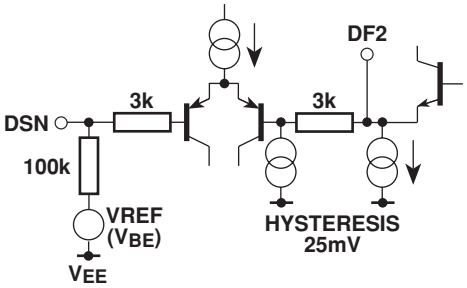
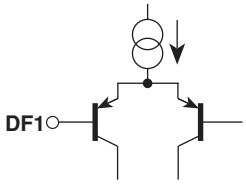
Pin	Name	Function	Schematic
15	DSN	**Data slice reference level** The DSN pin is defined internally by the Slice voltage V_{REF}. The DSN slice voltage can be offset from the internal reference V_{REF} by connecting a resistor from the DSN pin to V_{EE} and/or the peak detector output. For further information please refer to the Baseband section of the Functional Description.	
16	LF	**PLL loop filter connection** The phase detector output current is derived by two internal current sources. The nominal linear average output current is +15µA (5µA/radian). For further information please refer to the Phase Lock Loop VCO section of the Functional Description	
17	V_{EE}	Negative supply	
18	VCO2	**Voltage controlled oscillator** The voltage controlled oscillator circuit is designed from two cross coupled transistors. The centre frequency of the VCO is set by the external tank circuit. For further information please refer to the Voltage Controlled Oscillator (VCO) Circuit Design / Layout section of the Functional Description	
19	VCO1	**Voltage controlled oscillator**	See pin 18
20	DF2	**Data Filter Output** The data filter is configured as a unity gain amplifier with a low impedance output. Tracking of the received baseband signal is achieved by an internal current source. For further information please refer to the Baseband section of the Functional description.	
21	DF1	**Data filter input** Input to data filter. Bandwidth of second order Sallen and Key data filter is set by external components R10, R1 1, C5 and C6. For further information please refer to the Baseband section of the Functional Description.	

Table 1 Pin descriptions (continued)

Cont…

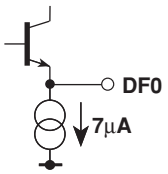
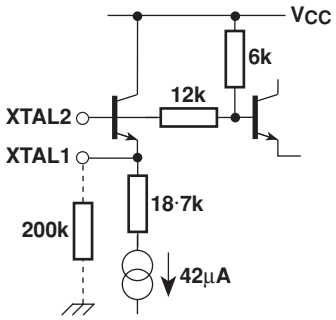
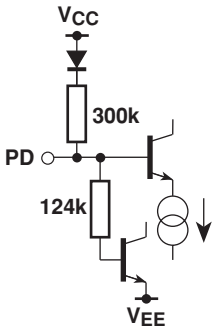
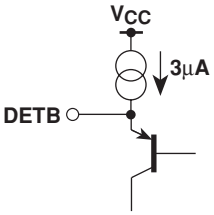
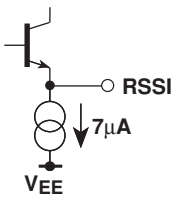
Pin	Name	Function	Schematic
22	DF0	**Anti-jam detector circuit output**	
23	XTAL2	**Crystal oscillator input** This pin is directly connected to the base of the Colpitts oscillator input transistor. The value of the feedback capacitors C13, C14 connected between XTAL1 and XTAL2 are set by the parallel load capacitance of the external crystal. Connecting a 200kΩ resistor from XTAL 1 to ground (in parallel with C14) will maintain oscillation of the crystal in PD0 mode but increase the receiver current consumption by approx 20µA.	
24	XTAL1	**Crystal oscillator input**	See pin 23
25	PD	**Power down input** This tristate input pin is designed to power-up the device in two modes PD0 to PD2 and PD1 to PD2. For further information please refer to the Functional Description.	
26	DETB	**Anti-jam detector input** DETB input is configured as a high impedance input where the signal is DC restored on the peak of the signal, with the aid of capacitor C10. For further information please refer to the Anti Jamming Circuit	
27	RSSI	**RSSI output** The RSSI output is configured as a low impedance output. Tracking of the receive baseband signal is achieved by an internal current source. See pins 3 and 11. For further information please refer to IF Amp/RSSI Detector	
28	IFFLT2	**Noise reducing IF filter**	See pin 1

Table 1 Pin descriptions (continued)

Electrical Characteristics – Test Conditions

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: T_{AMB} = −40°C to +105°C, V_{CC} = 3·0V to 6·0V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	3·0		6·0	V	
Ambient temperature	T_{AMB}	−40		+105	°C	
Test frequency			470		MHz	Local oscillator frequency configured for high side injection, except where otherwise specified (Note 9)
Local oscillator frequency	VCO		480·7	550 470	MHz MHz	−40°C to +85°C −40°C to +105°C

DC Electrical Characteristics

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: T_{AMB} = −40°C to +105°C, V_{CC} = 3·0V to 6·0V, application circuit Figure 25

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Current						
Receive mode (PD2)	I_{CC}		3·9	5·5	mA	All. PD = high, RF input <−50dBm (Figure 24)
Power down 1 (PD1)	I_{CC1}		0·35	0·55	mA	All. PD = V_{CC}/2 or high impedance source V_{CC} = 3·0V to 6·0V (Note 4 and Figure 20)
Power down 2 (PD0)	I_{CC2}		29	57	µA	All. PD = V_{EE} (Figure 22)

AC Electrical Characteristics (1)

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: T_{AMB} = −40°C to +105°C, V_{CC} = 3·0V to 6·0V, application circuit Figure 25

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input frequency range	f_S	260		470	MHz	All (Notes 9 and 10)
Intermediate frequency	IF	0·2		15	MHz	All (Notes 8 and 11)
Test fixture functionality	$V_{IN(MIN)}$		8·0 (−89)	23 (−80)	µVrms (dBm)	20kb/s data rate at 470MHz (Note 1)
Sensitivity (application), receiver BW = 470kHz	$V_{IN(MIN)}$	1·5 (−103)	1·12 (−106)	0·89 (−108)	µVrms (dBm)	2kb/s data rate, V_{CC} = 5V, f0 = 433·92MHz (Figure 19, Notes 3 and 11)
Sensitivity (application), receiver BW = 50kHz	$V_{IN(MIN)}$	0·79 (−109)	0·56 (−112)	0·45 (−114)	µVrms (dBm)	2kb/s data rate, V_{CC} = 5V, f0 = 433·92MHz (Figure 20, Notes 10 and 11)
Overload performance	$V_{IN(MAX)}$	0·5	2·23		Vrms	20kb/s data rate at 470MHz (Note 2)
PLL control line (pin 16) to achieve 90% of final value PD1 and PD2	t_{S2}	2·0	3·5	6·0	ms	All, local oscillator low side injection 423·33MHz, V_{CC} = 5V (Figures 7 and 18, Notes 5 and 11)
PLL control line (pin 16) to achieve 90% of final value PD1 and PD2	t_{S3}	0·20	0·35	1·5	ms	All, local oscillator low side injection 423·33MHz, V_{CC} = 5V (Figures 7 and 18, Notes 5 and 11)
Data output voltage high	V_{OH}	V_{CC}−0·7			V	I_{OH} = +20µA (Figure 20)
Data output voltage low	V_{OL}			0·7	V	I_{OL} = −20µA (Figure 20)
Conducted emissions	Antenna (LO)		5·6 (−92)		mVrms (dBm)	All, LO low side injection 423·33MHz, with SAW filter (Figure 26, Notes 6 and 11)
				100 (−60)	mVrms (dBm)	All, LO low side injection 423·33MHz, SAW filter removed (Figure 25, Notes 6 and 11)
Anti-jam rejection	Jam		+12	+20	dB	V_{CC} = 5V (Figure 8, Notes 7 and 11)

AC Electrical Characteristics (2)

These characteristics are typical values measured for a limited sample size. They are not guaranteed by production test. They are only given as a guide to assist in the design-in phase of KESRX05 (refer to Note 11)
All characteristics measured at T_{AMB} = 25°C and V_{CC} = 5V unless otherwise stated.

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Internal RF Amplifier						
Parallel input impedance	RF_{IN}		2·8//1·8		kΩ//pF	f_S = 434MHz
			1·78//1·7		kΩ//pF	f_S = 315MHz
Parallel output impedance	RF_{OUT}		10//1·1		kΩ//pF	f_S = 434MHz
			18//1·1		kΩ//pF	f_S = 315MHz
Noise figure	NF		4·5		dB	f_S = 434MHz, matched 50Ω environment input and output
Noise matching impedance	RF_{IN}		1·0//4·6		kΩ//nH	f_S = 434MHz
1dB compression point	RF_{IN}		−20		dBm	Input referred, f_S = 434MHz, matched 50Ω environment input and output
Amplifier gain	RF_{AMP}		13		dB	f_S = 434MHz, output matched to mixer input impedance
Mixer						
Parallel input impedance	MIXIP		1·6//1·8		kΩ//pF	f_S = 434MHz
			1·6//1·8		kΩ//pF	f_S = 315MHz
Output impedance	IF1		300		Ω	f_S = 10·7MHz
Noise figure (double sideband measurement	NF		10		dB	f_S = 434MHz, matched 50Ω environment input and output
Mixer conversion gain	A_{MIX}		9		dB	f_S = 434MHz,f_S = 434MHz, measured at input to ceramic filter. Include 6dB matching loss
IF Strip (RSSI)						
IF input impedance	IF_{IN}		3·1		kΩ	f_S = 10·7MHz
IF gain of log amp	A_{LOG}		80		dB	All (Figures 14 and 15)

NOTES

1. The Sensitivity of the test fixture is degraded by loading the input to RF amplifier with 50Ω, lack of image rejection and increasing the data filter bandwidth from 5 to 50kHz Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error ratio of 0·01 where the input signal is a return to zero pulse at 470MHz,with an average duty cycle of 50%, 20kb/s data rate with the receiver bandwidth set to 470kHz.
2. Peak RF input level, pin RFIN, to overload the demodulator with the AGC operating. Equivalent to +7dBm for 50Ω input impedance, Where the input signal is a return to zero pulse at 470MHz with an average duty cycle of 50% and 20kB/s data rate with the receiver bandwidth set to 470kHz.
3. Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error ratio of 0·01 where the input signal is a return to zero pulse with an average duty cycle of 50%, 2kb/s data rate. Equivalent to −103dBm for 50Ω input impedance. Does not include insertion loss of SAW filter at RF input but does include IF filter of 470kHz 3dB bandwidth and a data filter bandwidth of 5kHz. The results shown in Figure 20 and in the AC Electrical Characteristics (1) on page 7 are with the simple LC circuit L5//C7 tuned correctly to 10·7MHz.
4. The performance of the power down option PD1 to PD2 cannot be guaranteed below 3V for temperatures less than 0°C. However, the time to good data of PD0 to PD2 can be improved by connecting a 200kΩ in parallel wth C14 (see Table 1, pin 23).
5. Time taken for PLL lock voltage to achieve 90% transition point of the control signal and the VCO frequency to achieve within 470kHz of the final frequency. The time taken to acquire PLL acquisition is governed by the PLL loop filter (C12, C1 and R2) and the crystal oscillator components (XTAL1, C13 and C14). The dominant term for PLL aquistion is the start-up time of the crystal oscillator circuit, provided the PLL loop filter settling time is much less than the crystal oscillator start-up time. Figure 7 illustrates a suitable test setup for measuring the acquisition time of the PLL and the results are shown in Figure 18. The electrical characterisation parameters are based on the following sets of conditions:

Crystal oscillator circuit		PLL loop filter	
Ident	**Value**	**Ident**	**Value**
C13 = C14	15pF	C12	1·5nF
XTAL1	6·6128MHz	C1	180pF
ESR	15·3Ω	R1	10kΩ
L	85·36mH		
C0	1·83pF		
C1	6·8pF		

The performance of the crystal oscillator can be improve by increasing the value of ESR (100Ω max.) or bt maintaining the crystaloscillator in PD0 mode by connecting a 200kΩ resistor in parallel with C14 (see Table 1, pin 23). The typical time to valid data of the receiver at a data rate of 2kb/s is shown in Figure 17, which is accurate to ±250µs since the duration of the SPACE at 2kb/s = 250µs.

6. Local oscillator power fed back into 50Ω source at antenna input (RF input). Measured with RF input matching network shown in Figures 25 and 26.

NOTES (continued)

7. In-band interference rejection for an unmodulated interfering signal at 100kHz low side from the wanted modulated signal at 433.92MHz to achieve a Bit Error Rate = 0·01. Figure 6 illustrates a suitable test set-up for measuring the interference rejection and selectivity of the receiver. Wanted signal = −90dBm at 433·92MHz (2kb/. 50% duty cycle), interfering signal = −78dBm at 433·82MHz. (unmodulated). Interference rejection typically equals +12dBm i.e. in-band interfering signal is 12dBm above the wanted signal level at -90dBm.
8. Actual intermediate frequency determined by choice of crystal and external ceramic filter.
9. For temperatures between 85°C and 105°C the maximum frequency of operation of the VCO local oscillator must be limited to 470MHz. The recommended components to limit the maximum free running frequency of the VCO to less than 470MHz, for an operating supply range of 5V±5%, are:

Ident	Value	Tolerance
D1	BB833	±9%
C11	6·8pF	±0·1pF
C18	10pF	±0·1pF
L2	39nH	±2%

The component values recommended in Tables 5 and 6 are to allow the KESRX05 to operate below V_{CC} = 3V by maintaining the PLL lock voltage at approximately 1·5V (V_{CC}/2) so that the VCO maximum free running frequency can exceed 470MHz. Thus, the recommended VCO component values for D!, C11, C18 and L2 given in Tables 5 and 6 cannot be used at temperatures above 85°C.

10. Sensitivity is defined as the average signal level measured at the input necessary to achieve a bit error rate of 0·01 where the input signal is a return to zero pulse with an average duty cycle of 50%, 2kb/s data rate. Equivalent to −109dBm for a 50Ω input impedance. Does not include the insertion loss of a front end SAW filter at the R F input but does include the IF filter of 50kHz 3dB bandwidth and a data filter bandwidth of 5kHz. The results shown in Figure 20 and in the AC Electrical Characteristics (1) on page 7 are with the simple LC circuit L5//C7 tuned correctly to 10·7MHz.
11. This parameter is not 100% tested by production.

FUNCTIONAL DESCRIPTION

Power Down

The PD pin, a tristate input, provides a 2-stage power down for the receiver. The receiver is fully operational when the pin is held high and is fully powered down when the pin is taken to ground as shown in Table 2.

Pin 25		Status
PD0	Low (0V)	Receiver powered down
PD1	V_{CC}/2	Crystal oscillator running
PD2	High (V_{CC})	Receive mode

Table 2

PD0 = Low

None of the receiver circuits are functional. Current $I_{CC}2$, is reduced to its lowest level of <50µA (V_{CC} applied). A longer settling time (t_{S2}) is required to restore full performance after switching to receive mode PD0 to PD2 (Figures 7, 17 and 18). The settling time (time to valid data) of the receiver can be improved by maintaining the oscillation of the crystal in PD0 mode by placing a 200KΩ resistor in parallel with C14. The addition of this resistor will increase the current consumption of the receiver by approximately 20µA (see Table 1, pin 23).

PD1 = V_{CC}/2 or High-Z source (CMOS tristate)

A non-receiving state with some critical circuits running including the crystal oscillator. Current consumption $I_{CC}1$, is reduced to about 330µA. When switching to the receive state, PD1 to PD2 (Figures 7, 17 and 18), data can start to be recovered within 1ms (t_{S2}) for signals close to maximum sensitivity.

PD2 = High

The receiver is fully functional and ready to receive data.

RF Down-Converter

An internal RF amplifier is designed to interface directly to an antenna or to an input SAW filter with a maximum insertion loss of 3dB. The RF amplifier gain is about 1 3dB at 460MHz when matched into the mixer, while the RF amplifer noise figure is about 4·5dB when fed from a 50Ω source. The internal RF amplifier feeds a double balanced mixer through an external impedance matching circuit, RFOP to MIXIP.

The AGC circuit monitors the mixer signal output level. Control is fed back, applying AGC to the RF amplifier to prevent overloading in the mixer and the generation of unwanted distortion products. This also has the effect of reducing the RSSI characteristic slope and extending its range of operation by more than 20dB at high signal levels (Figure 13).

The AGC circuit also applies mixer booster current to improve the linearity of the mixer at high signal levels. This can be confirmed by monitoring the current consumption of the receiver with applied RF signal level (Figure 16).

The AGC circuit comes into operation at mixer output signals greater than approximately −25dBm and reduces the RF amplifer gain by 6dB at an input signal level of approximaely −30dBm. Since the AGC operates on the mixer output signal level then the exact point where the AGC comes into opera tion depends on the RF amplifer to mixer matching circuits and RF amplifer gain.

IF Interface

Unlike KESRX01 there is no internal integrated IF filter. This is to provide a more flexible design and allows the system designer to use a low IF or high IF up to 15MHz. Typically, a 10·7MHz ceramic IF filter connected between IFOUT and IFIN would be used together with an input RF SAW filter to give very good image channel rejection. The

choice of bandwidth for the 10·7MHz ceramic filter depends on frequency tolerancing of the transmitter, receiver, data rate and component cost.

The IF filter drive, IFOUT, is a voltage drive with a 300Ω series resistance (see Table 1, pin 6). This allows impedance matching to the ceramic IF filter to be set by an external series resistor. A 10·7MHz ceramic filter with, typically, a 300Ω input impedance does not require an external matching resistor at IFOUT.

The input to the log amp, IFIN, is high impedance with an internal 3kΩ shunt resistor. Impedance matching to the output of the ceramic filter is achieved by an external shunt resistor R9 between IFIN and IFDC1 (see Table 1, pin 3).

Phase Lock Loop VCO

The local oscillator (LO) is a VCO locked to a crystal reference by a phase lock loop (PLL). The VCO gain is nominally 26MHz/V depending on the external varactor used. The LO frequency is divided by 64 and fed into the phase-frequency detector, where the reference frequency is provided from the crystal oscillator. The AC phase detector output current into the PLL loop filter is nominally ±15µA. The maximum loop filter bandwidth is 50kHz.

VCO Circuit Design and Layout

The Local Oscillator (LO) frequency is controlled by a parallel resonant tuned circuit. The frequency of the local oscillator is controlled by a Phase Locked Loop (PLL), referenced to the crystal frequency.

Designing for VCO Track Parasitics

To remove the effect of track parasitics the following procedure should be adopted.

1. Open circuit the control feed back from the PLL control loop by removing R1.

2. Connect an external Power Supply Unit (PSU = V_{CC}/ 2) in place of R1, LF output (Figure 3).

3. Using a spectrum analyser, monitor the LO level at the RFIN port. Alternatively use a small pick-up coil to loosely couple to the signal generated across L2.

4. Note that the LO level is <<−65 dBm, range = 300 to 500MHz.

5. Vary the value of the PSU input to confirm that there is a corresponding change in LO frequency. Set the PSU at V_{CC}/2. If the VCO does not oscillate at V_{CC}/2, characterise the LO at an alternative voltage.

6. Using a plot of the varactor characteristic determine the varactor capacitance at V_{CC}/2. e.g. for a 2V V_{CC} design the Siemens BB833 capacitance at 1V = 10pF (approx.).

7. Using the following equation deduce the value of the total stray parasitic capacitance C_P.

$$C_P = \left[\frac{1}{(2\pi \times f_{LO}{}^2 \times L2)^{-C_V}}\right]$$

where C_V = varactor capacitance at V_{CC}/2

8. Using the following equation select the nearest value for $L2$ to centre the VCO at V_{CC}/2.

$$L2 = \frac{1}{(2\pi \times f_{LO}{}^2) \times (C_P + C_V)}$$

9. By varying the PSU voltage confirm that the LO is centred correctly at V_{CC}/2, and that the oscillator operates over the range 0V to V_{CC}.
10. Disconnect the PSU and reconnect R1. Measure the value at LF output using a ×10 probe and an oscilloscope. This should be a direct voltage with no ripple at V_{CC}/2 (±0.3V). If not repeat steps 1 to 8. To compensate for non standard inductor values vary the value of C18 and C11 to vary the capacitance of the varactor to centre the V_{CC} at V_{CC}/2.

NOTE: It is important to minimise stray capacitance in the VCO circuit to ensure that the VCO starts oscillating. The use of a varactor with a low capacitance at zero bias is advisable. Similarly, reducing the values of C11 and C18 whilst increasing L2 will help to reduce the capacitance of the varactor at 0V, improving the reliability of the oscillator. A compact design methodology is recommended for the VCO circuit components L2, C11, C18 and D1.

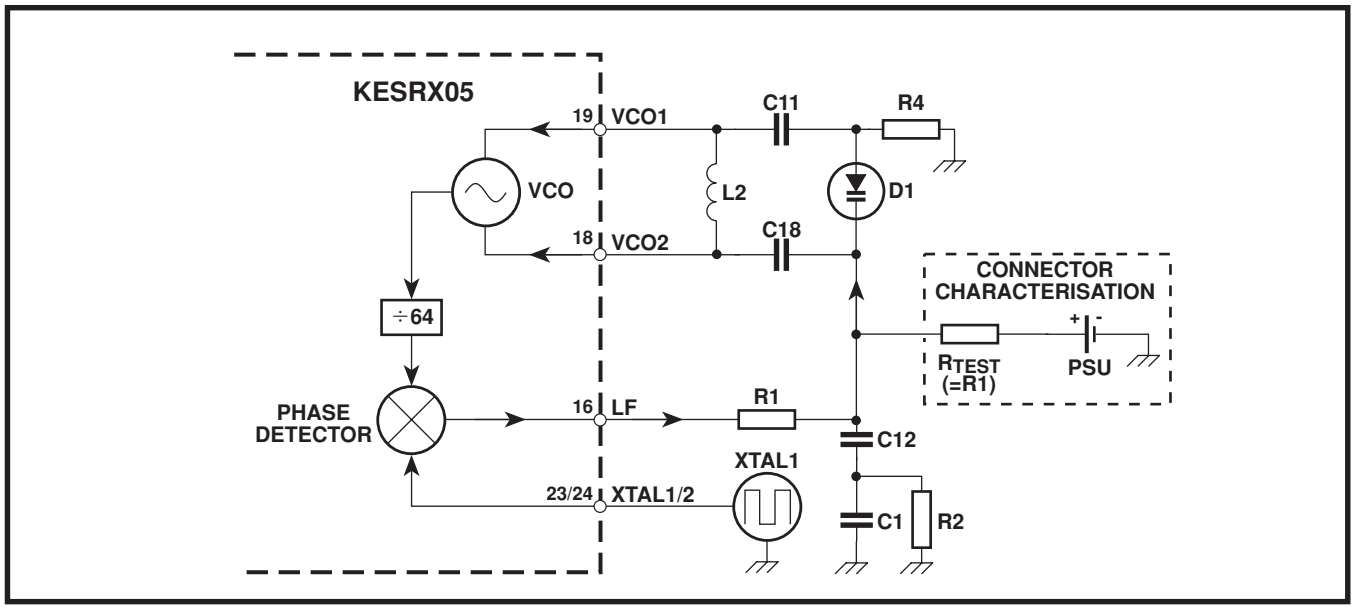


Figure 3 Characterising the VCO/PLL operation

IF Amp/RSSI Detector

This is a log amplifierwith a small signal gain >80dB and an RSSI output used as the detector. The 3dB bandwidth of the IF log amplifier is typically 45MHz to allow for high IFs to be used. However, normally, this wide IF bandwidth would limit the overall sensitivity of the receiver due to the amplified wideband noise generated in the first IF stage. Since the RSSI detector is not frequency selective, any wide band noise introduced after the intermediate filter CF1 will be detected as signal. A simple LC noise reduction filter is therefore positioned part way down the log amplifier to reduce the noise power from the earlier stages. Typically this filter only needs to be a fixed component parallel LC filter (L5 and C7) between pins IFFLT1 and IFFLT2 with a 1 MHz bandwidth (i.e. Q ~10). There are two internal 20kΩ damping resistors across these pins which will determine the Q and the choice of L and C values (AC equivalent circuit = 20kΩ), i.e:

$$L = \frac{2\times10^4}{2\pi f_{IF} Q} \qquad C = \frac{1}{(2\pi f_{IF})^2 L}$$

An external damping resistor can be used to lower the Q of the tuned LC circuit. This will alter the gain of the log amplifier, i.e., slope and gradient of Figure 15. The objective of the damping resistor is to prevent mis-tuning of the LC circuit due to component tolerancing and thus degrading the sensitivity of the receiver. The sensitivity results shown in Figures 19 and 20 and in the AC Electrical Characterisics (1) apply with no external damping resistor and the LC circuit correctly tuned to 10·7MHz. The preferred alternative to a damping resistor is to lower the Q of the the inductor L5 or to increase the tolerance of C6.

A ceramic resonator or filter is not a recommended here as the external LC filter provides a low impedance DC path to remove any DC voltage offsets at the output of the high gain log amplifier, RSSI pin 27. Further improvement in sensitivity can be gained by increasing the Q of the parallel LCfilter, provided that tolerancing of the LC filter is taken into account.

For a low IF receiver, <1 MHz, a low pass filter can be used for both the IF and noise reduction filter. Such a receiver, however, will have virtually no image rejection capability, and will thus have a 3dB penality in noise factor, impairing the ultimate sensitivity of the receiver by a minimum of 3dB.

The RSSI output transfer characteristic, at the RSSI pin, has a slope of about 16mV/d B. A typical transfer characteristic from RFIN input to RSSI output is plotted in Figures 14 and 15, measured with a constant wave (n0 modulation RF input signal. This shows the effect of the AGC in extending the range of the detector to >+10dBm RF input signal and includes the effect of the AGC circuit adapting to this signal level.

Because the RF amplifier AGC has a fast attack time and slow decay time characteristic, the gain of the stage remains constant during the data burst. This means that the change in output for a given extinction ratio also remains constant at approximately 16mV/dB up to peak input signal levels >+10dBm. This requires the decay time constant to exceed the transmitted bit period and no long period of zero signal power has been transmitted.

Increasing the decay time constant of the AGC circuit by increasing the value of C8 will impair the settling time (time to good data) of the receiver. When duty cycling the

operation to the receiver between PDO and PD2 to lower power consumption of the receiver. When Duty cycling the receiver between PD1 and PD2 the settling time of the receiver is independent of C8. In the application circuit Figures 25 and 26 the value of C8 is configured for minimum settling time. The times to valid data with C8 = 10nF are shown in Figure 18 for PD0 to PD2 and PD1 to PD2.

Anti-jamming Circuit

The output of the RSSI is AC coupled by C10 into the Anti-jamming circuit where the signal is DC restored on the peak signal level (Figure 10). The coupling capacitor charges to the appropriate DC level, which is related to the final slice level for the data comparator. The anti-jamming circuit amplifies the peak of the signal to recover the data signal component even in the presence of jamming signals. The interferer causes modulation of the wanted signal at the beat frequency of the two signals and reduces the amplitude of the wanted data component making it more difficult to recover. The action of the anti-jamming circuit centres the bandwidth of the receiver around the wanted signal proportional to the data filter bandwidth to suppress the interfering beat frequency recovering the wanted signal. Bypassing the anti-jamming circuit (Figure 11) will result in data corruption for interfering RF signal levels 6dB below the wanted signal (Figures 8 and 9).

The DC restoration circuit has a fast attack time and slow decay time, both controlled by the value of coupling capacitor chosen between RSSI and DETB pins. Reducing the data rate or increasing the mark/space ratio will require a corresponding increrase in the value of C10.

Figure 6 illustrates a suitable test setupforcharacterising the interference rejection and selectivity of the receiver.

Figure 8 illustrates the in-band interference rejection with the anti-jam circuit connected as shown in Figure 10 and bypassed (Figure 11) at V_{CC} = 3V and T_{AMB} = 25°C. Note the improvement in interference rejection between the two modes of operation over the wanted signal range of −94 to 0dBm. Note also the 40dB improvement in signal handling capability with the anti- jam circuit connected and the 20dB improvement with the SAW filter removed

Figure 9 illustrates the difference in receiver selectivity with the ant-jam circuit connected and bypassed. Note the improvement in receiver selectivity between the two modes of operation over the frequency range 433·92MHz ±5kHz and the ability of the anti-jam circuit to improce the selectivity of the SAW filter over the frequency range 433MHz to 434·5MHz. Also note the 20dB improvement in the in-band signal handling capability demonstrated in Figure 8 with the SAW filter not used. This can be used to improve the out-of-band blocking capability of the application without SAW filter (Figure 25); this design option can reduce the overall cost of the receiver by, typically, 1 to 2 US Dollars.The selectivity curve with the anti-jam circuit by-passed is governed by the response of the front end IF ceramic filter, secondary IF filter and data filter.

Figures 8 and 8 were recorded with the component specifications given in Table 3.

Component specification (Figure 10)		Component specification (Figure 11)	
R6	130kΩ	R6	12kΩ
C2	270pF	C2	N/A
L5//C7	1MHz at 10·7MHz	L5//C7	1MHz at 10·7MHz
Data filter BW	5kHz	Data filter BW	5kHz
IF BW	470kHz	IF BW	470kHz
SAW BW/No SAW BW	750kHz/1MHz	SAW BW/No SAW BW	750kHz/1MHz
OOK modulation	2kb/s (50% duty cycle)	OOK modulation	2kb/s (50% duty cycle)

Table 3 Component specification for Figures 10 and 11. The values given are changes from those given in Table 5 necessary to obtain the results shown in Figures 8 and 9.

Improving Anti-Jamming Performance

- Interference rejection (dB) = Interferer (dBm) − Wanted (dBm). The interference rejection of the receiver for different modulation schemes can be improved by:
- Changing the value of C2. Increasing the value of C2 may result in pulse stretching of the recovered signal.
- Adjusting the comparator reference level (DSN) by offsetting the internal reference (Figure 6) by a high value resistor from the DSN pin to V_{EE} and or the peak detector output. (Figures 25 and 26).
- Reducing the bandwidth of the data fillter, intermediate frequency filter CF1 and/or the noise reduction filter (L5 C7). Thebandwidth of the receiver must accommodate tolerancing of the data, transmitter and receiver.
- Increasing the value of AGC capacitor C8 to maintain the level of the AGC controi during the off period of the wanted modulation signal. This will improve the interference rejection of the receiver but increase the time to good data from power-up PD0 to PD2. The application circuit Figure 26 has been optimised for time to good data.
- Changing the value of C10 to allow the anti-jam circuit to detect/recover alternative data modulation schemes such as PWM.

Baseband

The RSSI output will contain wide band demodulated noise and signals which are within the RF and IF filter pass bands. An additional low pass data filter is therefore used to improve overall sensitivity.

KESRX05 has an integrated second-order Sallen and Key data filter whose characteristic is set by R10, R11, C5 and C6. Figure 10 showsthe connections and calculation for the −3dB cut-off frequency and filter type. The cut-off frequency is determined from the data rate and the level of pulse distortion which can be tolerated. The data filter cut off frequency is usually set at 3 to 5 times the minimum pulse width period, i.e:

$$f_C = 5 \times \frac{1}{\text{Data pulse width}}$$

The output from this filter, DF2, is directly coupled into the inverting input of the data comparator with a fixed slice level applied to the non-inverting input, DSN. A peak detector recovers the signal amplitude on the capacitor.

Normally, the comparator reference level used is the internal reference, a capacitor at Pin DSN serving to remove noise pick-up. In order to fine tune the slice level for sensitivity, squelch and optimum interference rejection the slice level can be offset from the internal reference by a high value resistor from the DSN pin to Vee and/or the peak detector output (Figures 25 and 26).

The data comparator (slicer) output, DATAOP, is CMOS compatible but is only capable of driving small capacitive loads, <20pF, depending on data rate. With the anti-jam circuit connected, data output has the inverted sense of the input signal at DF2.

To invert the sense of the data output with the anti-jam circuit connected, the buffer transistor circuit shown in Figure 4 can be used.

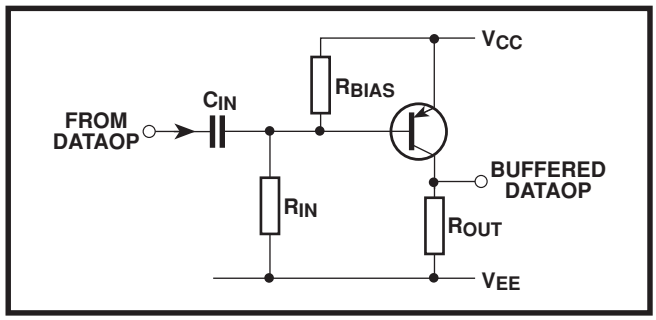


Figure 4

Data state		Buffered state	
High	Data	Low	V_{EE}
Low	Data	High	V_{CC}

Table 4

NOTE

Buffered DATAOP will squelch low if the input data signal remains continuously in a high or low state. The time taken for the buffered data output to squelch low is governed by the time constant $C_{IN}R_{IN}$.

The output drive current is nominally ±50µA so that a system using high data rates or higher capacitive loads, e.g. long track lengths, may need to incorporate a buffer transistor to provide the necessary edge speeds to the following logic circuits.The comparator has 20mV hysteresis built-in to reduce edge chatter.

The sense of the squelch on the data output is low when no signal is present. This may be confusing, as a low output during the data burst also corresponds to the on period, i.e. the MARK, of the RF OOK signal. However, it is the very first pulse of the data signal which causes the DC restoration capacitor of the anti-jamming circuit to charge to the correct level appropriate to the final slice level. As a consequence of this the very first pulse of the data transmission may be lost as the receiver adapts to the incoming signal level.

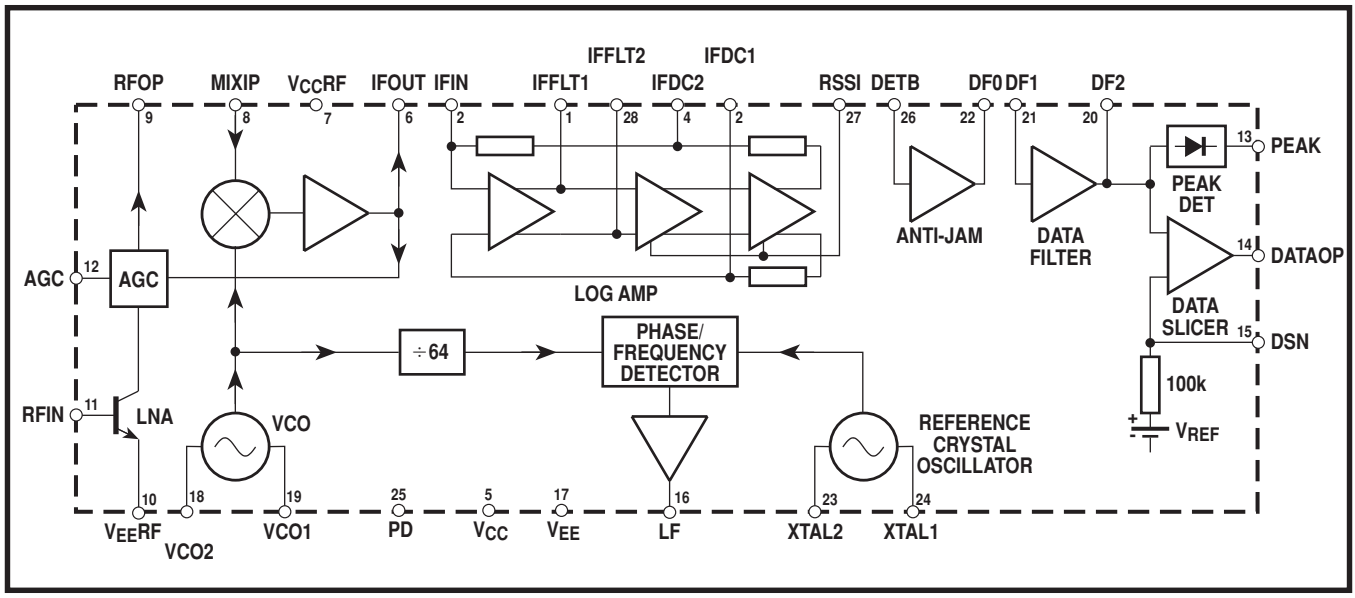
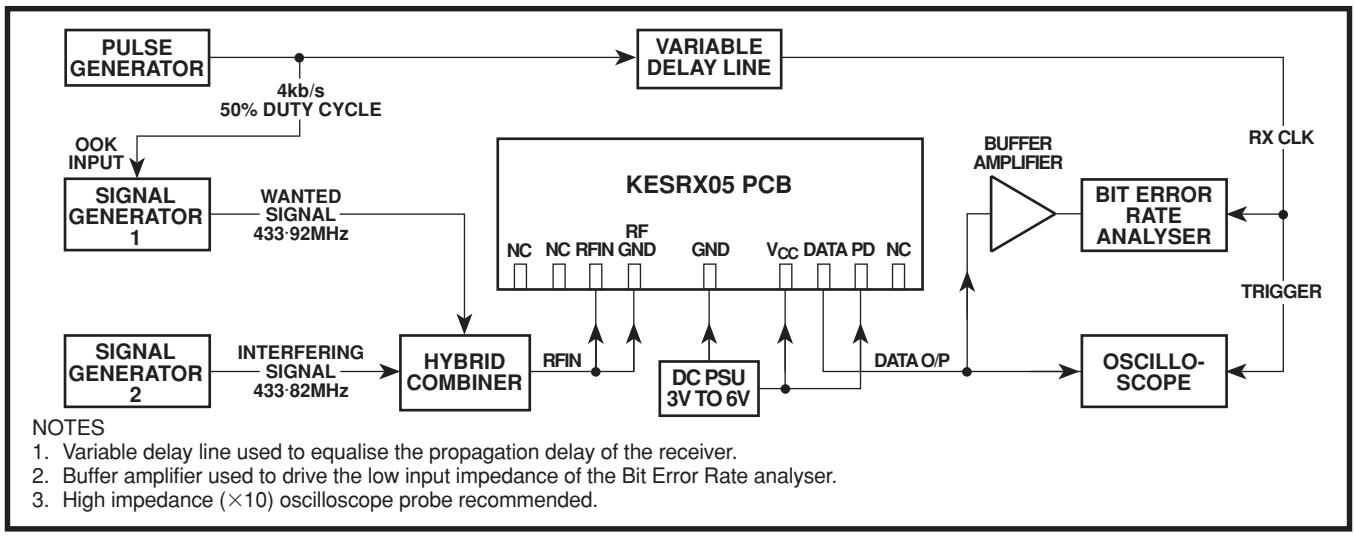
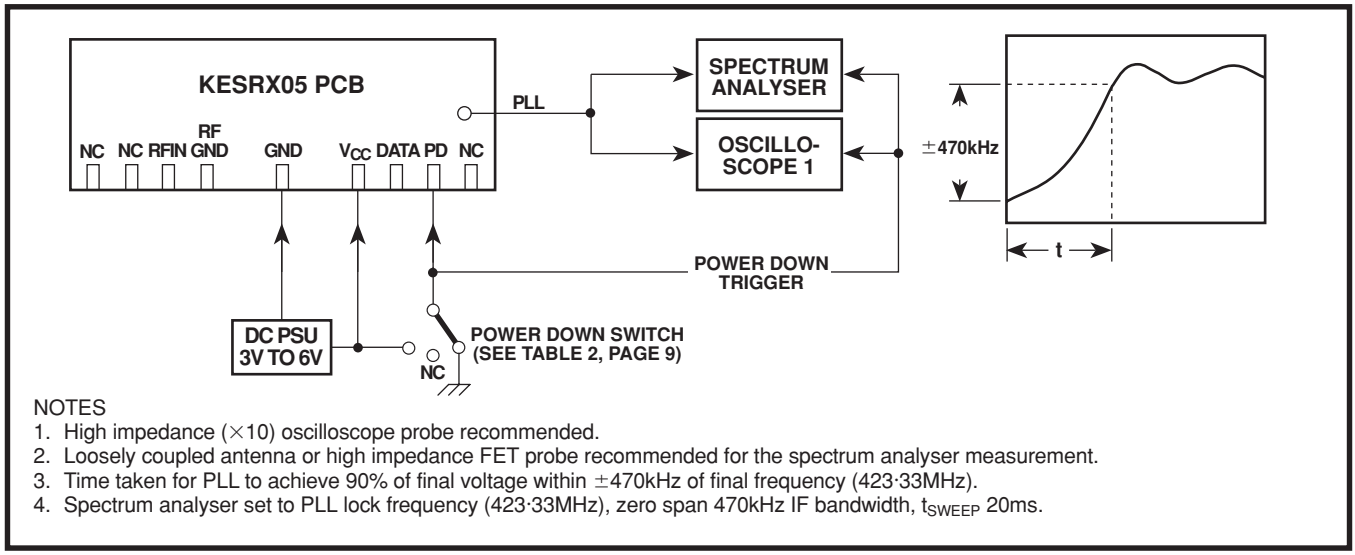


Figure 5 Block schematic of KESRX05



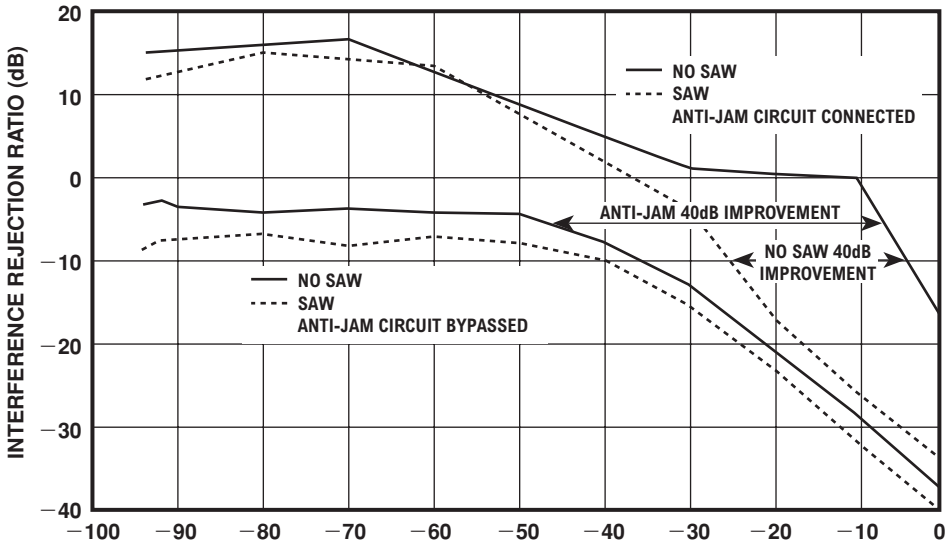
NOTES
1. Variable delay line used to equalise the propagation delay of the receiver.
2. Buffer amplifier used to drive the low input impedance of the Bit Error Rate analyser.
3. High impedance (×10) oscilloscope probe recommended.

Figure 6 Characterising selectivity and interference rejection



NOTES
1. High impedance (×10) oscilloscope probe recommended.
2. Loosely coupled antenna or high impedance FET probe recommended for the spectrum analyser measurement.
3. Time taken for PLL to achieve 90% of final voltage within ±470kHz of final frequency (423·33MHz).
4. Spectrum analyser set to PLL lock frequency (423·33MHz), zero span 470kHz IF bandwidth, t_{SWEEP} 20ms.

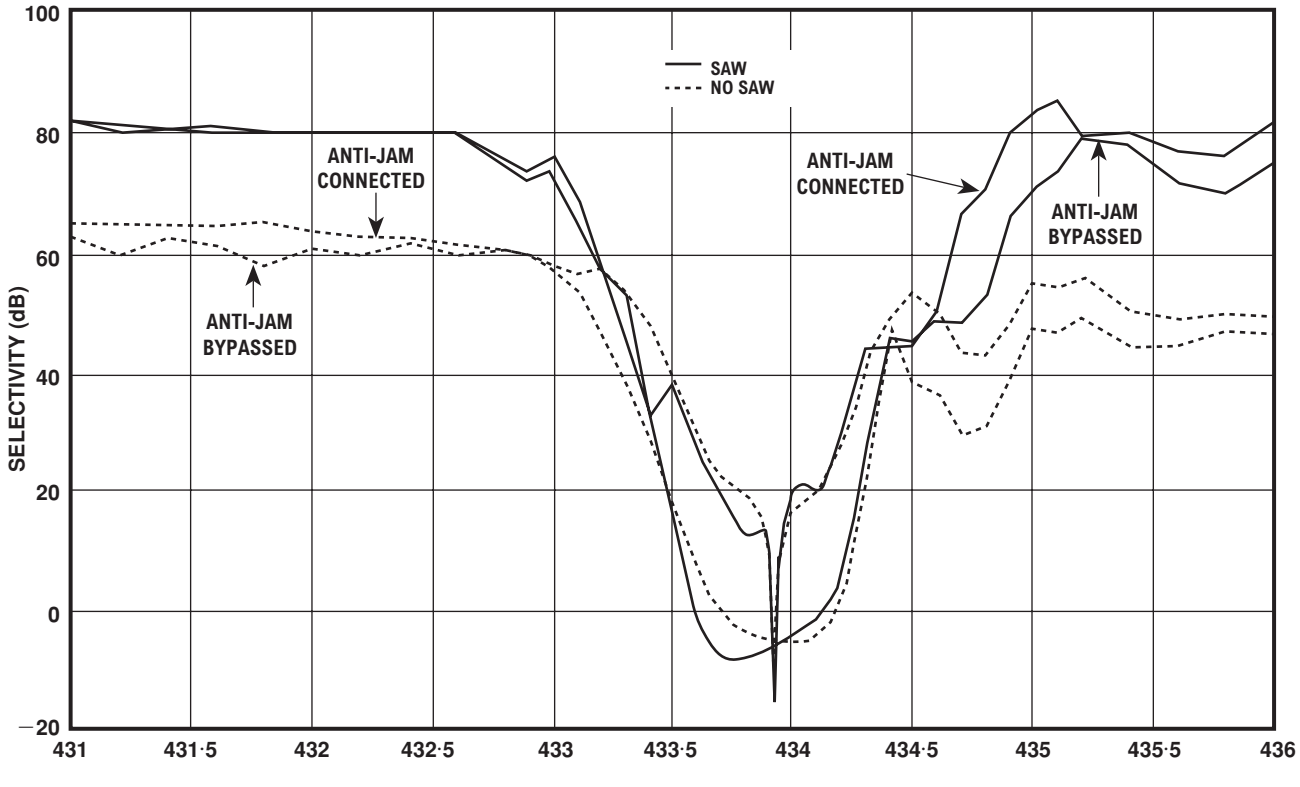
Figure 7 Characterising the PLL acquisition time from power-up



NOTE
Unmodulated interfering signal is 100kHz low side from wanted signal. Both signals are within the passband of the receiver (ceramic filter)

i.e. Wanted signal = 433·92 MHz at 2kb/s, −90 to 0dBm (50% duty cycle)
Interfering signal = 433·82MHz continuous carrier, −90 to 0dBm

Figure 8 In-band interference rejection of the receiver



NOTE
The action of the anti-jam circuit to centre the bandwidth of the receiver around the wanted modulated signal at 433·92 MHz, 20kb/s, 50% duty cycle, −90dBm Also notice the ability of the receiver to achieve the same selectivity performance over the frequency range 433 to 434.5 MHz with and wthout a SAW filter.

Figure 9 KESRX05 selectivity response

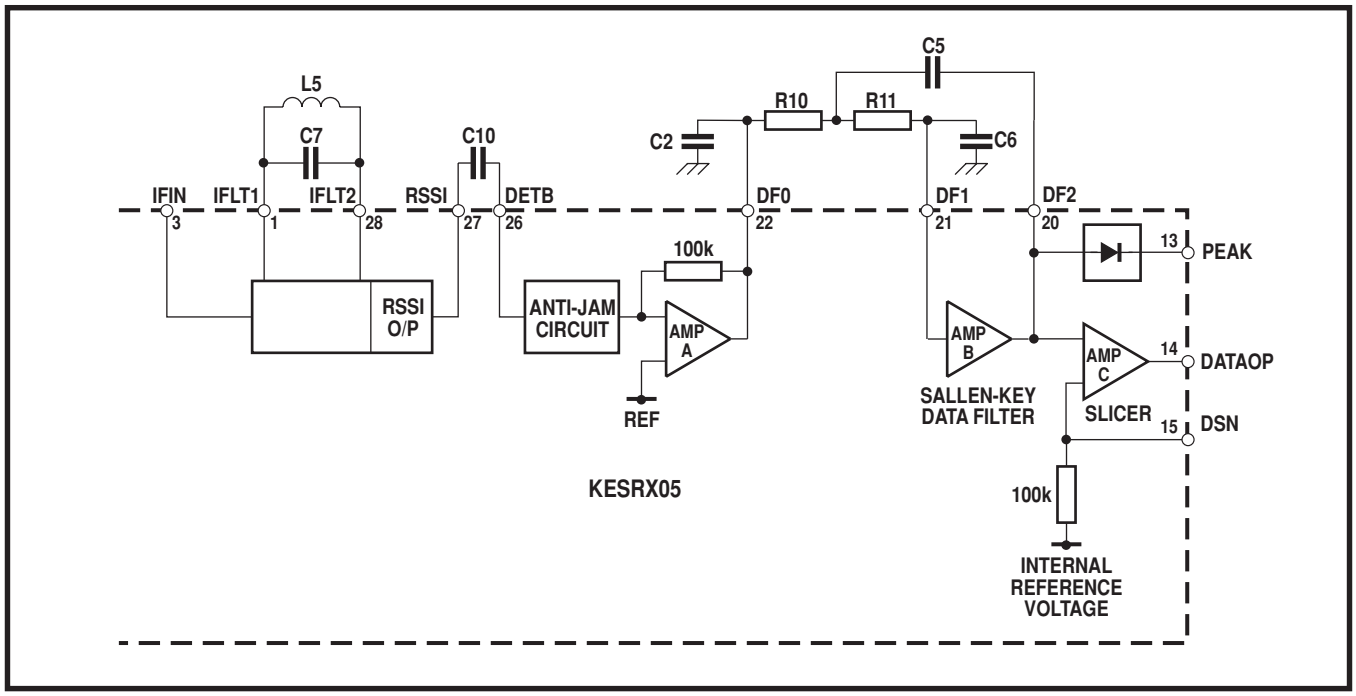


Figure 10 Anti-jam circuit and data filter. Component idents refer to Figure 25, Figure 26 and Table 5.

Sallen and Key Filter Components

Cut-off frequency = f_C, therefore $\omega_C = 2\pi f_C Y$

$$C5 = \frac{2Q}{R\omega_C} \qquad C6 = \frac{1}{2QR\omega_C}$$

where, for a Bessel response, Q = 0·557 and Y = 1·732 and, for a Butterworth response, Q = 0·71 and Y = 1·0.

Example

To implement a filter response with a 10kHz 3dB cut-off frequency and with R10 = R11 = 100kΩ,

Bessel filter: C5 = 106pF, C6 = 80pF
Butterworth filter: C5 = 150pF, C6 = 150pF

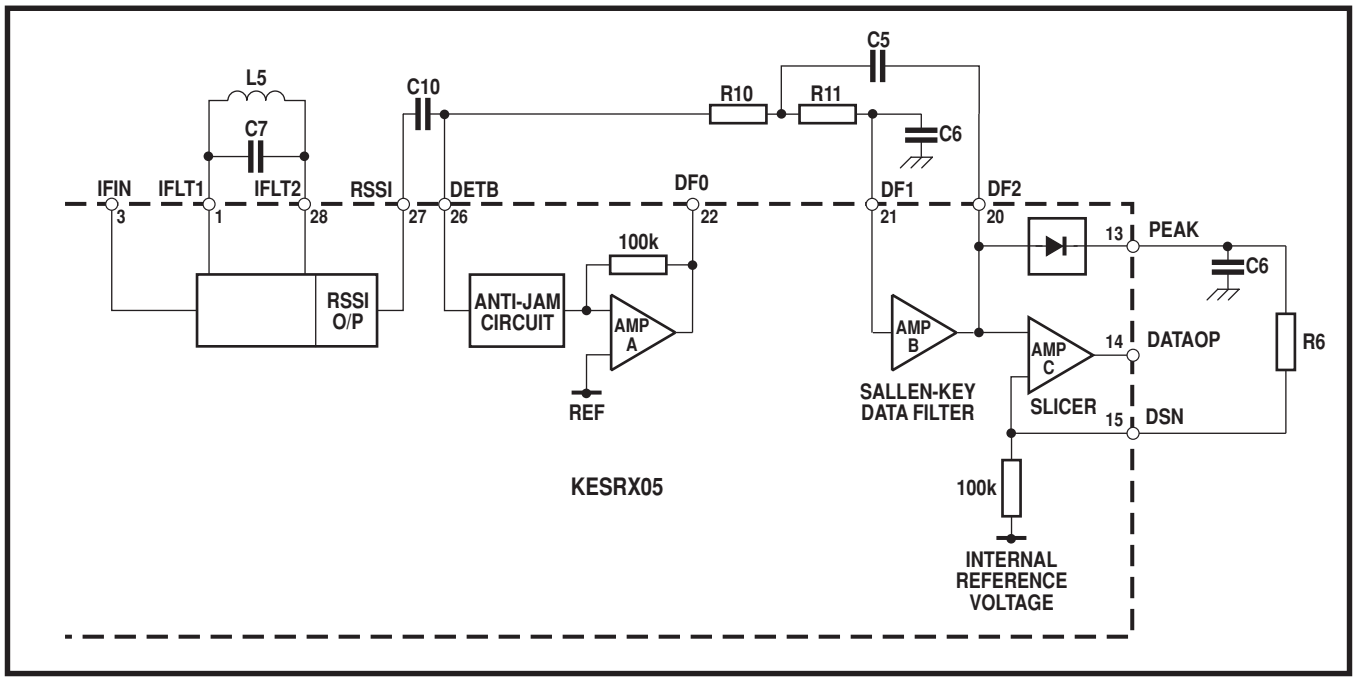
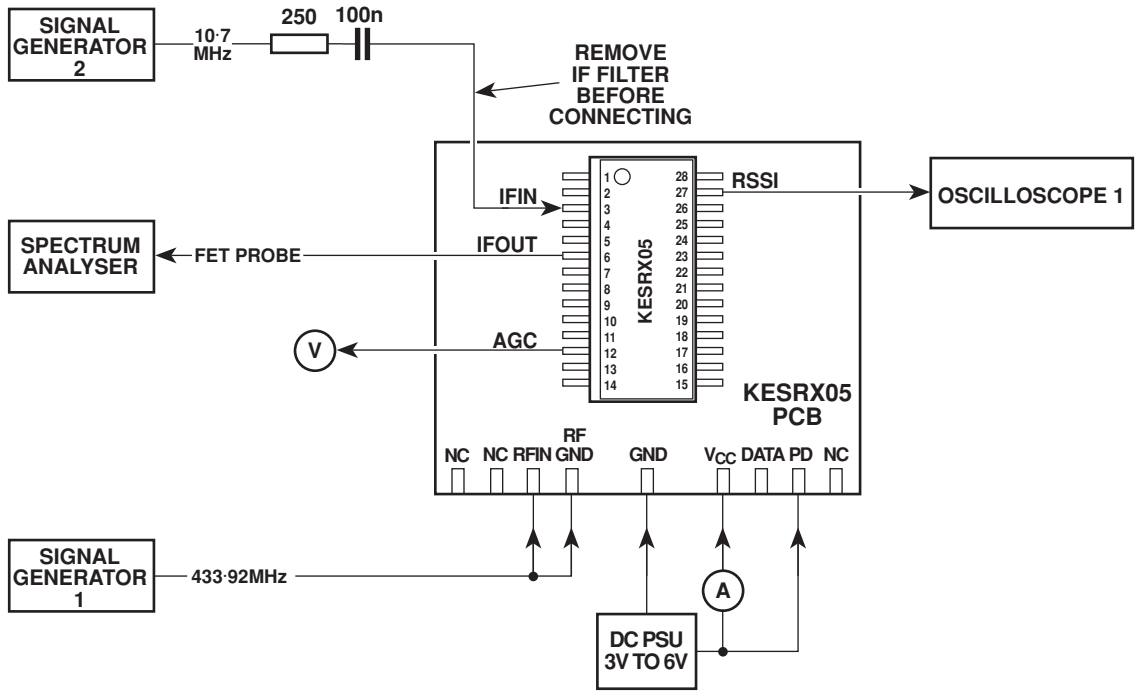


Figure 11 Bypassing the anti-jam circuit (use component revisions recommended in Table 3)



NOTES
1. The 250Ω resistor added to the output of signal generator 2 modifies its characteristic impedance to mimic the output of the ceramic filter.
2. The 100nF capacitor brevents de-biasing of IFIN/

Figure 12 Characterising the receiver performance (Figures 13 to 16)

The characteristics shown in Figures 13 to 24 are typical results measured from a a limited sample of production devices (see notes on page 19)

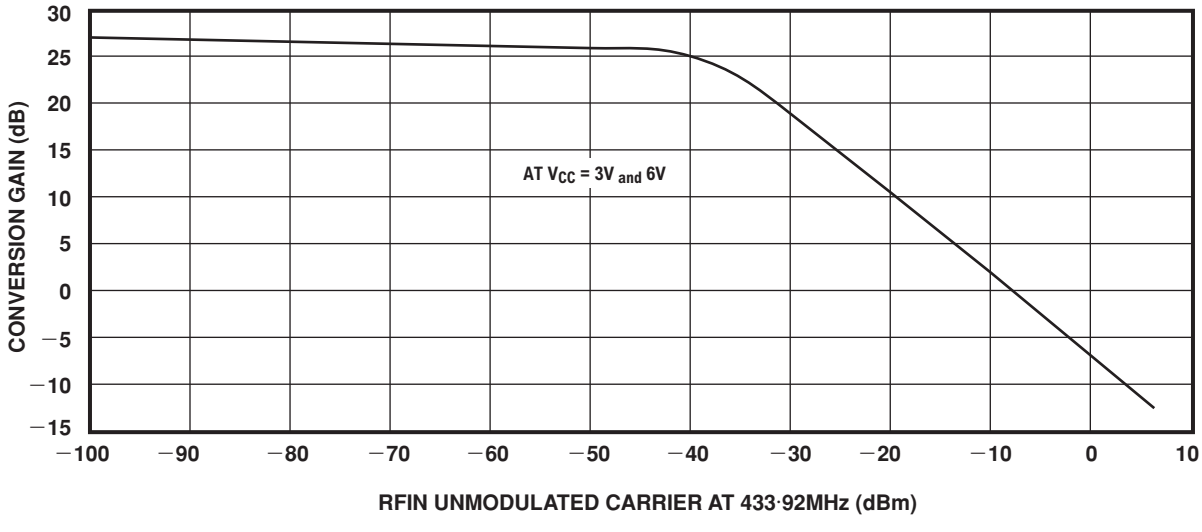


Figure 13 RFIN to IFOUT conversion gain (see RF Down-Converter, page 9)

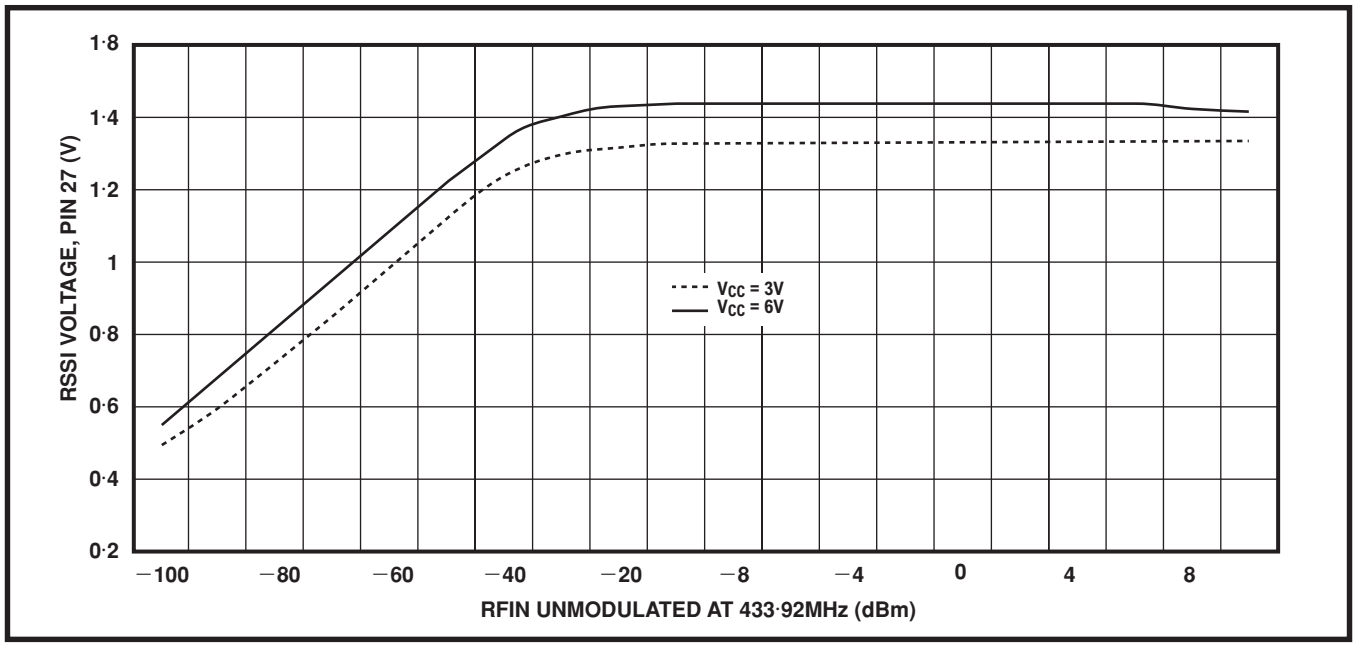


Figure 14 RFIN to RSSI output transfer characteristic (see IF Amp/RSSI Detector, page 11)

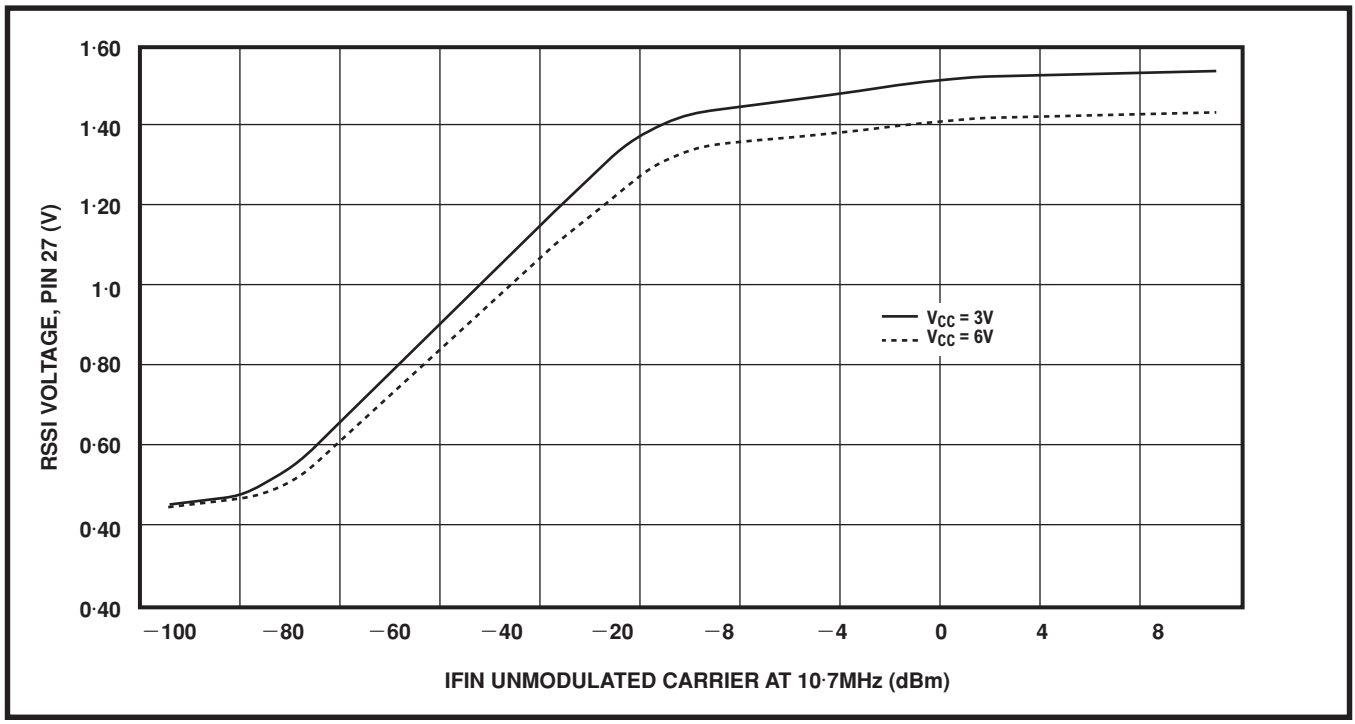


Figure 15 IFIN to RSSI output transfer characteristic (see IF Amp/RSSI Detector, page 11)

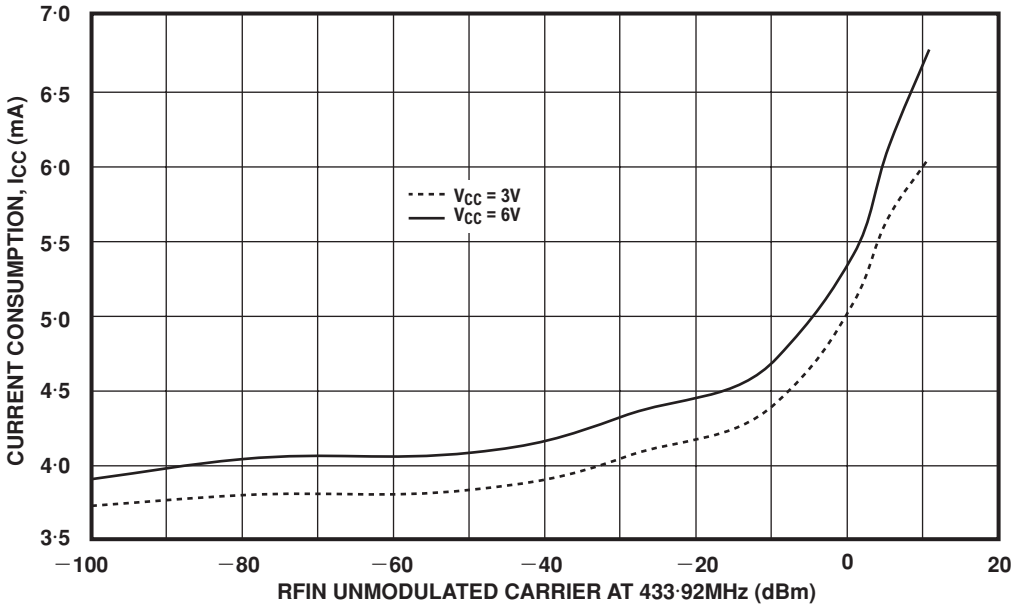
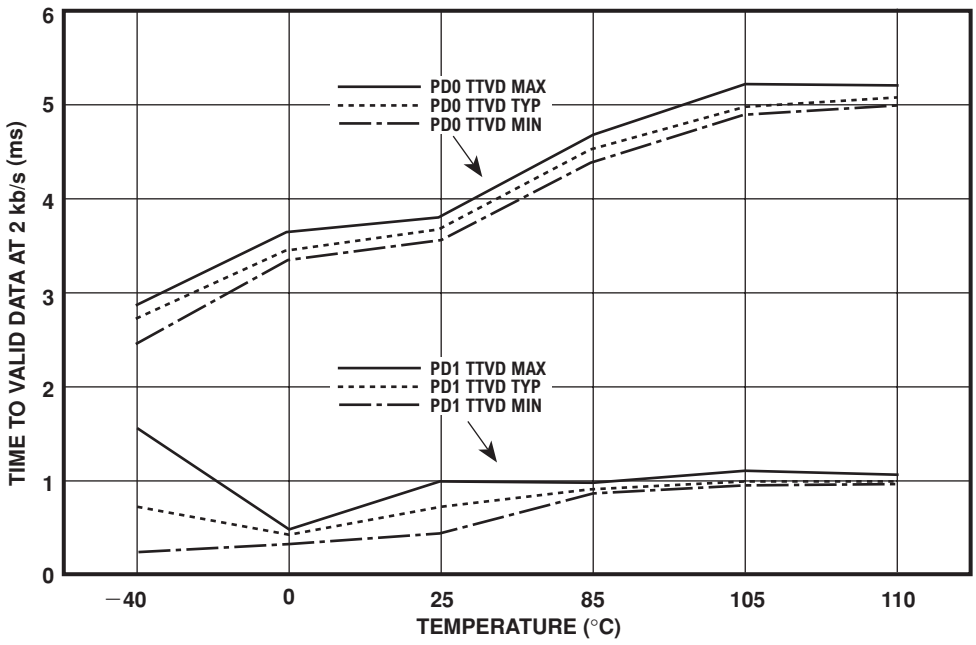


Figure 16 Receiver current consumption v. received signal strength RFIN (see RF Down-converter, page 9)

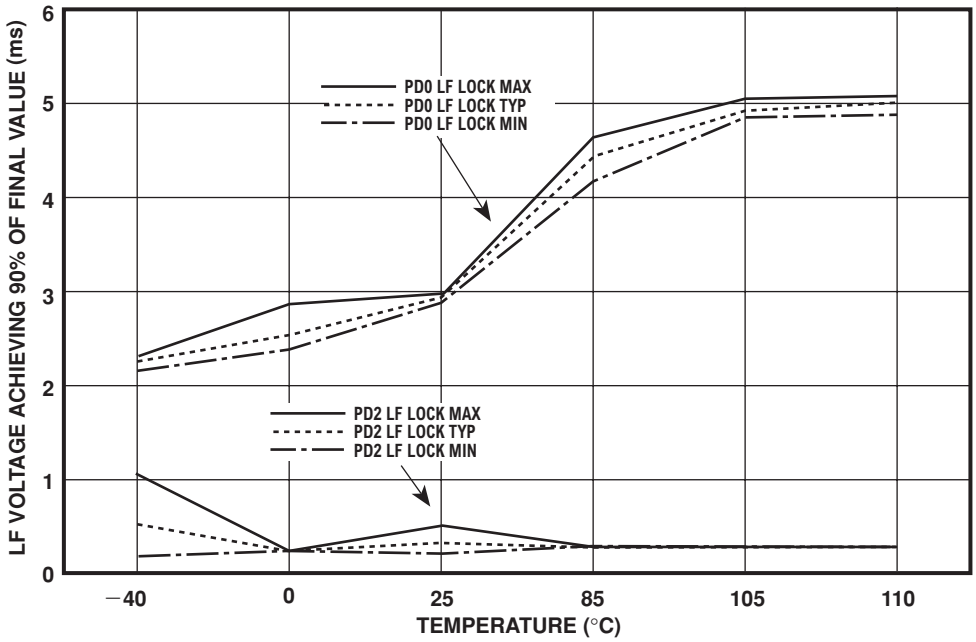
NOTES

1. Conversion gain of the receiver is limited by the insertion loss of the front end SAW filter.
2. Dynamic range of the RSSI output transfer characteristic (Figure 14) is governed by the noise figure of the receiver, which is limited by the insertion loss of the front end SAW filter and the bandwidth of the 10·7MHz ceramic filter.
3. Reduction in conversion gain and increase in receiver current consumption coincides with lift-off of the AGC control line (pin 12). Action of the AGC applies additional mixer booster current to improve the linearity of the mixer at high signal levels.



NOTE
Time to valid data of PD0 to PD2 can be improved by maintaining the crystal oscillator in PD0 mode (see Power Down, page 9 and Table 1, pin 23.)

Figure 17 PD0 to PD2 and PD1 to PD2 time to valid data (see Power Down, page 9)



NOTE
Time to PLL acquisition of PD0 to PD2 can be improved by maintaining the crystal oscillator in PD0 mode (see Power Down, page 9 and Table 1, pin 23).

Figure 18 PD0 to PD2 and PD1 to PD2 time to PLL acquisition (tS1 and tS2, AC Electrical Characteristics (1), page 7)

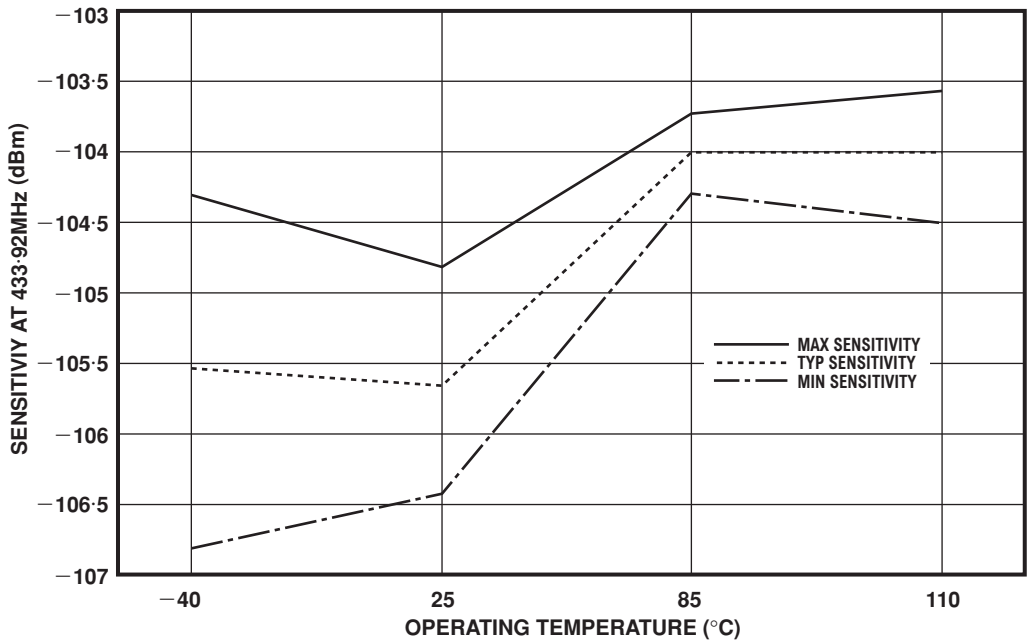


Figure 19 Receiver sensitivity v. temperature at V_{CC} = 5V (V_{IN}, AC Electrical Characteristics (1), page 7)

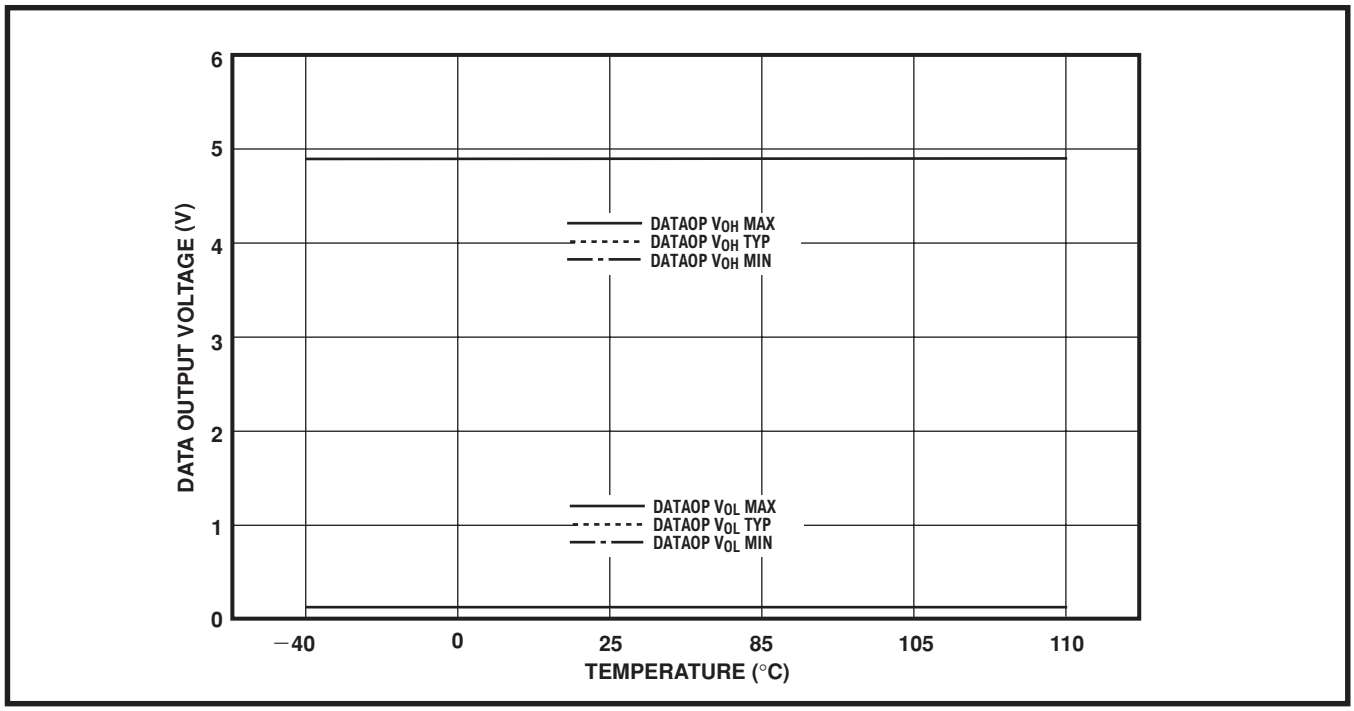


Figure 20 DATAOP I/O voltage drive at ±20μA (V_{OH}/V_{OH}, AC Electrical Characteristics (1), page 7)

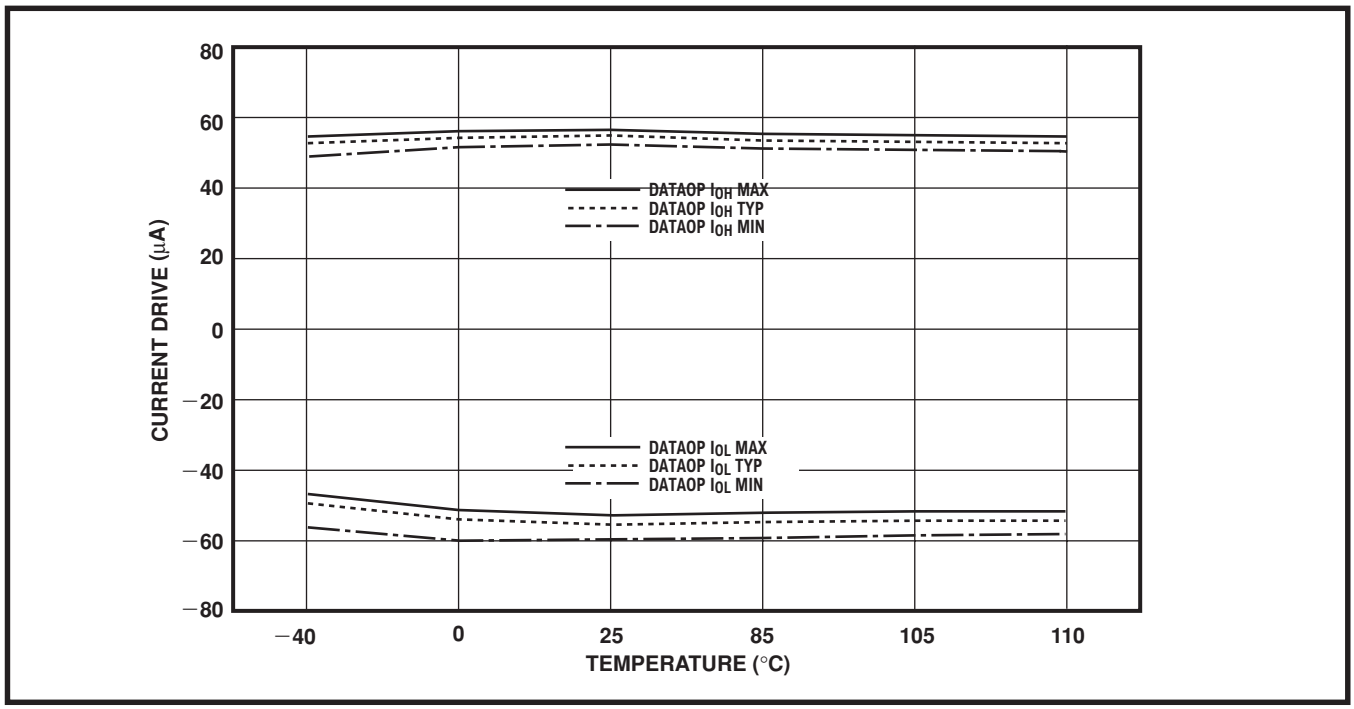


Figure 21 DATAOP I/O current drive at ±20μA (see Baseband, page 13)

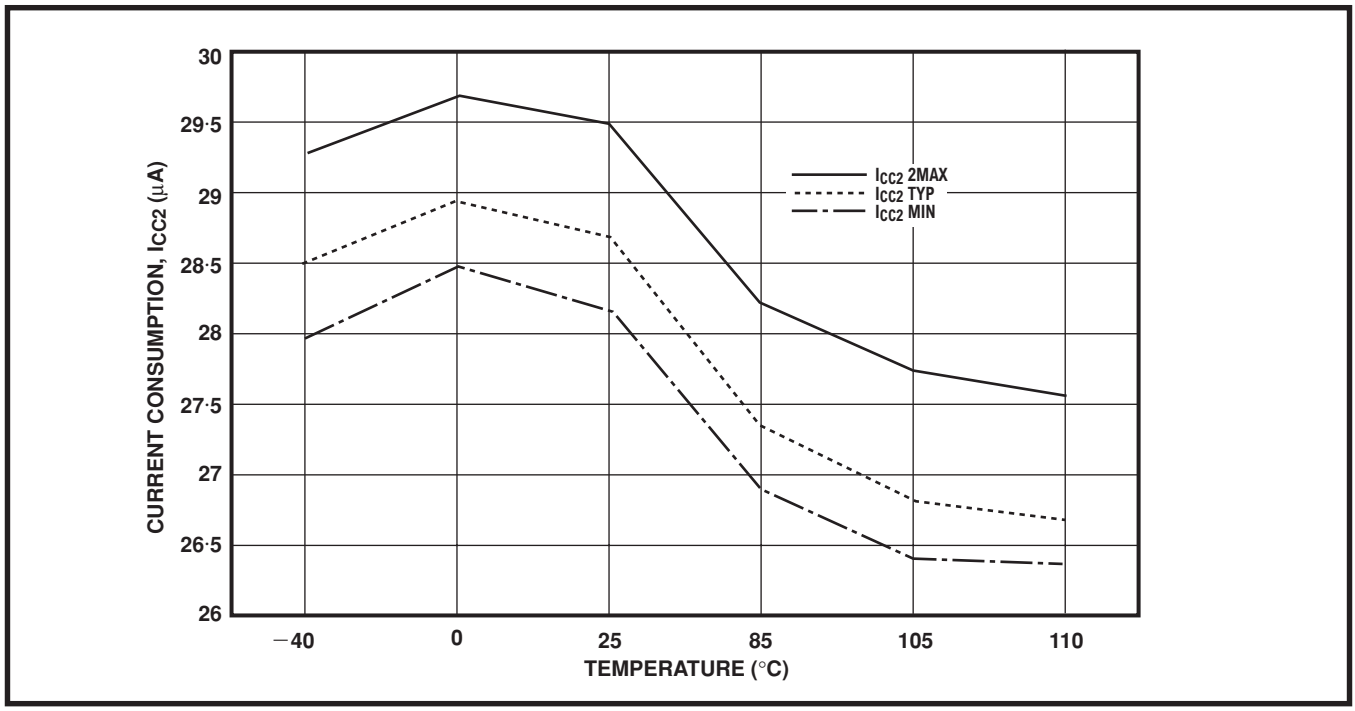


Figure 22 Receiver current consumption in PD0 mode, DC Electrical Characteristics, page 7

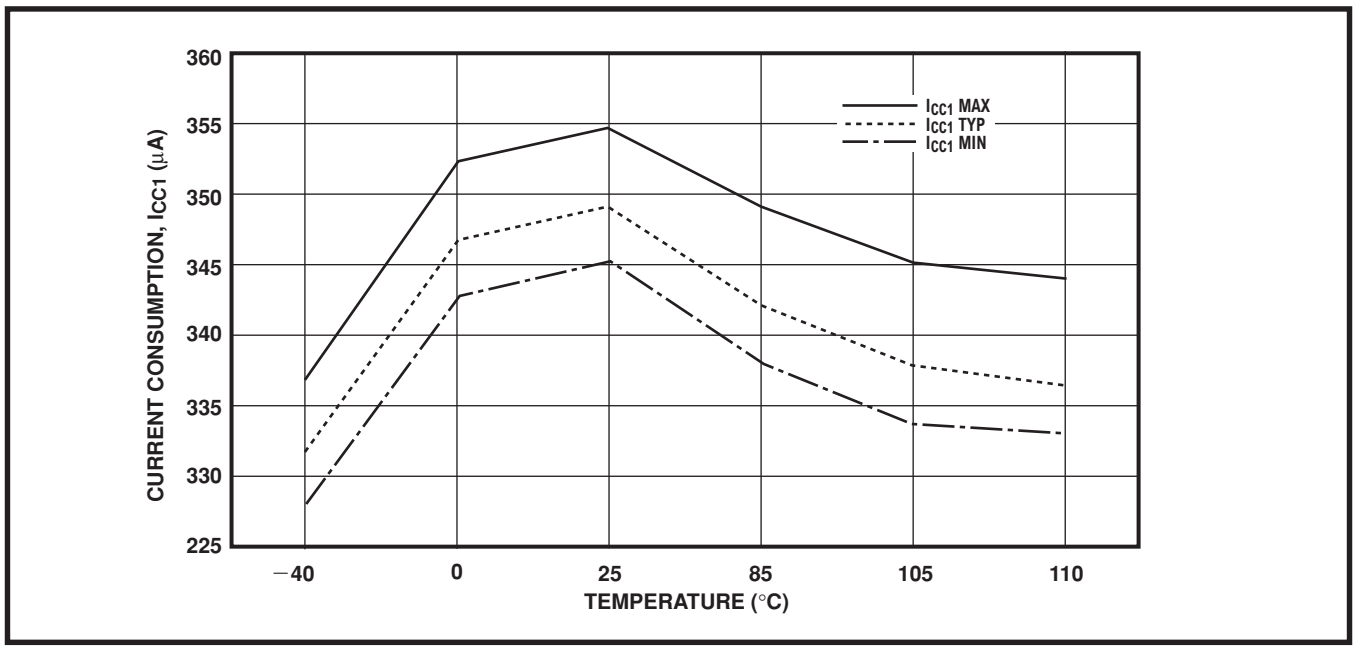


Figure 23 Receiver current consumption in PD1 mode, DC Electrical Characteristics, page 7

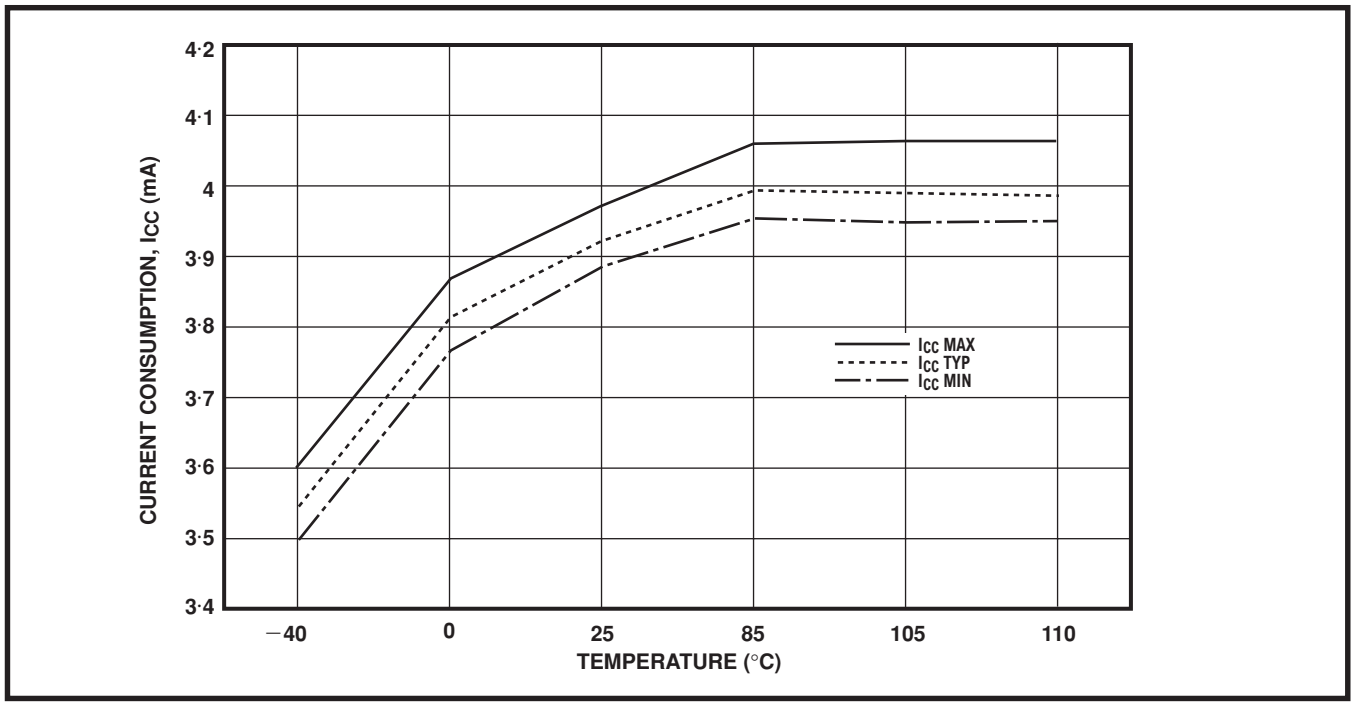


Figure 24 Receiver current consumption in PD2 mode, DC Electrical Characteristics, page 7

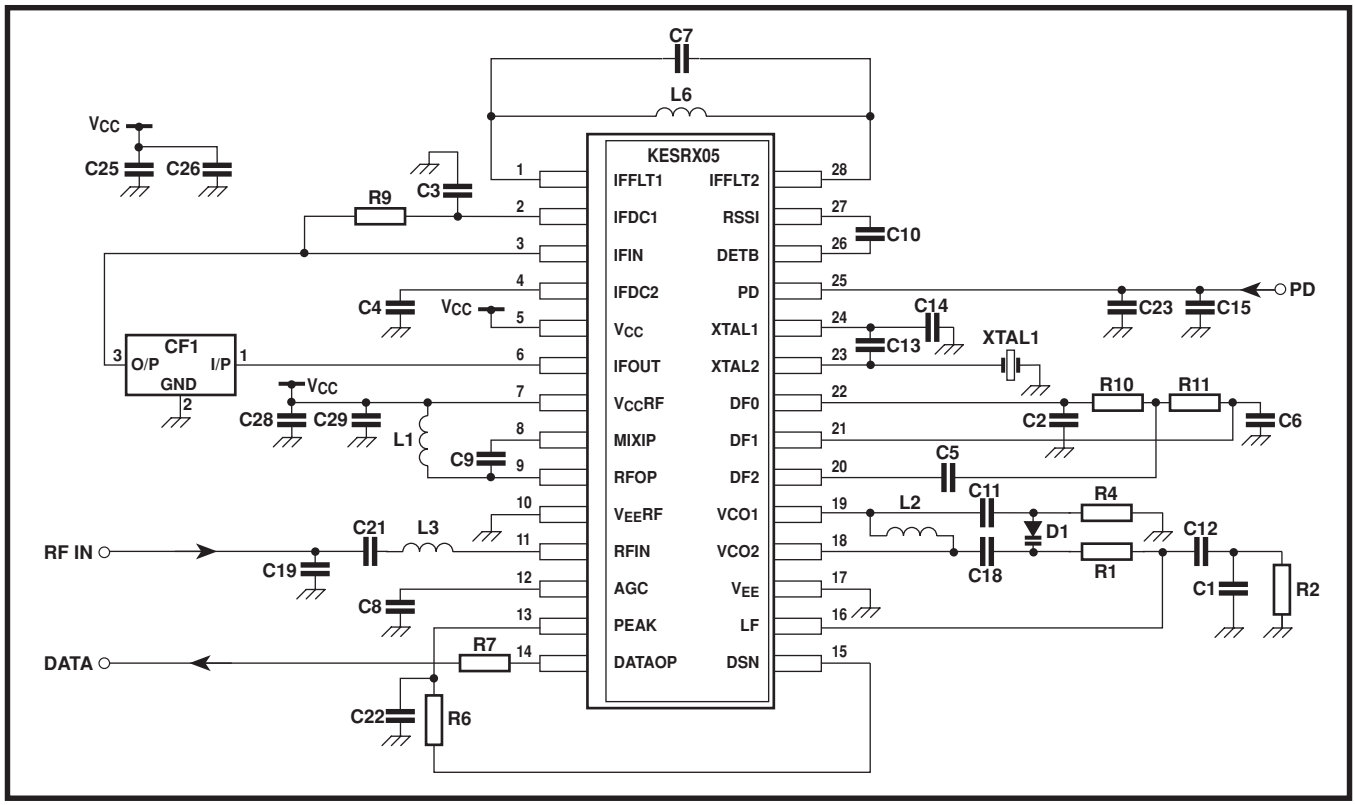


Figure 25 Application circuit diagram for KESRX05 with NO SAW filter

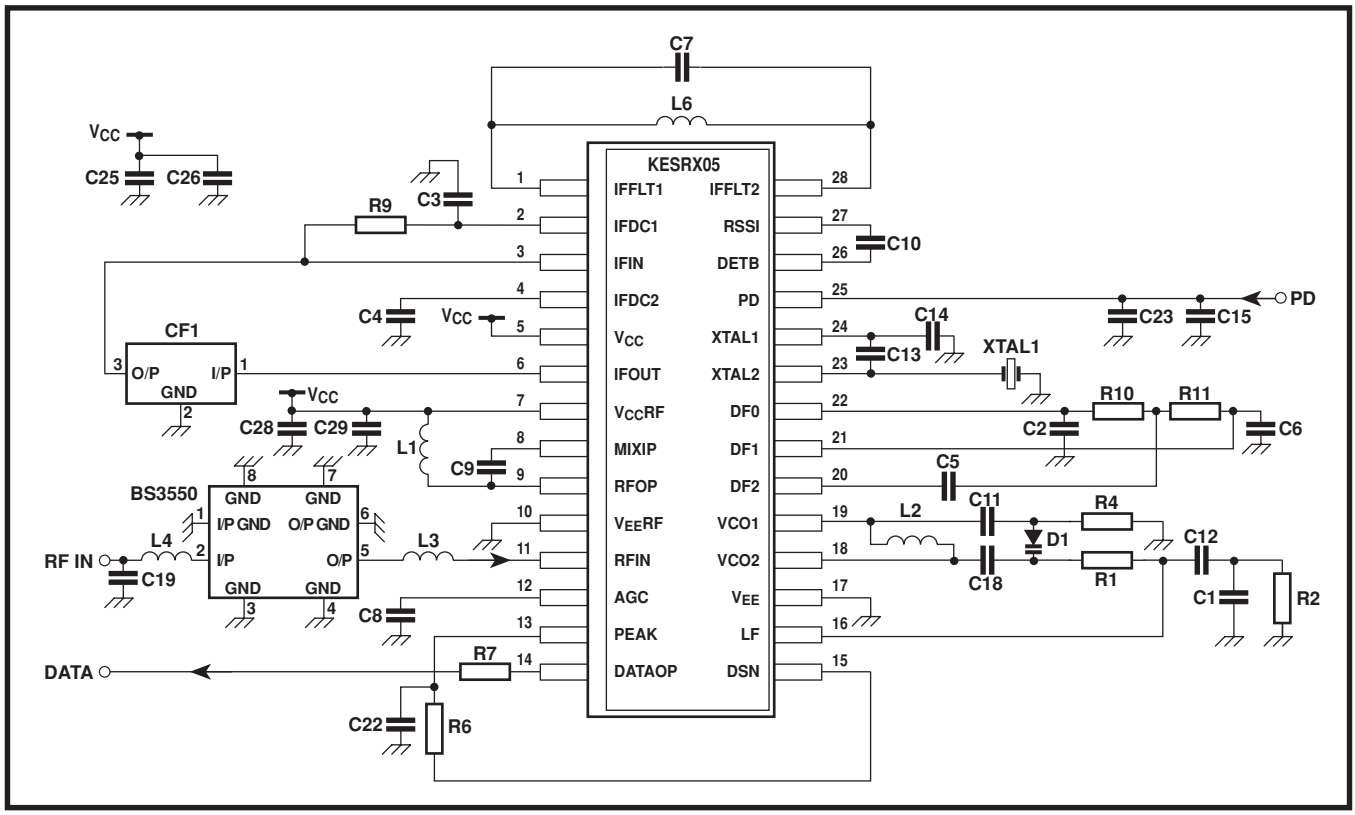
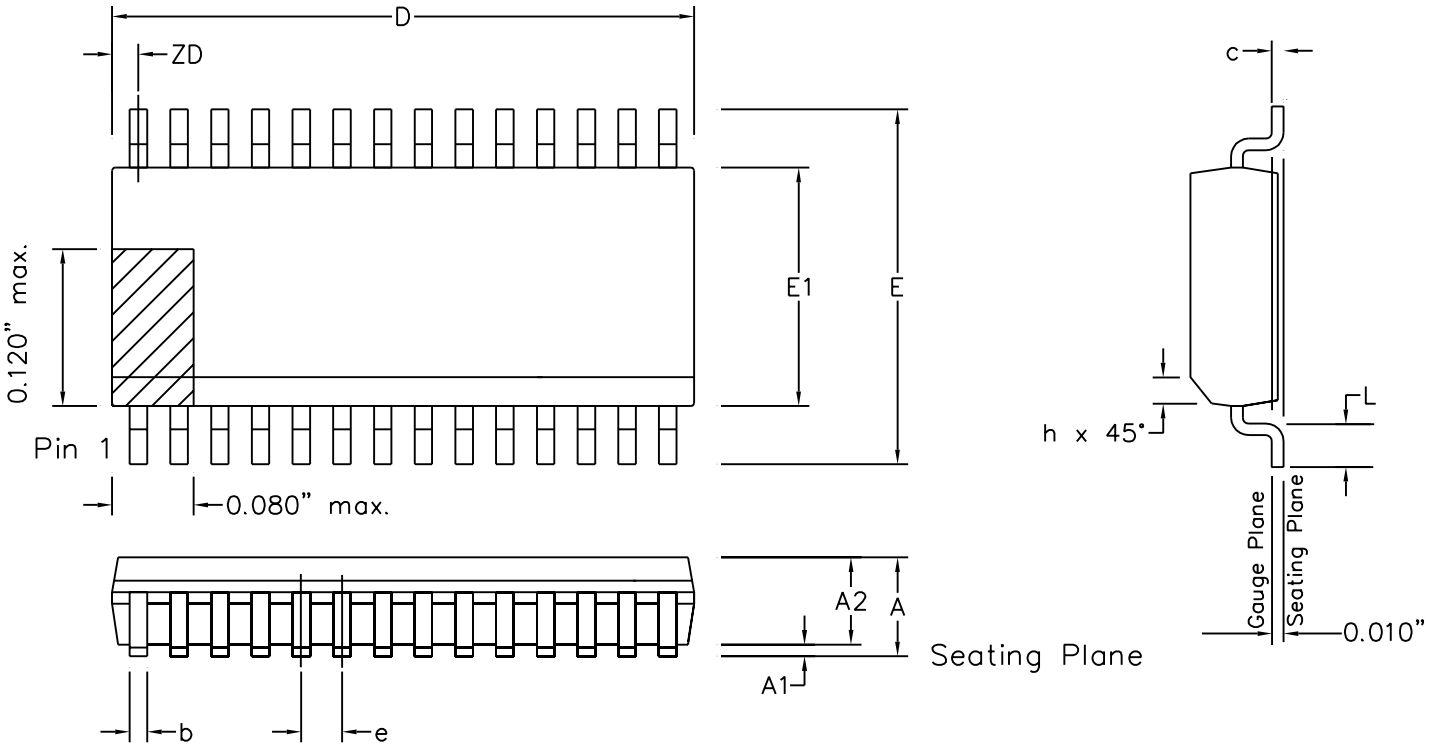


Figure 26 Application circuit diagram for KESRX05 with SAW filter

Ident	Value	Part No./tolerance	Supplier	Size
C1	150ph	GRM39C0G151J	Murata	0603
C2	270pF	GRM39C0G271J	Murata	0603
C3	10nF	GRM39X7R103K	Murata	0603
C4	10nF	GRM39X7R103K	Murata	0603
C5	270pF	GRM39SL271J	Murata	0603
C6	270pF	GRM39SL271J	Murata	0603
C7 (1)	47pF	GRM39COG470G	Murata	0603
C8	10nF	GRM39Y5V103K	Murata	0603
C9	56pF	GRM39COG560J	Murata	0603
C10	1μF	GRM40Y5V105Z	Murata	0805
C11 (1)	12pF	GRM39COG120J	Murata	0603
C12	1·5nF	GRM39X7R152K	Murata	0603
C13	18pF	GRM39COG180J	Murata	0603
C14	18pF	G RM39COG180J	Murata	0603
C15	100pF	GRM39COG101J	Murata	0603
C18 (1)	12pF	GRM39COG120J	Murata	0603
C19 (2)	2pF	GRM39COG2R0C	Murata	0603
C21 (3)	220pF	GRM39COG221J	Murata	0603
C22	1μF	GRM40Y5V105Z	Murata	0805
C23	100pF	GRM39COG101J	Murata	0603
C25	100pF	GRM39COG101J	Murata	0603
C26	1μF	GRM40Y5V105Z	Murata	0805
C28	1μF	GRM40Y5V105Z	Murata	0805
C29	100pF	GRM39COG101J	Murata	0603
R1	4.7kΩ	N/A	Rohm	0603
R2	10kΩ	N/A	Rohm	0603
R4	4.7kΩ	N/A	Rohm	0603
R6	100kΩ	N/A	Rohm	0805
R7	100kΩ	N/A	Rohm	0603
R9 (1)	360Ω	N/A	Rohm	0603
R10	100kΩ	N/A	Rohm	0603
R11	100kΩ	N/A	Rohm	0603
D1	BB833	4 to 10pF	Siemens	SOD323
CF1 (1)	SFE10.7MA26	3dB BW = 230kHz	Murata	Radial
SAWF	B3550	3dB BW = 230kHz	TOKO	5mm^2
L1 (2)	39nH	LL2012-F39NJ	TOKO	2012
L2 (2)	27nH	LL2012-F27NJ	TOKO	2012
L3 (2, 3)	68nH	LL2012-F68NJ	TOKO	1608
L3 (1,3)	100nH	LL1608-FHR10J	TOKO	1608
L4 (2,4)	33nH	LL2012-F33NJ	TOKO	2021
L5 (1)	4.7μH	FLU25204R7J	TOKO	2520
XTAL1 (2)	6·61281MHz	±100 PPM	Kinseki / Quartz Tek	HC49/4H
KESRX05			Mitel Semiconductor	QP28

Table 5 Components for Figures 25 and 26

NOTES
1. Adjust for alternative IF/ceramic filter.
2. Adjust for alternative centre frequency.
3. Without SAW filter (Figure 25).
4. With SAW filter (Figure 26).



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.386	0.394	9.80	10.01
ZD	0.033 REF.		0.84 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	28			
Conforms to JEDEC MO-137AF Iss. A				

This drawing supersedes
418/ED/51617/004 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
QP / Q

Package Code DG

Package Outline for 28 lead QSOP (0.150" Body Width)

GPD00292

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