Features

- High Performance, Low Power AVR®32 UC 32-Bit Microcontroller
  - Compact Single-cycle RISC Instruction Set Including DSP Instruction Set
  - Read-Modify-Write Instructions and Atomic Bit Manipulation
  - Up to 66 MHz Clock Frequency with 1.24 DMIPS/MHz
  - Memory Protection Unit
- Multi-hierarchy Bus System
  - High-Performance Data Transfers on Separate Buses for Increased Performance
  - 15 Peripheral DMA Channels for Automatic Data Transfer
- Internal High-Speed Flash
  - 512K Bytes, 256K Bytes, 128K Bytes Versions
  - Single Cycle Access up to 30 MHz
  - Prefetch Buffer Optimizing Instruction Execution at Maximum Speed
  - 1ms Page Programming Time and 2ms Full-Chip Erase Time
  - 100,000 Write Cycles, 10-year Data Retention Capability
  - Flash Security Locks and User Defined Configuration Area
- Internal High-Speed SRAM, Single-Cycle Access at Full Speed
  - 64K Bytes (512KB and 256KB Flash), 32K Bytes (128KB Flash)
- External Memory Interface on AT32UC3A0 Derivatives
  - SDRAM / SRAM Compatible Memory Bus (16-bit Data and 24-bit Address Buses)
- Interrupt Controller
  - Autovectored Low Latency Interrupt Service with Programmable Priority
- System Functions
  - Power and Clock Manager Including Internal RC Clock and One 32KHz Oscillator
  - Two Multipurpose Oscillators and Two Phase-Lock-Loop (PLL)
  - Watchdog Timer, Real-Time Clock Timer
- Universal Serial Bus (USB)
  - Device 2.0 Full Speed and On-The-Go (OTG) Low Speed and Full Speed
  - Flexible End-Point Configuration and Management with Dedicated DMA Channels
  - On-chip Transceivers Including Pull-Ups
- Ethernet MAC 10/100 Mbps interface
  - 802.3 Ethernet Media Access Controller
  - Supports Media Independent Interface (MII) and Reduced MII (RMII)
- One Three-Channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, PWM, Capture and Various Counting Capabilities
- One 7-Channel 16-bit Pulse Width Modulation Controller (PWM)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Independant Baudrate Generator, Support for IrDA and ISO7816 interfaces
  - Support for Hardware Handshaking, RS485 Interfaces and Modem Line
- Two Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals
- One Synchronous Serial Protocol Controller
  - Supports I2S and Generic Frame-Based Protocols
- One Master/Slave Two-Wire Interface (TWI), 400kbit/s I2C-compatible
- One 8-channel 10-bit Analog-To-Digital Converter
- On-Chip Debug System (JTAG interface)
  - Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace
- 100-pin TQFP (69 GPIO pins), 144-pin LQFP (109 GPIO pins)
- 5V Input Tolerant I/Os
- Single 3.3V Power Supply

AVR®32 32-Bit Microcontroller

AT32UC3A0512
AT32UC3A0256
AT32UC3A0128
AT32UC3A1512
AT32UC3A1256
AT32UC3A1128

Preliminary

Summary

32058AS–AVR32–03/07

1. Description

The AT32UC3A is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 66 MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A incorporates on-chip Flash and SRAM memories for secure and fast access. For applications requiring additional memory, an external memory interface is provided on AT32UC3A0 derivatives.

The Peripheral Direct Memory Access controller enables data transfers between peripherals and memories without processor involvement. PDCA drastically reduces processing overhead when transferring continuous and large data streams between modules within the MCU.

The PowerManager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The Timer/Counter includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The PWM modules provides seven independent channels with many configuration options including polarity, edge alignment and waveform non overlap control. One PWM channel can trigger ADC conversions for more accurate close loop control implementations.

The AT32UC3A also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like UART, SPI or TWI, other interfaces like flexible Synchronous Serial Controller, USB and Ethernet MAC are available.

The Synchronous Serial Controller provides easy access to serial communication protocols and audio standards like I2S.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration. The On-The-GO (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor.

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC module provides on-chip solutions for network-connected devices.

AT32UC3A integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

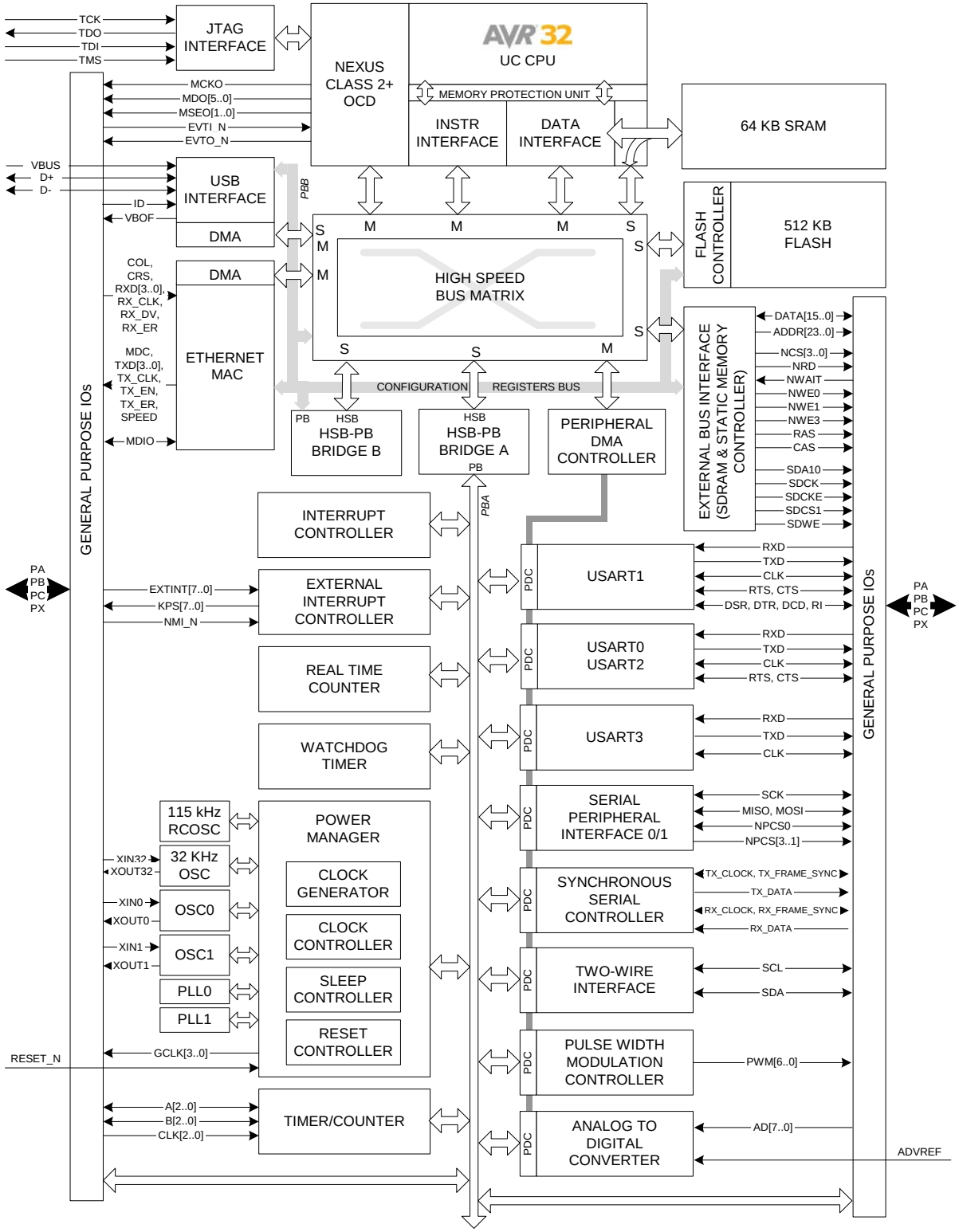
2. Configuration Summary

The table below lists all AT32UC3A memory and package configurations:

Device	Flash	SRAM	Ext. Bus Interface	Package
AT32UC3A0512	512 Kbytes	64 Kbytes	yes	144 lead LQFP
AT32UC3A1512	512 Kbytes	64 Kbytes	no	100 lead TQFP
AT32UC3A0256	256 Kbytes	64 Kbytes	yes	144 lead LQFP
AT32UC3A1256	256 Kbytes	64 Kbytes	no	100 lead TQFP
AT32UC3A0128	128 Kbytes	32 Kbytes	yes	144 lead LQFP
AT32UC3A1128	128 Kbytes	32 Kbytes	no	100 lead TQFP

3. Blockdiagram

Figure 3-1. Blockdiagram



3.1 Processor and architecture

3.1.1 AVR32 UC CPU

- 32-bit load/store AVR32A RISC architecture.
  - 15 general-purpose 32-bit registers.
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
  - Fully orthogonal instruction set.
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
  - Innovative instruction set together with variable instruction length ensuring industry leading code density.
  - DSP extention with saturating arithmetic, and a wide variety of multiply instructions.
- 3 stage pipeline allows one instruction per clock cycle for most instructions.
  - Byte, half-word, word and double word memory access.
  - Multiple interrupt priority levels.
- MPU allows for operating systems with memory protection.

3.1.2 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 2+
  - Low-cost NanoTrace supported.
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

3.1.3 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Fifteen channels
  - Two for each USART
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for each ADC
  - Two for each TWI Interface

3.1.4 Bus system

- High Speed Bus (HSB) matrix with 6 Masters and 6 Slaves handled
  - Handles Requests from the CPU Data Fetch, CPU Instruction Fetch, PDCA, USBB, Ethernet Controller, CPU SAB, and to internal Flash, internal SRAM, Peripheral Bus A, Peripheral Bus B, EBI.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
  - One Address Decoder Provided per Master

- **Peripheral Bus A able to run on at divided bus speeds compared to the High Speed Bus**

Figure 3-1 gives an overview of the bus system. All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the High Speed Bus, and which DMA controller is connected to which peripheral.

4. Signals Description

The following table gives details on the signal name classified by peripheral

The signals are multiplexed with GPIO pins as described in ”Peripheral Multiplexing on I/O lines” on page 25.

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDSYS	Power supply for PLL and ADC	Power		1.65 to 1.95 V
VDDCORE	Core Power Supply	Power		1.65 to 1.95 V
VDDIO	I/O Power Supply	Power		3.0 to 3.6V
VDDANA	Analog Power Supply	Power		3.0 to 3.6V
VDDIN	Voltage Regulator Input Supply	Power		3.0 to 3.6V
VDDOUT	Voltage Regulator Output	Power Output		1.65 to 1.95 V
GNDANA	Analog Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators, and PLL’s				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO0 - MDO5	Trace Data Output	Output		
MSEO0 - MSEO1	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Manager - PM				
GCLK0 - GCLK3	Generic Clock Pins	Output		
RESET_N	Reset Pin	Input	Low	
Real Time Counter - RTC				
RTC_CLOCK	RTC clock	Output		
Watchdog Timer - WDT				
WDTEXT	External Watchdog Pin	Output		
External Interrupt Controller - EIC				
EXTINT0 - EXTINT7	External Interrupt Pins	Input		
KPS0 - KPS7	Keypad Scan Pins	Output		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
Ethernet MAC - MACB				
COL	Collision Detect	Input		
CRS	Carrier Sense and Data Valid	Input		
MDC	Management Data Clock	Output		
MDIO	Management Data Input/Output	I/O		
RXD0 - RXD3	Receive Data	Input		
RX_CLK	Receive Clock	Input		
RX_DV	Receive Data Valid	Input		
RX_ER	Receive Coding Error	Input		
SPEED	Speed			
TXD0 - TXD3	Transmit Data	Output		
TX_CLK	Transmit Clock or Reference Clock	Output		
TX_EN	Transmit Enable	Output		
TX_ER	Transmit Coding Error	Output		
External Bus Interface - HEBI - uC3015 Only				
ADDR0 - ADDR23	Address Bus	Output		
CAS	Column Signal	Output	Low	

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DATA0 - DATA15	Data Bus	I/O		
NCS0 - NCS3	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
NWE3	Write Enable 3	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDCS0-SDCS1	SDRAM Chip Select	Output	Low	
SDWE	SDRAM Write Enable	Output	Low	
General Purpose Input/Output 2 - GPIOA, GPIOB, GPIOC				
P0 - P31	Parallel I/O Controller GPIOA	I/O		
P0 - P31	Parallel I/O Controller GPIOB	I/O		
P0 - P5	Parallel I/O Controller GPIOC	I/O		
P0 - P31	Parallel I/O Controller GPIOX	I/O		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
Timer/Counter - TIMER				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		Only USART0, USART1
DCD	Data Carrier Detect			Only USART0
DSR	Data Set Ready			Only USART0
DTR	Data Terminal Ready			Only USART0
RI	Ring Indicator			Only USART0
RTS	Request To Send	Output		Only USART0, USART1
RXD	Receive Data	Input		
RXDN	Inverted Receive Data	Input	Low	
TXD	Transmit Data	Output		
TXDN	Inverted Transmit Data	Output	Low	
Analog to Digital Converter - ADC				

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
AD0 - AD7	Analog input pins	Analog input		
ADVREF	Analog positive reference voltage input	Analog input		2.6 to 3.6V
Pulse Width Modulator - PWM				
PWM0 - PWM6	PWM Output Pins	Output		
Universal Serial Bus Device - USB				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		

5. Package and Pinout

The device pins are multiplexed with peripheral functions as described in ”Peripheral Multiplexing on I/O lines” on page 25.

Figure 5-1. TQFP100 Pinout

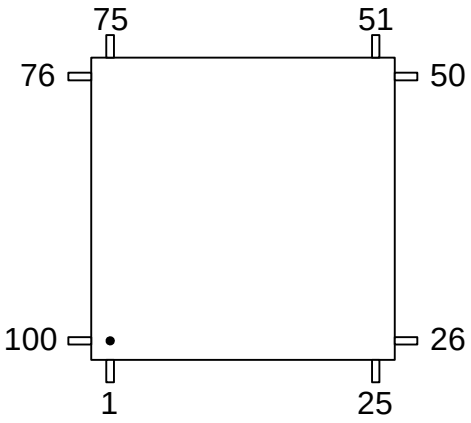


Table 5-1. TQFP100 Package Pinout

1	PB20	**26**	PA05	**51**	PA21	**76**	PB08
2	PB21	**27**	PA06	**52**	PA22	**77**	PB09
3	PB22	**28**	PA07	**53**	PA23	**78**	PB10
4	VDDIO	**29**	PA08	**54**	PA24	**79**	VDDIO
5	GND	**30**	PA09	**55**	PA25	**80**	GND
6	PB23	**31**	PA10	**56**	PA26	**81**	PB11
7	PB24	**32**	N/C	**57**	PA27	**82**	PB12
8	PB25	**33**	PA11	**58**	PA28	**83**	PA29
9	PB26	**34**	VDDCORE	**59**	VDDANA	**84**	PA31
10	PB27	**35**	GND	**60**	ADVREF	**85**	PC02
11	VDDOUT	**36**	PA12	**61**	GNDANA	**86**	PC03
12	VDDIN	**37**	PA13	**62**	VDDSYS	**87**	PB13
13	GND	**38**	VDDCORE	**63**	PC00	**88**	PB14
14	PB28	**39**	PA14	**64**	PC01	**89**	TMS
15	PB29	**40**	PA15	**65**	PB00	**90**	TCK
16	PB30	**41**	PA16	**66**	PB01	**91**	TDO
17	PB31	**42**	PA17	**67**	VDDIO	**92**	TDI
18	RESET_N	**43**	PA18	**68**	VDDIO	**93**	PC04
19	PA00	**44**	PA19	**69**	GND	**94**	PC05
20	PA01	**45**	PA20	**70**	PB02	**95**	PB15
21	GND	**46**	VBUS	**71**	PB03	**96**	PB16
22	VDDCORE	**47**	VDDIO	**72**	PB04	**97**	VDDCORE

Table 5-1. TQFP100 Package Pinout

23	PA02	**48**	DM	**73**	PB05	**98**	PB17
24	PA03	**49**	DP	**74**	PB06	**99**	PB18
25	PA04	**50**	GND	**75**	PB07	**100**	PB19

Figure 5-2. LQFP144 Pinout

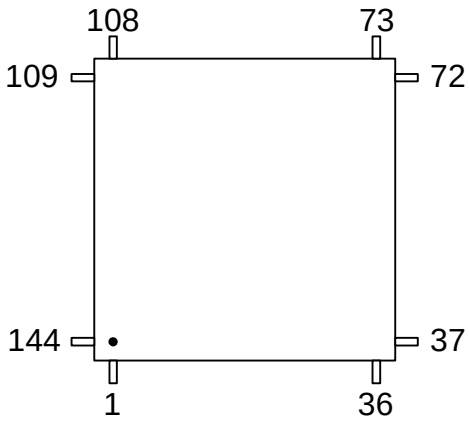


Table 5-2. VQFP144 Package Pinout

1	PX00	**37**	GND	**73**	PA21	**109**	GND
2	PX01	**38**	PX10	**74**	PA22	**110**	PX30
3	PB20	**39**	PA05	**75**	PA23	**111**	PB08
4	PX02	**40**	PX11	**76**	PA24	**112**	PX31
5	PB21	**41**	PA06	**77**	PA25	**113**	PB09
6	PB22	**42**	PX12	**78**	PA26	**114**	PX32
7	VDDIO	**43**	PA07	**79**	PA27	**115**	PB10
8	GND	**44**	PX13	**80**	PA28	**116**	VDDIO
9	PB23	**45**	PA08	**81**	VDDANA	**117**	GND
10	PX03	**46**	PX14	**82**	ADVREF	**118**	PX33
11	PB24	**47**	PA09	**83**	GNDANA	**119**	PB11
12	PX04	**48**	PA10	**84**	VDDSYS	**120**	PX34
13	PB25	**49**	N/C	**85**	PC00	**121**	PB12
14	PB26	**50**	PA11	**86**	PC01	**122**	PA29
15	PB27	**51**	VDDCORE	**87**	PX20	**123**	PA31
16	VDDOUT	**52**	GND	**88**	PB00	**124**	PC02
17	VDDIN	**53**	PA12	**89**	PX21	**125**	PC03
18	GND	**54**	PA13	**90**	PB01	**126**	PB13
19	PB28	**55**	VDDCORE	**91**	PX22	**127**	PB14
20	PB29	**56**	PA14	**92**	VDDIO	**128**	TMS
21	PB30	**57**	PA15	**93**	VDDIO	**129**	TCK

Table 5-2. VQFP144 Package Pinout

22	PB31	**58**	PA16	**94**	GND	**130**	TDO
23	RESET_N	**59**	PX15	**95**	PX23	**131**	TDI
24	PX05	**60**	PA17	**96**	PB02	**132**	PC04
25	PA00	**61**	PX16	**97**	PX24	**133**	PC05
26	PX06	**62**	PA18	**98**	PB03	**134**	PB15
27	PA01	**63**	PX17	**99**	PX25	**135**	PX35
28	GND	**64**	PA19	**100**	PB04	**136**	PB16
29	VDDCORE	**65**	PX18	**101**	PX26	**137**	PX36
30	PA02	**66**	PA20	**102**	PB05	**138**	VDDCORE
31	PX07	**67**	PX19	**103**	PX27	**139**	PB17
32	PA03	**68**	VBUS	**104**	PB06	**140**	PX37
33	PX08	**69**	VDDIO	**105**	PX28	**141**	PB18
34	PA04	**70**	DM	**106**	PB07	**142**	PX38
35	PX09	**71**	DP	**107**	PX29	**143**	PB19
36	VDDIO	**72**	GND	**108**	VDDIO	**144**	PX39

6. Power Considerations

6.1 Power Supplies

The AT32UC3A has several types of power supply pins:

- **VDDIO: Powers I/O lines. Voltage is 3.3V nominal.**
- **VDDANA: Powers the ADC Voltage is 3.3V nominal.**
- **VDDIN: Input voltage for the voltage regulator. Voltage is 3.3V nominal.**
- **VDDCORE: Powers the core, memories, and peripherals. Voltage is 1.8V nominal.**
- **VDDSYS: Powers the PLL and ADC. Voltage is 1.8V nominal.**

The ground pins GND are common to VDDCORE and VDDIO. The ground pin for VDDANA and VDDSYS is GNDANA.

See ”Electrical Characteristics” on page 33 for power consumption on the various supply pins.

6.2 Voltage Regulator

The AT32UC3A embeds a voltage regulator that converts from 3.3V to 1.8V with a load of up to 100 mA. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDOUT. VDDOUT should be externally connected to the 1.8V domains to be powered.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

7. I/O Line Considerations

7.1 JTAG pins

TMS, TDI and TCK have pull-up resistors. TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

7.2 RESET_N pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

7.3 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

7.4 GPIO pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column “Reset State” of the GPIO Controller multiplexing tables.

8. Memories

8.1 Embedded Memories

- **Internal High-Speed Flash**
  - **512 KBytes (AT32UC3A0512, AT32UC3A1512)**
  - **256 KBytes (AT32UC3A0256, AT32UC3A1256)**
  - **128 KBytes (AT32UC3A1128)**
    - **0 Wait State Access at up to 30 MHz in Worst Case Conditions**
    - **1 Wait State Access at up to 60 MHz in Worst Case Conditions**
    - **Pipelined Flash Architecture, allowing burst reads from sequential Flash locations, hiding penalty of 1 wait state access**
    - **Pipelined Flash Architecture typically reduces the cycle penalty of 1 wait state operation to only 15% compared to 0 wait state operation**
    - **10 000 Write Cycles, 10-year Data Retention Capability**
    - **1 ms Page Programming Time, 2 ms Chip Erase Time**
    - **Sector Lock Capabilities, Bootloader Protection, Security Bit**
    - **64 Fuses, 32 Of Which Are Preserved During Chip Erase**
    - **User Page For Data To Be Preserved During Chip Erase**
- **Internal High-Speed SRAM, Single-cycle access at full speed**
  - **64 KBytes (AT32UC3A0512, AT32UC3A0, AT32UC3A0256 & AT32UC3A1256)**
  - **32KBytes (AT32UC3A1128)**

8.2 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AVR32 UC CPU uses unsegmented translation, as described in the AVR32 Architecture Manual. The 32-bit physical address space is mapped as follows:

Table 8-1. AT32UC3A Physical Memory Map

Start Address	Size					Device
	AT32UC3A0512	AT32UC3A1512	AT32UC3A0256	AT32UC3A1256	AT32UC3A1128	
0x0000_0000	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	32 Kbyte	Embedded SRAM
0x8000_0000	512 Kbyte	512 Kbyte	256 Kbyte	256 Kbyte	128 Kbyte	Embedded Flash
0xC000_0000	16 Mbyte	-	16 Mbyte	-	-	EBI SRAM CS0
0xC800_0000	16 Mbyte	-	16 Mbyte	-	-	EBI SRAM CS2
0xCC00_0000	16 Mbyte	-	16 Mbyte	-	-	EBI SRAM CS3
0xD000_0000	128 Mbyte	-	128 Mbyte	-	-	EBI SRAM/SDRAM CS1
0xE000_0000	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	USB Configuration
0xFFFE_0000	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	HSB-PB Bridge A
0xFFFF_0000	64 Kbyte	64 Kbyte	64 kByte	64 kByte	64 Kbyte	HSB-PB Bridge B

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table

below can be used to index the HMATRIX control registers. For example, MCFG0 is associated with the CPU Data master interface.

Table 8-2. High Speed Bus masters

Master 0	CPU Data
Master 1	CPU Instruction
Master 2	CPU SAB
Master 3	PDCA
Master 4	MACB DMA
Master 5	USBB DMA

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

Table 8-3. High Speed Bus slaves

Slave 0	Internal Flash
Slave 1	HSB-PB Bridge 0
Slave 2	HSB-PB Bridge 1
Slave 3	Internal SRAM Slave
Slave 4	USBB Slave
Slave 5	EBI

9. Peripherals

9.1 Peripheral address map

Table 9-1. Peripheral Address Mapping

Address		Peripheral Name	Bus
0xE0000000	USBB	USBB Slave Interface - USBB	HSB
0xFFFE0000	USBB	USBB Configuration Interface - USBB	PBB
0xFFFE1000	HMATRIX	HMATRIX Configuration Interface - HMATRIX	PBB
0xFFFE1400	FLASHC	Flash Controller - FLASHC	PBB
0xFFFE1800	MACB	MACB Configuration Interface - MACB	PBB
0xFFFE1C00	SMC	Static Memory Controller Configuration Interface - SMC	PBB
0xFFFE2000	SDRAMC	SDRAM Controller Configuration Interface - SDRAMC	PBB
0xFFFF0000	PDCA	Peripheral DMA Interface - PDCA	PBA
0xFFFF0800	INTC	Interrupt Controller Interface - INTC	PBA
0xFFFF0C00	PM	Power Manager - PM	PBA
0xFFFF0D00	RTC	Real Time Clock - RTC	PBA
0xFFFF0D30	WDT	WatchDog Timer - WDT	PBA
0xFFFF0D80	EIC	External Interrupt Controller - EIC	PBA
0xFFFF1000	GPIO	General Purpose IO Controller - GPIO	PBA
0xFFFF1400	USART0	Universal Synchronous Asynchronous Receiver Transmitter - USART0	PBA
0xFFFF1800	USART1	Universal Synchronous Asynchronous Receiver Transmitter - USART1	PBA

Table 9-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFFF1C00	USART2	Universal Synchronous Asynchronous Receiver Transmitter - USART2	PBA
0xFFFF2000	USART3	Universal Synchronous Asynchronous Receiver Transmitter - USART3	PBA
0xFFFF2400	SPI0	Serial Peripheral Interface - SPI0	PBA
0xFFFF2800	SPI1	Serial Peripheral Interface - SPI1	PBA
0xFFFF2C00	TWI	Two Wire Interface - TWI	PBA
0xFFFF3000	PWM	Pulse Width Modulation Controller - PWM	PBA
0xFFFF3400	SSC	Synchronous Serial Controller - SSC	PBA
0xFFFF3800	TC	Timer/Counter - TC	PBA
0xFFFF3C00	ADC	Analog To Digital Converter - ADC	PBA

9.2 Interrupt Request Signal Map

The various modules may output Interrupt request signals. These signals are routed to the Interrupt Controller (INTC), described in a later chapter. The Interrupt Controller supports up to 64 groups of interrupt requests. Each group can have up to 32 interrupt request signals. All interrupt signals in the same group share the same autovector address and priority level. Refer to the documentation for the individual submodules for a description of the semantic of the different interrupt requests.

The interrupt request signals are connected to the INTC as follows.

Table 9-2. Interrupt Request Signal Map

Group	Line	Module	Signal
0	0	Peripheral DMA Controller	PDCA 16

Table 9-2. Interrupt Request Signal Map

1	0	External Interrupt Controller	EIC 0
	1	External Interrupt Controller	EIC 1
	2	External Interrupt Controller	EIC 2
	3	External Interrupt Controller	EIC 3
	4	External Interrupt Controller	EIC 4
	5	External Interrupt Controller	EIC 5
	6	External Interrupt Controller	EIC 6
	7	External Interrupt Controller	EIC 7
	8	Real Time Counter	RTC
	9	Power Manager	PM
2	0	General Purpose Input/Output Controller	GPIO 0
	1	General Purpose Input/Output Controller	GPIO 1
	2	General Purpose Input/Output Controller	GPIO 2
	3	General Purpose Input/Output Controller	GPIO 3
	4	General Purpose Input/Output Controller	GPIO 4
	5	General Purpose Input/Output Controller	GPIO 5
	6	General Purpose Input/Output Controller	GPIO 6
	7	General Purpose Input/Output Controller	GPIO 7
	8	General Purpose Input/Output Controller	GPIO 8
	9	General Purpose Input/Output Controller	GPIO 9
	10	General Purpose Input/Output Controller	GPIO 10
	11	General Purpose Input/Output Controller	GPIO 11
	12	General Purpose Input/Output Controller	GPIO 12
	13	General Purpose Input/Output Controller	GPIO 13

Table 9-2. Interrupt Request Signal Map

3	0	Peripheral DMA Controller	PDCA 0
	1	Peripheral DMA Controller	PDCA 1
	2	Peripheral DMA Controller	PDCA 2
	3	Peripheral DMA Controller	PDCA 3
	4	Peripheral DMA Controller	PDCA 4
	5	Peripheral DMA Controller	PDCA 5
	6	Peripheral DMA Controller	PDCA 6
	7	Peripheral DMA Controller	PDCA 7
	8	Peripheral DMA Controller	PDCA 8
	9	Peripheral DMA Controller	PDCA 9
	10	Peripheral DMA Controller	PDCA 10
	11	Peripheral DMA Controller	PDCA 11
	12	Peripheral DMA Controller	PDCA 12
	13	Peripheral DMA Controller	PDCA 13
	14	Peripheral DMA Controller	PDCA 14
4	0	Flash Controller	FLASHC
5	0	Universal Synchronous Asynchronous Receiver Transmitter	USART0
6	0	Universal Synchronous Asynchronous Receiver Transmitter	USART1
7	0	Universal Synchronous Asynchronous Receiver Transmitter	USART2
8	0	Universal Synchronous Asynchronous Receiver Transmitter	USART3
9	0	Serial Peripheral Interface	SPI0
10	0	Serial Peripheral Interface	SPI1
11	0	Two-wire Interface	TWI
12	0	Pulse Width Modulation Controller	PWM
13	0	Synchronous Serial Controller	SSC
14	0	Timer/Counter	TC0
	1	Timer/Counter	TC1
	2	Timer/Counter	TC2
15	0	Analog to Digital Converter	ADC
16	0	Ethernet MAC	MACB
17	0	USB Interface	USBB
18	0	SDRAM Controller	SDRAMC

9.3 Clock Connections

9.3.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 9-3. Timer/Counter clock connections

Source	Name	Connection
Internal	TIMER_CLOCK1	clk_slow
	TIMER_CLOCK2	clk_pba / 4
	TIMER_CLOCK3	clk_pba / 8
	TIMER_CLOCK4	clk_pba / 16
	TIMER_CLOCK5	clk_pba / 32
External	XC0	See Section 9.6
	XC1	
	XC2	

9.3.2 USARTs

Each USART can be connected to an internally divided clock:

Table 9-4. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

9.3.3 SPIs

Each SPI can be connected to an internally divided clock:

Table 9-5. SPI clock connections

SPI	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 32
1			

9.4 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible,

depending on the configuration of the OCD AXS register. For details, see the AVR32 UCTechnical Reference Manual.

Table 9-6. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1
EVTI_N	PB19	PA08
MDO[5]	PB16	PA27
MDO[4]	PB14	PA26
MDO[3]	PB13	PA25
MDO[2]	PB12	PA24
MDO[1]	PB11	PA23
MDO[0]	PB10	PA22
EVTO_N	PB20	PB20
MCKO	PB21	PA21
MSEO[1]	PB04	PA07
MSEO[0]	PB17	PA28

9.5 DMA handshake signals

The PDMA and the peripheral modules communicate through a set of handshake signals. The following table defines the valid settings for the Peripheral Identifier (PID) in the PDMA Peripheral Select Register (PSR).

Table 9-7. PDMA Handshake Signals

PID Value	Peripheral module & direction
0	ADC
1	SSC - RX
2	USART0 - RX
3	USART1 - RX
4	USART2 - RX
5	USART3 - RX
6	TWI - RX
7	SPI0 - RX
8	SPI1 - RX
9	SSC - TX
10	USART0 - TX
11	USART1 - TX
12	USART2 - TX
13	USART3 - TX

Table 9-7. PDMA Handshake Signals

PID Value	Peripheral module & direction
14	TWI - TX
15	SPI0 - TX
16	SPI1 - TX

9.6 Peripheral Multiplexing on I/O lines

Each GPIO line can be assigned to one of 3 peripheral functions; A, B or C. The following table define how the I/O lines on the peripherals A, B and C are multiplexed by the GPIO.

Table 9-8. GPIO Controller Function Multiplexing

TQFP100	VQFP144	PIN	GPIO Pin	Function A	Function B	Function C
19	25	PA00	GPIO 0	USART0 - RXD	TC - CLK0	
20	27	PA01	GPIO 1	USART0 - TXD	TC - CLK1	
23	30	PA02	GPIO 2	USART0 - CLK	TC - CLK2	
24	32	PA03	GPIO 3	USART0 - RTS	EIC - EXTINT[4]	
25	34	PA04	GPIO 4	USART0 - CTS	EIC - EXTINT[5]	
26	39	PA05	GPIO 5	USART1 - RXD	PWM - PWM[4]	
27	41	PA06	GPIO 6	USART1 - TXD	PWM - PWM[5]	
28	43	PA07	GPIO 7	USART1 - CLK	PM - GCLK[0]	SPI0 - NPCS[3]
29	45	PA08	GPIO 8	USART1 - RTS	SPI0 - NPCS[1]	EIC - EXTINT[7]
30	47	PA09	GPIO 9	USART1 - CTS	SPI0 - NPCS[2]	
31	48	PA10	GPIO 10	SPI0 - NPCS[0]	EIC - EXTINT[6]	
33	50	PA11	GPIO 11	SPI0 - MISO	USBB - USB_ID	
36	53	PA12	GPIO 12	SPI0 - MOSI	USBB - USB_VBOF	
37	54	PA13	GPIO 13	SPI0 - SCK		
39	56	PA14	GPIO 14	SSC - TX_FRAME_SYNC	SPI1 - NPCS[0]	EBI - NCS[0]
40	57	PA15	GPIO 15	SSC - TX_CLOCK	SPI1 - SCK	EBI - ADDR[20]
41	58	PA16	GPIO 16	SSC - TX_DATA	SPI1 - MOSI	EBI - ADDR[21]
42	60	PA17	GPIO 17	SSC - RX_DATA	SPI1 - MISO	EBI - ADDR[22]
43	62	PA18	GPIO 18	SSC - RX_CLOCK	SPI1 - NPCS[1]	
44	64	PA19	GPIO 19	SSC - RX_FRAME_SYNC	SPI1 - NPCS[2]	
45	66	PA20	GPIO 20	NMI	SPI1 - NPCS[3]	
51	73	PA21	GPIO 21	ADC - AD[0]	EIC - EXTINT[0]	
52	74	PA22	GPIO 22	ADC - AD[1]	EIC - EXTINT[1]	
53	75	PA23	GPIO 23	ADC - AD[2]	EIC - EXTINT[2]	
54	76	PA24	GPIO 24	ADC - AD[3]	EIC - EXTINT[3]	
55	77	PA25	GPIO 25	ADC - AD[4]	EIC - SCAN[0]	EBI - NCS[0]
56	78	PA26	GPIO 26	ADC - AD[5]	EIC - SCAN[1]	EBI - ADDR[20]

Table 9-8. GPIO Controller Function Multiplexing

57	79	PA27	GPIO 27	ADC - AD[6]	EIC - SCAN[2]	EBI - ADDR[21]
58	80	PA28	GPIO 28	ADC - AD[7]	EIC - SCAN[3]	EBI - ADDR[22]
83	122	PA29	GPIO 29	TWI - SDA	USART2 - RTS	
84	123	PA30	GPIO 30	TWI - SCL	USART2 - CTS	
65	88	PB00	GPIO 32	MACB - TX_CLK	USART2 - RTS	
66	90	PB01	GPIO 33	MACB - TX_EN	USART2 - CTS	
70	96	PB02	GPIO 34	MACB - TXD[0]		
71	98	PB03	GPIO 35	MACB - TXD[1]		
72	100	PB04	GPIO 36	MACB - CRS	USART3 - CLK	EBI - NCS[3]
73	102	PB05	GPIO 37	MACB - RXD[0]		
74	104	PB06	GPIO 38	MACB - RXD[1]		
75	106	PB07	GPIO 39	MACB - RX_ER		
76	111	PB08	GPIO 40	MACB - MDC		
77	113	PB09	GPIO 41	MACB - MDIO		
78	115	PB10	GPIO 42	MACB - TXD[2]	USART3 - RXD	EBI - SDCK
81	119	PB11	GPIO 43	MACB - TXD[3]	USART3 - TXD	EBI - SDCKE
82	121	PB12	GPIO 44	MACB - TX_ER	TC - CLK0	EBI - RAS
87	126	PB13	GPIO 45	MACB - RXD[2]	TC - CLK1	EBI - CAS
88	127	PB14	GPIO 46	MACB - RXD[3]	TC - CLK2	EBI - SDWE
95	134	PB15	GPIO 47	MACB - RX_DV		
96	136	PB16	GPIO 48	MACB - COL	USBB - USB_ID	EBI - SDA10
98	139	PB17	GPIO 49	MACB - RX_CLK	USBB - USB_VBOF	EBI - ADDR[23]
99	141	PB18	GPIO 50	MACB - SPEED	ADC - TRIGGER	PWM - PWM[6]
100	143	PB19	GPIO 51	PWM - PWM[0]	PM - GCLK[0]	EIC - SCAN[4]
1	3	PB20	GPIO 52	PWM - PWM[1]	PM - GCLK[1]	EIC - SCAN[5]
2	5	PB21	GPIO 53	PWM - PWM[2]	PM - GCLK[2]	EIC - SCAN[6]
3	6	PB22	GPIO 54	PWM - PWM[3]	PM - GCLK[3]	EIC - SCAN[7]
6	9	PB23	GPIO 55	TC - A0	USART1 - DCD	
7	11	PB24	GPIO 56	TC - B0	USART1 - DSR	
8	13	PB25	GPIO 57	TC - A1	USART1 - DTR	
9	14	PB26	GPIO 58	TC - B1	USART1 - RI	
10	15	PB27	GPIO 59	TC - A2	PWM - PWM[4]	
14	19	PB28	GPIO 60	TC - B2	PWM - PWM[5]	
15	20	PB29	GPIO 61	USART2 - RXD	PM - GCLK[1]	EBI - NCS[2]
16	21	PB30	GPIO 62	USART2 - TXD	PM - GCLK[2]	EBI - SDCS
17	22	PB31	GPIO 63	USART2 - CLK	PM - GCLK[3]	EBI - NWAIT
63	85	PC00	GPIO 64			
64	86	PC01	GPIO 65			
85	124	PC02	GPIO 66			

Table 9-8. GPIO Controller Function Multiplexing

86	125	PC03	GPIO 67			
93	132	PC04	GPIO 68			
94	133	PC05	GPIO 69			
	1	PX00	GPIO 100	EBI - DATA[10]		
	2	PX01	GPIO 99	EBI - DATA[9]		
	4	PX02	GPIO 98	EBI - DATA[8]		
	10	PX03	GPIO 97	EBI - DATA[7]		
	12	PX04	GPIO 96	EBI - DATA[6]		
	24	PX05	GPIO 95	EBI - DATA[5]		
	26	PX06	GPIO 94	EBI - DATA[4]		
	31	PX07	GPIO 93	EBI - DATA[3]		
	33	PX08	GPIO 92	EBI - DATA[2]		
	35	PX09	GPIO 91	EBI - DATA[1]		
	38	PX10	GPIO 90	EBI - DATA[0]		
	40	PX11	GPIO 109	EBI - NWE1		
	42	PX12	GPIO 108	EBI - NWE0		
	44	PX13	GPIO 107	EBI - NRD		
	46	PX14	GPIO 106	EBI - NCS[1]		
	59	PX15	GPIO 89	EBI - ADDR[19]		
	61	PX16	GPIO 88	EBI - ADDR[18]		
	63	PX17	GPIO 87	EBI - ADDR[17]		
	65	PX18	GPIO 86	EBI - ADDR[16]		
	67	PX19	GPIO 85	EBI - ADDR[15]		
	87	PX20	GPIO 84	EBI - ADDR[14]		
	89	PX21	GPIO 83	EBI - ADDR[13]		
	91	PX22	GPIO 82	EBI - ADDR[12]		
	95	PX23	GPIO 81	EBI - ADDR[11]		
	97	PX24	GPIO 80	EBI - ADDR[10]		
	99	PX25	GPIO 79	EBI - ADDR[9]		
	101	PX26	GPIO 78	EBI - ADDR[8]		
	103	PX27	GPIO 77	EBI - ADDR[7]		
	105	PX28	GPIO 76	EBI - ADDR[6]		
	107	PX29	GPIO 75	EBI - ADDR[5]		
	110	PX30	GPIO 74	EBI - ADDR[4]		
	112	PX31	GPIO 73	EBI - ADDR[3]		
	114	PX32	GPIO 72	EBI - ADDR[2]		
	118	PX33	GPIO 71	EBI - ADDR[1]		
	120	PX34	GPIO 70	EBI - ADDR[0]		
	135	PX35	GPIO 105	EBI - DATA[15]		

Table 9-8. GPIO Controller Function Multiplexing

	137	PX36	GPIO 104	EBI - DATA[14]		
	140	PX37	GPIO 103	EBI - DATA[13]		
	142	PX38	GPIO 102	EBI - DATA[12]		
	144	PX39	GPIO 101	EBI - DATA[11]		

9.7 Oscillator Pinout

The oscillators are not mapped to the normal A,B or C functions and their muxings are controlled by registers in the Power Manager (PM). Please refer to the power manager chapter for more information about this.

Table 9-9. Oscillator pinout

TQFP100 pin	VQFP144 pin	Pad	Oscillator pin
85	124	PC02	xin0
93	132	PC04	xin1
63	85	PC00	xin32
86	125	PC03	xout0
94	133	PC05	xout1
64	86	PC01	xout32

9.8 Peripheral overview

9.8.1 External Bus Interface

- **Optimized for Application Memory Space support**
- **Integrates Two External Memory Controllers:**
  - **Static Memory Controller**
  - **SDRAM Controller**
- **Optimized External Bus:**
  - **16-bit Data Bus**
  - **24-bit Address Bus, Up to 16-Mbytes Addressable**
  - **Optimized pin multiplexing to reduce latencies on External Memories**
- **4 SRAM Chip Selects, 1SDRAM Chip Select:**
  - **Static Memory Controller on NCS0**
  - **SDRAM Controller or Static Memory Controller on NCS1**
  - **Static Memory Controller on NCS2**
  - **Static Memory Controller on NCS3**

9.8.2 Static Memory Controller

- 5 Chip Selects Available
- 64-Mbyte Address Space per Chip Select
- 8-, 16-bit Data Bus
- Word, Halfword, Byte Transfers
- Byte Write or Byte Select Lines
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- Compliant with LCD Module
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes

9.8.3 SDRAM Controller

- Numerous Configurations Supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with Two or Four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming Facilities
  - Word, Half-word, Byte Access
  - Automatic Page Break When Memory Boundary Has Been Reached
  - Multibank Ping-pong Access
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
  - Supports Mobile SDRAM Devices
- Error Detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by Software
- CAS Latency of 1, 2, 3 Supported
- Auto Precharge Command Not Used

9.8.4 USB Controller

- USB 2.0 Compliant, Full-/Low-Speed (FS/LS) and On-The-Go (OTG), 12 Mbit/s
- 7 Pipes/Endpoints
- 960 bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 2 Memory Banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint Configuration and Management with Dedicated DMA Channels
- On-Chip Transceivers Including Pull-Ups

9.8.5 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors

- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

9.8.6 Two-wire Interface

- High speed up to 400kbit/s
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

9.8.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

9.8.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

9.8.9 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement

  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

9.8.10 Pulse Width Modulation Controller

- 7 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

9.8.11 Ethernet 10/100 MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data

10. Boot Sequence

This chapter summarizes the boot sequence of the AT32UC3A. The behaviour after power-up is controlled by the Power Manager. For specific details, refer to Section 13. ”Power Manager (PM)” on page 47.

10.1 Starting of clocks

After power-up, the device will be held in a reset state by the Power-On Reset circuitry, until the power has stabilized throughout the device. Once the power has stabilized, the device will use the internal RC Oscillator as clock source.

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system recieves a clock with the same frequency as the internal RC Oscillator.

10.2 Fetching of initial instructions

After reset has been released, the AVR32 UC CPU starts fetching instructions from the reset address, which is 0x8000_0000. This address points to the first address in the internal Flash.

The code read from the internal Flash is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-60°C to +150°C
Voltage on any Pin except RESET_N with respect to Ground	-TBDV to V_{CC}+TBDV
Voltage on RESET_N with respect to Ground	-TBDV to +TBDV
Maximum Operating Voltage (VDDCORE, VDDSYS)	1.95V
Maximum Operating Voltage (VDDIO)	3.6V
DC Current per I/O Pin	TBD mA
DC Current V_{CC} and GND Pins	TBD mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{VDDCORE}$	DC Supply Core			1.65		1.95
V_{VDDBU}	DC Supply Backup			1.65		1.95
V_{VDDOSC}	DC Supply Oscillator			1.65		1.95
V_{VDDPLL}	DC Supply PLL			1.65		1.95
V_{VDDUSB}	DC Supply USB			1.65		1.95
V_{VDDIO}	DC Supply Peripheral I/Os			3.0		3.6
V_{REF}	Analog reference voltage			2.6		3.6
V_{IL}	Input Low-level Voltage			-0.3		+0.8
V_{IH}	Input High-level Voltage			2.0		V_{VDDIO}+0.3
V_{OL}	Output Low-level Voltage					0.4
V_{OH}	Output High-level Voltage	V_{VDDIO}= V_{VDDIOM} or V_{VDDIOP}		V_{VDDIO}-0.4		
I_{LEAK}	Input Leakage Current	Pullup resistors disabled				TBD
C_{IN}	Input Capacitance	TQFP100 Package				TBD
R_{PULLUP}	Pull-up Resistance				TBD	
I_O	Output Current					TBD
I_{SC}	Static Current	On $V_{VDDCORE}$ = 1.8V, CPU = 0 Hz, CPU is in static mode	T_A =25°C		TBD	
		All inputs driven; RESET_N=1, CPU is in static mode	T_A =85°C			TBD

11.3 Power Consumption

The values in Table 11-1 and Table 11-2 on page 35 are measured values of power consumption with operating conditions as follows:

- V_{DDIO} = 3.3V
- V_{DDCORE} = V_{DDSYS} = 1.8V
- T_A = 25°C
- I/Os are inactive

These figures represent the power consumption measured on the power supplies.

Table 11-1. Power Consumption for Different Modes[1]

Mode	Conditions	Consumption	Unit
Active	Core/HSB clock is 66 MHz. PBA clock is 30 MHz. PBB clock is 66 MHz. All peripheral clocks activated. Measured while the processor is executing a recursive Fibonacci algorithm.	40	mA

Table 11-2. Power Consumption by Peripheral in Active Mode

Peripheral	Consumption	Unit
GPIO	TBD	mA
USART	TBD	
USBB	TBD	
MACB	TBD	
SMC	TBD	
SDRAMC	TBD	
ADC	TBD	
TWI	TBD	
PWM	TBD	
SPI	TBD	
SSC	TBD	
Timer Counter Channels	TBD	

11.4 Clock Characteristics

These parameters are given in the following conditions:

- V_{DDCORE} = 1.8V
- Ambient Temperature = 25°C

11.4.1 CPU/HSB Clock Characteristics

Table 11-3. Core Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPCPU})$	CPU Clock Frequency			66	MHz
t_{CPCPU}	CPU Clock Period		15,15		ns

11.4.2 PBA Clock Characteristics

Table 11-4. PBA Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPPBA})$	PBA Clock Frequency			33	MHz
t_{CPPBA}	PBA Clock Period		30,30		ns

11.4.3 PBB Clock Characteristics

Table 11-5. PBB Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPPBB})$	PBB Clock Frequency			66	MHz
t_{CPPBB}	PBB Clock Period		15,15		ns

11.4.4 XIN Clock Characteristics

Table 11-6. XIN Clock Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPXIN})$	XIN Clock Frequency		3	24	MHz
t_{CPXIN}	XIN Clock Period		20.0		ns
t_{CHXIN}	XIN Clock High Half-period		0.4 x t_{CPXIN}	0.6 x t_{CPXIN}	
t_{CLXIN}	XIN Clock Low Half-period		0.4 x t_{CPXIN}	0.6 x t_{CPXIN}	
C_{IN}	XIN Input Capacitance	(1)		TBD	pF
R_{IN}	XIN Pulldown Resistor	(1)		TBD	kΩ

Note: 1. These characteristics apply only when the Main Oscillator is in bypass mode (i.e., when MOSCEN = 0 and OSCBYPASS = 1 in the CKGR_MOR register.)

11.5 Crystal Oscillator Characteristis

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C and worst case of power supply, unless otherwise specified.

11.5.1 32 KHz Oscillator Characteristics

Table 11-7. 32 KHz Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CP32KHz})$	Crystal Oscillator Frequency			32 768		Hz
	Duty Cycle		TBD		TBD	%
t_{ST}	Startup Time	R_S = TBD kΩ, C_L = TBD pF(1)			TBD	ms

Note: 1. R_S is the equivalent series resistance, C_L is the equivalent load capacitance.

11.5.2 Main Oscillators Characteristics

Table 11-8. Main Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency		0.45		16	MHz
C_{L1}, C_{L2}	Internal Load Capacitance (C_{L1} = C_{L2})			TBD		pF
C_L	Equivalent Load Capacitance			TBD		pF
	Duty Cycle		TBD	TBD	TBD	%
t_{ST}	Startup Time				TBD	ms
I_{OSC}	Current Consumption	Active mode @TBD MHz			TBD	µA
		Standby mode @TBD V			TBD	µA

Notes: 1. C_S is the shunt capacitance

11.5.3 PLL Characteristics

Table 11-9. Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		80		240	MHz
F_{IN}	Input Frequency		TBD		TBD	MHz
I_{PLL}	Current Consumption	active mode			TBD	mA
		standby mode			TBD	µA

Note: 1. Startup time depends on PLL RC filter. A calculation tool is provided by Atmel.

11.6 USB Transceiver Characteristics

11.6.1 Electrical Characteristics

Table 11-10. Electrical Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Levels						
V_{IL}	Low Level				TBD	V
V_{IH}	High Level		TBD			V
V_{DI}	Differential Input Sensivity	|(D+) - (D-)|	TBD			V
V_{CM}	Differential Input Common Mode Range		TBD		TBD	V
C_{IN}	Transceiver capacitance	Capacitance to ground on each line			TBD	pF
I	Hi-Z State Data Line Leakage	$0V < V_{IN} < 3.3V$	TBD		TBD	µA
R_{EXT}	Recommended External USB Series Resistor	In series with each USB pin with ±5%		TBD		Ω
Output Levels						
V_{OL}	Low Level Output	Measured with R_L of 1.425 kΩ tied to 3.6V	TBD		TBD	V
V_{OH}	High Level Output	Measured with R_L of 14.25 kΩ tied to GND	TBD		TBD	V
V_{CRS}	Output Signal Crossover Voltage	Measure conditions described in Figure 11-1	TBD		TBD	V

11.6.2 Switching Characteristics

Table 11-11. In Low Speed

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 400 pF	TBD		TBD	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 400 pF	TBD		TBD	ns
t_{FRFM}	Rise/Fall time Matching	C_{LOAD} = 400 pF	TBD		TBD	%

Table 11-12. In Full Speed

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 50 pF	TBD		TBD	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 50 pF	TBD		TBD	ns
t_{FRFM}	Rise/Fall time Matching		TBD		TBD	%

Figure 11-1. USB Data Signal Rise and Fall Times

11.7 AC Characteristics - TBD

11.8 EBI Timings - TBD

12. Mechanical Characteristics

12.1 Thermal Considerations

12.1.1 Thermal Data

Table 12-1 summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	TBD	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	TBD	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	LQFP144	TBD	°C/W
θ_{JC}	Junction-to-case thermal resistance		LQFP144	TBD	

12.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

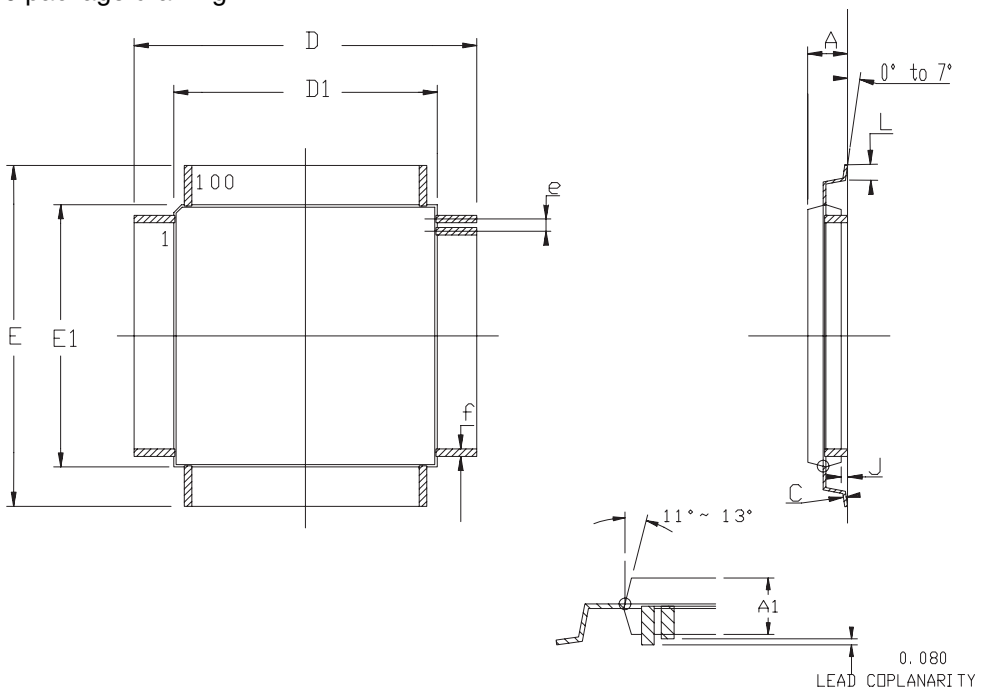
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 12-1 on page 41.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 12-1 on page 41.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section "Power Consumption" on page 34.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

12.2 Package Drawings

Figure 12-1. TQFP-100 package drawing



	MM		INCH	
	Min	Max	Min	Max
A	----	1.20	----	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	16.00 BSC		.630 BSC	
D1	14.00 BSC		.551 BSC	
E	16.00 BSC		.630 BSC	
E1	14.00 BSC		.551 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.020 BSC	
f	0.17	0.27	.007	.011

Table 12-2. Device and Package Maximum Weight

TBD	mg

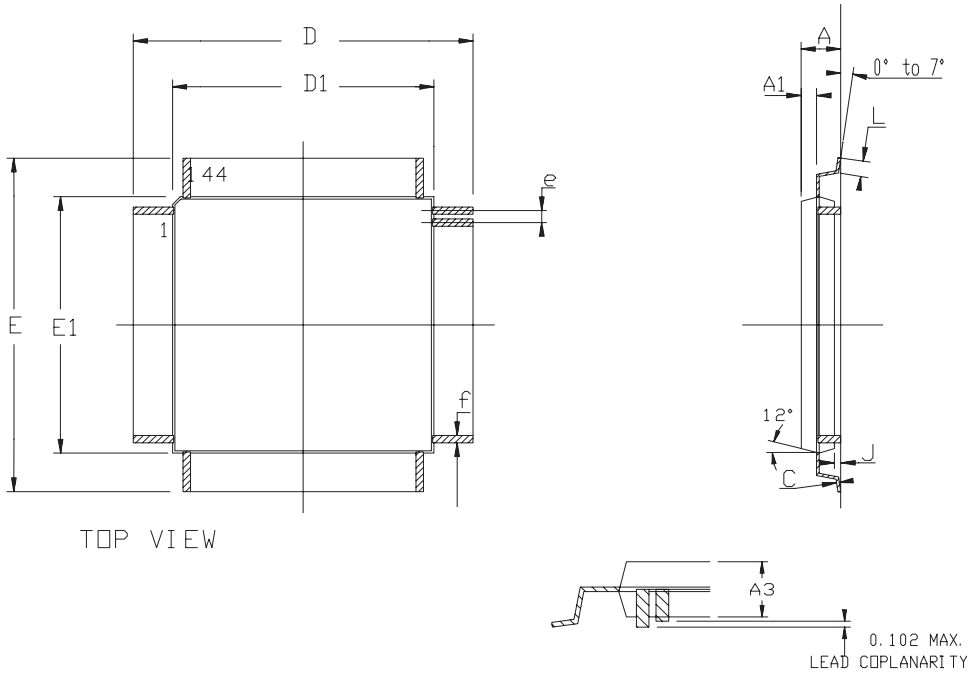
Table 12-3. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 12-2. LQFP-144 package drawing



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
C	0.09	0.20	.004	.008
A3	1.35	1.45	.053	.057
D	21.90	22.10	.862	.870
D1	19.90	20.10	.783	.791
E	21.90	22.10	.862	.870
E1	19.90	20.10	.783	.791
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.22 BSC		.009 BSC	

Table 12-5. Device and Package Maximum Weight

TBD	mg

Table 12-6. Package Characteristics

Moisture Sensitivity Level	TBD

Table 12-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.3 Soldering Profile

Table 12-8 gives the recommended soldering profile from J-STD-20.

Table 12-8. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	TBD
Preheat Temperature 175°C ±25°C	TBD
Temperature Maintained Above 217°C	TBD
Time within 5°C of Actual Peak Temperature	TBD
Peak Temperature Range	TBD
Ramp-down Rate	TBD
Time 25°C to Peak Temperature	TBD

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.

13. Ordering Information

Device	Ordering Code	Package	Conditioning	Temperature Operating Range
AT32UC3A0512	AT32UC3A0512-ALUT	144 lead LQFP	Tray	Industrial (-40°C to 85°C)
AT32UC3A1512	AT32UC3A1512-AUT	100 lead TQFP	Tray	Industrial (-40°C to 85°C)
AT32UC3A0256	AT32UC3A0256-ALUT	144 lead LQFP	Tray	Industrial (-40°C to 85°C)
AT32UC3A1256	AT32UC3A1256-AUT	100 lead TQFP	Tray	Industrial (-40°C to 85°C)
AT32UC3A0128	AT32UC3A0128-ALUT	100 lead TQFP	Tray	Industrial (-40°C to 85°C)
AT32UC3A1128	AT32UC3A1128-AUT	100 lead TQFP	Tray	Industrial (-40°C to 85°C)

14. Errata

14.1 Rev. E

1. **SPI FDIV option does not work**
   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround
   Do not set FDIV = 1.

2. **PWM counter restarts at 0x0001**
   The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

   Fix/Workaround
   - The first period is 0x0000, 0x0001, ..., period

   - Consecutive periods are 0x0001, 0x0002, ..., period

3. **PWM channel interrupt enabling triggers an interrupt**
   When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

   Fix/Workaround
   When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

4. **PWM update period to a 0 value does not work**
   It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

   Fix/Workaround
   Do not update the PWM_CUPD register with a value equal to 0.

5. **PWM channel status may be wrong if disabled before a period has elapsed**
   Before a PWM period has elapsed, the read channel status may be wrong. The CHIDx-bit for a PWM channel in the PWM Enable Register will read '1' for one full PWM period even if the channel was disabled before the period elapsed. It will then read '0' as expected.

   Fix/Workaround

Reading the PWM channel status of a disabled channel is only correct after a PWM period has elapsed.

6. **SSC does not trigger RF when data is low**

   The SSC cannot transmit or receive data when CKS = CKDIV and CKO = none, in TCMR or RCMR respectively.

   Fix/Workaround

   Set CKO to a value that is not "none" and bypass the output of the TK/RK pin with the PIO.

7. **SSC Data is not sent unless clock is set as output**

   The SSC cannot transmit or receive data when CKS = CKDIV and CKO = none, in TCMR or RCMR respectively.

   Fix/Workaround

   Set CKO to a value that is not "none" and bypass the output of the TK/RK pin with the PIO.

8. **USB No end of host reset signaled upon disconnection**

   In host mode, in case of an unexpected device disconnection whereas a usb reset is being sent by the usb controller, the UHCON.RESET bit may not been cleared by the hardware at the end of the reset.

   Fix/Workaround

   A software workaround consists in testing (by polling or interrupt) the disconnection (UHINT.DDISCI == 1) while waiting for the end of reset (UHCON.RESET == 0) to avoid being stuck.

9. **Incorrect Processor ID**

   The processor ID reads 0x01 and not 0x02 as it should.

   Fix/Workaround

   None.

10. **Bus error should be masked in Debug mode**

    If a bus error occurs during debug mode, the processor will not respond to debug commands through the DINST register.

    Fix/Workaround

    A reset of the device will make the CPU respond to debug commands again.

11. **Code execution from external SDRAM does not work**

    Code execution from SDRAM does not work.

    Fix/Workaround

    Do not run code from SDRAM.

12. **Read Modify Write (RMW) instructions on data outside the internal RAM does not work.**

    Read Modify Write (RMW) instructions on data outside the internal RAM does not work.

    Fix/Workaround

    Do not perform RMW instructions on data outside the internal RAM.

13. USART Manchester Encoder Not Working

Manchester encoding/decoding is not working.

Fix/Workaround

Do not use manchester encoding.

14. USART RXBREAK problem when no timeguard

In asynchronous mode the RXBREAK flag is not correctly handled when the timeguard is 0 and the break character is located just after the stop bit.

Fix/Workaround

If the NBSTOP is 1, timeguard should be different from 0.

15 USART Handshaking: 2 characters sent / CTS rises when TX

If CTS switches from 0 to 1 during the TX of a character, if the Holding register is not empty, the TXHOLDING is also transmitted.

Fix/Workaround

None.

16. USART PDC and TIMEGUARD not supported in MANCHESTER

Manchester encoding/decoding is not working.

Fix/Workaround

Do not use manchester encoding.

17. Voltage regulator input and output is connected to VDDIO and VDDCORE inside the device

The voltage regulator input and output is connected to VDDIO and VDDCORE respectively inside the device.

Fix/Workaround

Do not supply VDDCORE externally, as this supply will work in paralell with the regulator.

18. ADC possible miss on DRDY when disabling a channel

The ADC does not work properly when more than one channel is enabled.

Fix/Workaround

Do not use the ADC with more than one channel enabled at a time.

19. ADC OVRE flag sometimes not reset on Status Register read

The OVRE flag does not clear properly if read simultaneously to an end of conversion.

Fix/Workaround

None.

20. CRC calculation of a locked device will calculate CRC for 512 kB of flash memory, even though the part has less flash.

Fix/Workaround

The flash address space is wrapping, so it is possible to use the CRC value by calculating CRC of the flash content concatenated with itself N times. Where N is 512 kB/flash size.

21. SDRAM SDCKE rise at the same time as SDCK while exiting self-refresh mode

SDCKE rise at the same time as SDCK while exiting self-refresh mode.

Fix/Workaround

None.

22. PCx pins go low in stop mode

In sleep mode stop all PCx pins will be controlled by GPIO module instead of oscillators. This can cause drive contention on the XINx in worst case.

Fix/Workaround

Before entering stop mode set all PCx pins to input and GPIO controlled.

23. Need two NOPs instruction after instructions masking interrupts

The instructions following in the pipeline the instruction masking the interrupt through SR may behave abnormally.

Fix/Workaround

Place two NOPs instructions after each SSRF or MTSR instruction setting IxM or GM in SR.

15. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

15.1 Rev. A 03/07

1. Initial revision.

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