FAN8621B

12V Spindle Motor and Voice Coil Motor Driver IC

Features

General

- Hysteresis power on reset with delay function
- 5V, 12V supplies monitoring
- Thermal shut down(TSD)
- Programmable precision regulator usging minimal external component
- Three state control input to reduce number of PINs

Spindle Motor(SPM)

- ASIC based start-up
- Internal back-EMF processing
- Internal sensorless commutation
- Internal SPM speed control with SFLL(Syncronized Frequency Lock Loop).
- Linear SPM current control
- Selectable Motor Speed (5400/7200 RPM)
- Soft commutation circuitry to reduce acoustic noise
- Adjustable brake delay time
- Maximum 2A start-up current capability
- Internal and external spindle brake
- Speed lock indicator output

Voice Coil Motor (VCM)

- Intelligent retract (decreased bouncing)
- 1.2A internal VCM power driver
- Selectable transconductance
- 4V precision reference output
- Two PWM input (fine/coarse) for VCM set point

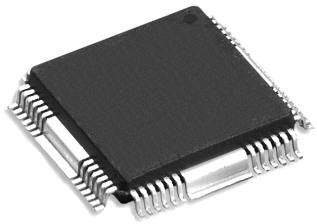
Typical Applications

- Hard disk drive(HDD)

Description

The FAN8621B, is a Bipolar monolithic stand-alone IC, designed for 12V HDD applications.The internal power stage consists of vertical PNP and NPN TRs for both SPM and VCM, thus minimizing voltage drop, and increasing drive capability up to 2A for SPM and 1.2A for VCM. This device includes soft commutation drive to reduce audible noise and intelligent retract function for decreased bouncing.

48-QFPH-1414

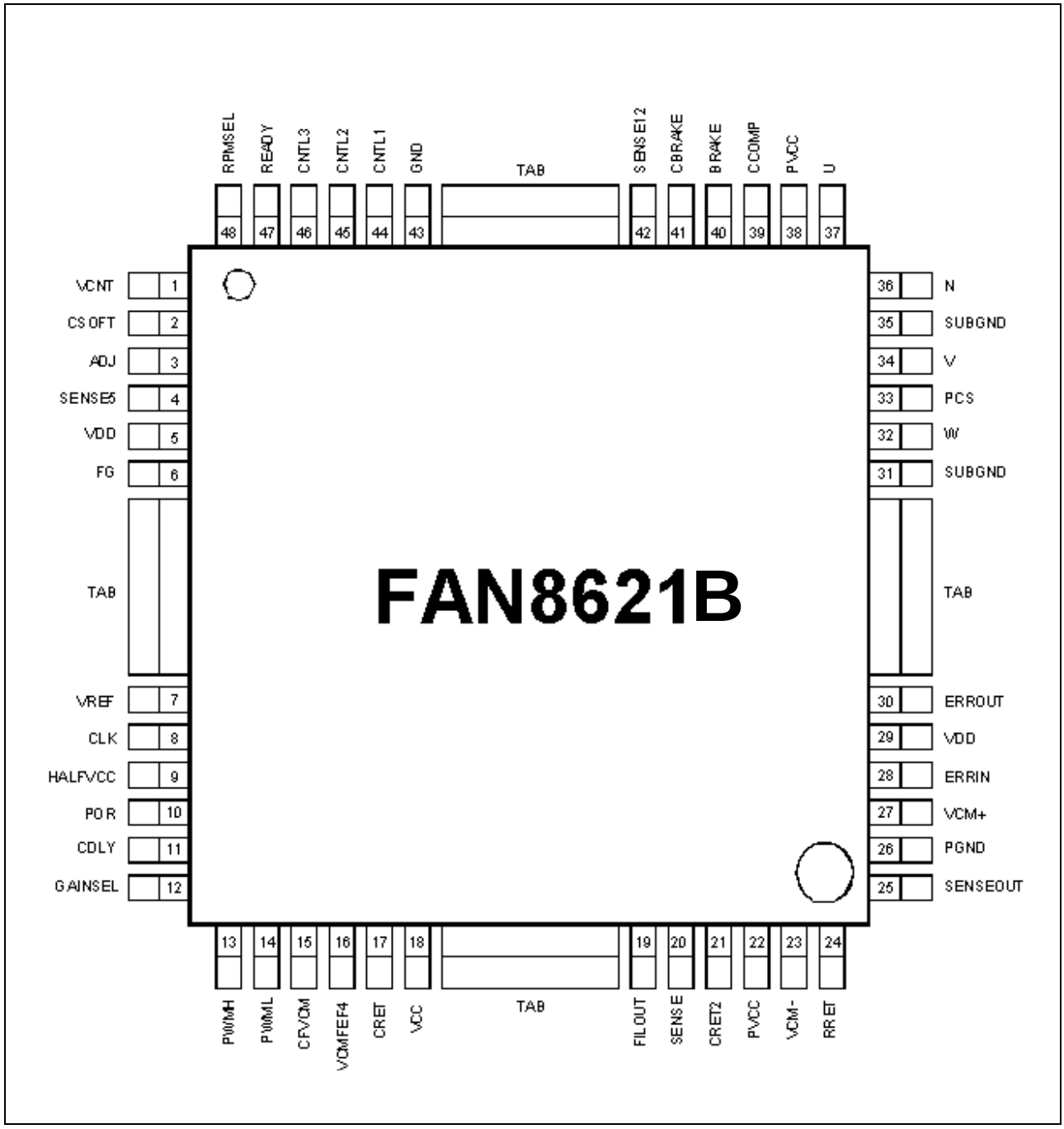


Ordering Information

Device	Package	Operating Temp.
FAN8621B	48-QFPH-1414	0 ~ 70°C

Rev. 1.0.0
May. 2000.

Pin Assignments



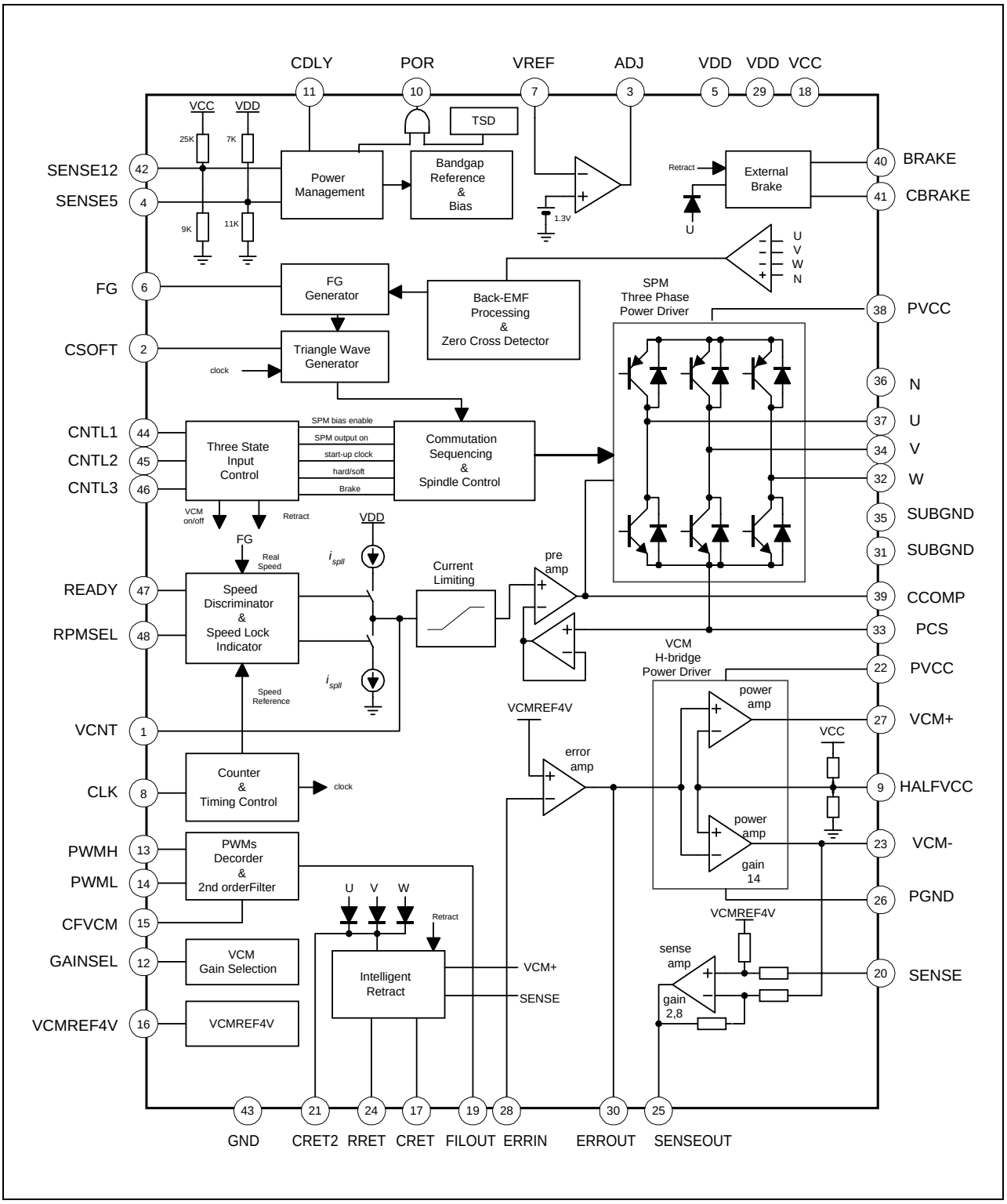
Pin Definitions

Pin Number	Pin Name	IO	Pin Function Description
1	VCNT	A	Speed controller output. Range 3.8V to 0.5V
2	CSOFT	A	Capacitor for soft commutation
3	ADJ	A	Adjust external regulator voltage (VREF)
4	SENSE5	A	5V power line sensing
5	VDD	P	5V power line
6	FG	O	Frequency generation for spindle rotation speed. Typically 1.08KHz (5400RPM)
7	VREF	P	Regulator voltage output. This voltage is controlled by pin 3 voltage
8	CLK	I	System clock. Digital clock input as a time reference
9	HALFVCC	P	1/2 VCC
10	POR	O	Power on reset. H : normal, L: power fail
11	CDLY	A	Define POR delay time
12	GAINSEL	I	Sense amplifier gain selection. H : High gain (8), L : Low gain (2)
13	PWMH	I	Coarse PWM input for VCM set point
14	PWML	I	Fine PWM input for VCM set point
15	CFVCM	A	Output of PWM inputs to voltage converter
16	VCMREF4V	P	4V reference output for VCM
17	CRET	A	Define retract delay time.
18	VCC	P	12V power line
19	FILOUT	A	Filtered output of PWM inputs. This voltage define VCM set point
20	SENSE	A	Non-inverting input of differential amplifier for VCM current sensing
21	CRET2	A	Power for retract when power down
22	PVCC	P	12V power line for VCM
23	VCM-	A	Negative output terminal of VCM power amplifier
24	RRET	A	Adjust maximum retract current
25	SENSEOUT	A	Output of differential amplifier for VCM current sensing
26	PGND	P	Ground for VCM
27	VCM+	A	positive output terminal of VCM power amplifier
28	ERRIN	A	Inverting input of VCM error amplifier
29	VDD	P	5V power line
30	ERROUT	A	Output of VCM error amplifier
31	SUBGND	P	Ground for spindle motor
32	W	A	Spindle W phase output

Pin Definitions (Continued)

Pin Number	Pin Name	IO	Pin Function Description
33	PCS	A	Spindle current sensing.
34	V	A	Spindle V phase output
35	SUBGND	P	Ground for spindle
36	N	A	Spindle N phase output
37	U	A	Spindle U phase output
38	PVCC	P	12V power line for spindle
39	CCOMP	A	Current controller output. This Voltage define spindle output current
40	BRAKE	A	Gating signal for external brake
41	CBRAKE	A	Charged back-EMF to supply brake power when power down
42	SENSE12	A	12V power line sensing
43	GND	P	Ground
44	CNTL1	I	Control input for spindle . H: spindle enable, Z: Spindle bias enable, L: brake
45	CNTL2	I	Start-up clock and soft commutation. H: Start-up clock , L : soft commutation.
46	CNTL3	I	Control input for VCM. H: VCM enable, Z : VCM disable, L: retract
47	READY	O	Speed lock indicator when speed is within 0.7% speed error range. H : speed locked, L: unlocked
48	RPMSEL	I	Target spindle speed selection. L : 5400 rpm, H: 7200 rpm with 5MHz Clock

Internal Block Diagram



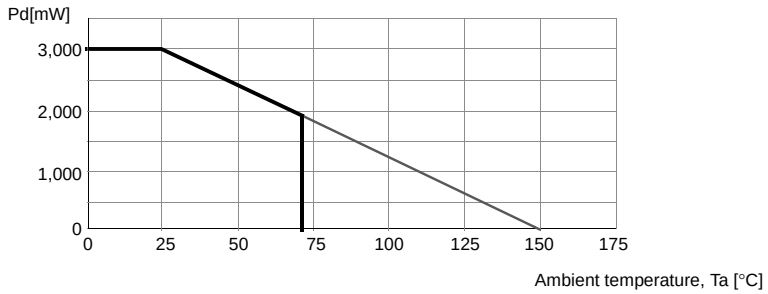
Absolute Maximum Ratings(Ta = 25°C)

Parameter	Symbol	Value	Unit
Supply voltage (signal)	V_{DD}	6.0	V
Supply voltage (signal)	V_{CC}	15.0	V
Supply voltage (power)	PV_{CC}	15.0	V
Storage Temperature	T_{STG}	–55 ~ 125	°C
Power dissipation	P_D	3.0 note	W
Maximum Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_{AMB}	0 ~ 70	°C

NOTE:

1. When mounted on 50mm × 50mm × 1mm PCB (Phenolic resin material)
2. Power dissipation is reduced 16mV / °C for using above Ta=25°C.
3. Do not exceed Pd and SOA(Safe Operation Area).

Power Dissipation Curve



Recommanded Operating Coditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (signal)	V_{DD}	4.5	5.0	5.5	V
Supply voltage (signal)	Vcc	10.8	12.0	13.2	V
Supply voltage (power)	PV_{CC}	10.8	12.0	13.2	V

Electrical Characteristics

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
SUPPLY CURRENT						
VDD Line supply current1	I_{DD1}	CNTL1=L,CNTL2=CNTL3=Z (brake)	80-	100	120	mA
VDD Line supply current2	I_{DD2}	CNTL1= CNTL2 =CNTL3=Z (SPM bias enable)	25	35	45	mA
VDD Line supply current3	I_{DD3}	CNTL1=CNTL3=H,CNTL2=Z (SPM,VCM enable)	25	35	45	mA
VDD Line supply current4	I_{DD4}	CNTL1=CNTL2=Z,CNTL3= L (retract)	25	35	45	mA
VCC Line supply current1	I_{CC1}	CNTL1=L,CNTL2=CNTL3=Z (brake)	2	7	12	mA
VCC Line supply current2	I_{CC2}	CNTL1= CNTL2 =CNTL3=Z (SPM bias enable)	4	9	15	mA
VCC Line supply current3	I_{CC3}	CNTL1=CNTL3=H,CNTL2=Z (SPM,VCM enable)	10	20	60	mA
VCC Line supply current4	I_{CC4}	CNTL1=CNTL2=Z,CNTL3=L (retract)	12	19	25	mA
SUPPLY MONITOR						
Threshold voltage1 for VCC	V_{TH12A}	V_{CC}=sweep,V_{DD}=5V	9.05	9.40	9.75	V
Threshold voltage2 for VCC	V_{TH12B}	V_{CC}=sweep,V_{DD}=5V	8.75	9.10	9.45	V
Hysteresis on VCCcomparator	V_{HYS12}	V_{CC}=sweep,V_{DD}=5V	0.15	0.3	0.45	V
Threshold voltage1 for VDD	V_{TH5A}	V_{CC}=12V,V_{DD}=sweep	3.45	3.90	4.15	V
Threshold voltage2 for VDD	V_{TH5B}	V_{CC}=12V,V_{DD}=sweep	3.30	3.75	4.00	V
Hysteresis on V comparator	V_{HYS5}	V_{CC}=12V,V_{DD}=sweep	0.08	0.15	0.23	V
POWER ON RESET GENERATOR						
Charging current for POR cap	I_{CPOR}		–18.0	–14	–10	μA
POR threshold voltage	V_{THPOR}		1.1	1.3	1.5	V
Output high voltage	V_{PORH}	V_{CC} = 12V, V_{DD}= 5V, POR output current is 1mA	4.5	-	Vdd	V
Output low voltage	V_{PORL}	V_{CC} = 12V, V_{DD}= 5V, POR output current is 1mA	0	-	0.5	V
CONTROL INPUTs(CNTL1,CNTL2,CNTL3)						
Control input low voltage	V_{CTL}	CNTL1=CNTL2=CNTL3=sweep	0.8	1.3	1.7	V
Control input high voltage	V_{CTH}	CNTL1=CNTL2=CNTL3=sweep	1.85	2.3	2.75	V
Control input low current	I_{CTI}	CNTL1=CNTL2=CNTL3=sweep	-290	-200	-110	μA
Control input high current	I_{CTH}	CNTL1=CNTL2=CNTL3=sweep	55	110	190	μA

Electrical Characteristics (Contnued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SPINDLE MOTOR (SPM)						
FG FREQUENCY GENERATOR						
FG frequency	F_{FG}	CLK=5MHz,RPMSEL=L (5400 RPM)	0.97	1.08	1.18	KHz
FG duty	D_{FG}	F_{FG} = 1.08KHz	45	50	50	%
FG output high voltage	V_{FGH}	FG output current is 1mA	4.5	-	V_{DD}	V
FG output low voltage	V_{FGL}	FG output current is 1mA	-	-	0.5	V
READY SIGNAL GENERATION						
READY high output	V_{RDH}	CNTL1=H,within ±0.7% motor speed error,	4.5	-	V_{DD}	V
READY low output	V_{RDL}	READY output current is 1mA	-	-	0.5	V
SINDLE OUTPUT SATURATION VOLTAGE						
U Saturation voltage upper	V_{SUU}	I_U=1A	0.2	0.6	1.0	V
VSaturation voltage upper	V_{SVU}	I_V=1A	0.2	0.6	1.0	V
W Saturation voltage upper	V_{SWU}	I_W=1A	0.2	0.6	1.0	V
U Saturation voltage lower	V_{SUL}	I_U=1A	0.2	0.4	0.8	V
V Saturation voltage lower	V_{SVL}	I_V=1A	0.2	0.4	0.8	V
W Saturation voltage lower	V_{SWL}	I_W=1A	0.2	0.4	0.8	V
RPMSELECT INPUT						
RPMSEL threshold voltage	V_{RPH}	-	1.1	1.5	1.7	V
RPMSEL input high current	I_{RPHI}	-	60	91	110	µA
RPMSEL input low current	I_{RPLO}	-	-5	0	5	µA
SPEED CONTROLLER						
Speed controller high voltage	V_{CNTH}	-	3.5	3.8	4.2	V
Speed controller low voltage	V_{CNTL}	-	-	-	0.5	V
High voltage of linear range	V_{LIMITH}	-	3.15	3.5	3.85	V
Low voltage of linear range	V_{LIMITL}	-	1.15	1.5	1.85	V
F/I converter charge current	I_{SPLLC}	-	-70	-50	-40	µA
F/I converter discharge current	I_{SPLLD}	-	40	52	70	µA
Transeconductance gain of SPM	GM_{SPM}	R_{PCS}=0.33Ω	0.6	0.8	1.0	-
CURRENT LIMITTER						
Limit voltage of current amp	V_{LIMIT1}	R_{PCS} = 0.33Ω	-	0.57	-	V
Limit voltage of current amp	V_{LIMIT2}	R_{PCS} = 0.33Ω	-	0	-	V
Equivalent output resistance	R_{CC}	-	-	20	-	KΩ
EXTERNAL REGULATOR						
Regulator output voltage	V_{REG}	V_{ADJ}(pin3) = 1.3V	-	3.3	-	V
Regulator line regulation	R_{LINE}	-	-	-	2.0	%
Regulator load regulation	R_{LOAD}	I_O= 500mA	-	-	2.0	%

Electrical Characteristics (Contnued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SPINDLE MOTOR (Continued)						
BRAKE						
Cbrake output voltage	V_{BC}	-	11	11.3	11.8	V
Brake output high voltage	V_{BH}	-	11	–	–	V
Brake output low voltage	V_{BL}	-	-	-	0.5	V
SOFT COMMUTATION						
Soft commutation high voltage	V_{SOFTH}	-	3.1	-	3.7	V
Soft commutation low voltage	V_{SOFTL}	-	1.4	1.7	2.0	V
Discharging current	I_{SOFTC}	-	30	45	60	µA
Charging current	I_{SOFTD}	-	-60	-45	-30	µA
DRIVE OUTPUTS (U,V,W)						
Total voltage Drop	V_{DROPS}	I_{MOTOR} = 1A	-	-	1.8	V
Leakage current	I_{LEAKS}	-	–10	0	10	µA
VOICE COIL MOTOR CIRCUIT(VCM)						
PWM INPUTS						
PWMH/PWML high input voltage	V_{PWMH}	-	2.8	-	-	V
PWMH/PWML low input voltage	V_{PWML}	-	-	-	2.2	V
PWMH charge/discharge current	I_{PWMH}	-	650	670	690	µA
PWML charge/discharge current	I_{PWML}	-	10	10.5	11	µA
PWM current ratio	I_{RATIO}	I_{PWMH}/I_{PWML}	63	64	65	
Internal resister	R_{FVCM}	-	-	3	-	kΩ
VCN PWM FILTER						
Maximum phase shift	D_F	Measure at 500Hz, C_{CFVCM} = 1nF	-	-	–2	deg
Cut-off frequency	F_{CO}	-	-	100	-	KHz
Attenuation at 1MHz	F_{ITER}	-	-	70	-	dB
Filter output voltage1	V_{CVCM1}	PWMH=PWML=0%	5.6	6.00	6.40	V
Filter output voltage2	V_{CVCM2}	PWMH=PWML=50%	3.8	4.0	4.2	V
Filter output voltage3	V_{CVCM3}	PWMH=PWML=100%	1.6	2	2.4	V
VCM REFERENCE						
VCM reference voltage 4V	V_{REF4}	CNTL3 = 5V, VREF4V output current=1mA	3.8	4	4.2	V
VCM reference voltage 1/2 V_{CC}	V_{REF6}	HALFVCC output current =1µA	5.9	6.0	6.1	V

Electrical Characteristics (Contnued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSE AMPLIFIER						
Amp high output voltage	V_{SOH}	-	10.8	-	-	V
Amp low output voltage	V_{SOL}	-	-	-	1.2	V
Input offset voltage	V_{OSS}	-	–15	0	15	mV
Short circuit current	I_{SSC}	-	10	-	-	mA
Unity gain bandwidth	B_{GS}	-	-	2	-	MHz
Voltage gain 1	A_{VS1}	GAINSEL : L	-	18	-	dB
Voltage gain 2	A_{VS2}	GAINSEL : H	-	6	-	dB
ERROR AMPLIFIER						
Amp high output voltage	V_{EOH}	-	10.8	-	-	V
Amp low output voltage	V_{EOL}	-	-	-	1.2	V
Input offset voltage	V_{OSE}	-	–15	0	15	mV
Open loop gain	A_{VE}	-	-	80	-	dB
Unity gain bandwidth	B_{GE}	-	-	2	-	MHz
Short circuit current	I_{SSE}	-	8	-	-	mA
POWER AMPLIFIER						
Output high voltage	V_{POH}	-	11.5	-	-	V
Output low voltage	V_{POL}	-	-	-	0.5	V
Input offset voltage	V_{OSP}	-	–15	0	15	mV
Gain	A_{PO}	-	21.2	22	23.8	dB
Unity gain bandwidth	B_{GP}	-	-	2	-	MHz
Total voltage Drop	V_{DROPV}	when VCM current is 0.7A	-	-	1.5	V
Leakage current	I_{LEAKV}	-	–20	0	20	µA
VCM AMP TOTAL						
VCM offset current	V_{VCMOS}	PWMH=PWML=50% Duty	–20	0	20	mA
VCM transconductance low gain	GM_{VH}	GAINSEL = H,sense resister is 1Ω	0.05	0.12	0.14	A/V
VCM transconductance high gain	GM_{VL}	GAINSEL = L,sense resister is 1Ω	0.35	0.45	0.55	A/V
RETRACT FUNCTION						
Min operating voltage of CRET2	V_{CRET2}	-	2.0	-	-	V
Cret charge current	I_{CRET}	-	-70	-85	-100	µA
Max. retract sink current	I_{RCT}	-	-	125	-	mA
Retract reference voltage	V_{RET}	-	0.75	0.9	1.05	V
Retract current limit resister	R_{IRET}	-	-	3	-	KΩ
Leakage current of output TR	I_{LRET}	-	–10	0	10	µA
Sink saturation voltage	V_{RTSAT}	-	-	0.4	0.7	V
THERMAL SHUT DOWN						
Operating temperature	T_{TSD}	-	135	150	165	°C
Thermal hystereis	T_{HYS}	-	20	30	40	°C

Application Informations

General

The FAN8621B is a stand alone combination chip consisting of Spindle Motor (SPM) and Voice Coil Motor (VCM)circuit for HDD applications. The speed control of SPM is achieved by internal Synchronous Phase Locked Loop (SPLL). The FAN8621B supplies adjustable regulated power with external component and signals READY indicating SPM is locked within some speed range (typically ±0.7% speed error). Current set point is applied by two PWM signals and VCM current is monitored by external sense resistor. VCM circuit generates 4 voltage references for testing. Fig.1 shows overall interfacing of FAN8621B with external and HDD motors

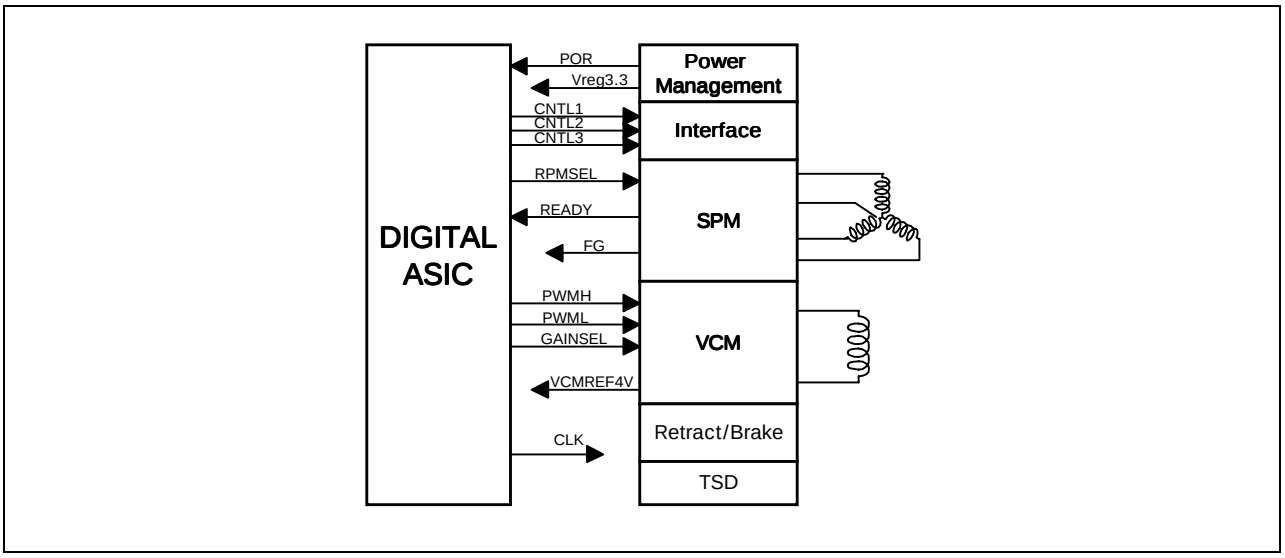


Figure 1. Overall Interfacing of the FAN8621B

The control signals have three status and their function is summarized as follows;

Signals \ Pin Status		H	Z	L
CNTL1	SPM	enable(1)	bias enable	disable
	Brake	disable	disable	enable
CNTL2	Commutation	hard	Hard	soft
	Start Clock	high(2)	low(2)	-
CNTL3	VCM	enable	disable	disable
	Retract	disable	disable	enable
GAINSEL	Start-up hold	normal	normal	hold(3)
	Sense Amp gain	2	2	8

Table 1. Control PIN function

Notes:
1. SPM bias + SPM Output Driver enable
2. Makes SPM Open Loop (Start-up) Commutation Signal
3. Test Only when READY is low

Spindle Motor Driver

The spindle motor driver has two operating modes : hard commutation in start-up and acceleration mode and soft commutation in steady state to reduce acoustic noise.

Start-up and Acceleration

To spin up the motor, open mode start-up clock must be fed to CNTL2 pin in range 20 ~ 200Hz depending on number of platter and motor RPM. This HIGH and OPEN signal commutates motor current in turn while back-EMF comparator checks back-EMF level. When the back-EMF detects motor position, then operating mode is changed from start-up mode to acceleration mode. Also internal commutation logic starts sensorless commutation.

Speed Control

Spindle motor speed is defined by system clock and RPMSEL (pin48) . For your reference, see table2

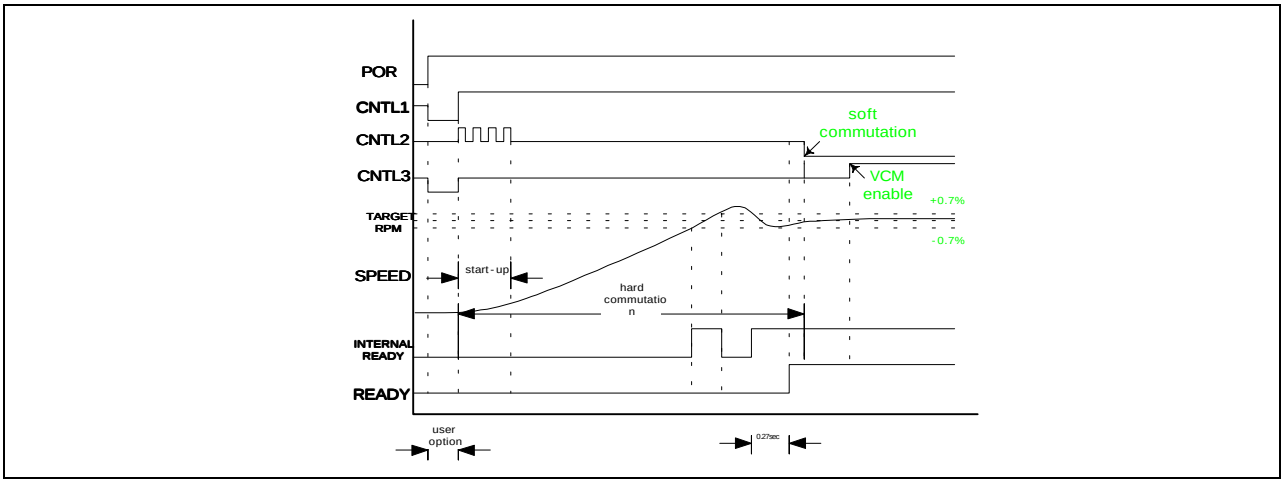


Figure 2. Typical Control Sequence of the FAN8621B

Speed and rotor position of spindle motor is measured by back-EMFs. Back-EMF comparator detects zero crossing point (ZCP) of unexcited phase back-EMF. The output frequency of comparator multiplied by 3 represents motor speed FG (pin6). FG frequency is calculated as follows

FG = motor RPM/60 × pole number/2 × phase number

Pin Value / Speed	System clock (CLK, pin8)	Rpm selection (RPMSEL, pin48)
5400 rpm	5MHz	L
7200 rpm		H
3600rpm	3.333MHz	L
4800rpm		H

Table 2. RPM selection

For example, 8 pole, three phase 5400 rpm motor,

f_{FG} = 5400 / 60 × 8 / 2 × 3 = 1080Hz

The spindle motor speed is controlled by SPLL which consists of Synchronous F/I converter , loop filter , and inner current control loop. F/I converter compares RPM reference time with 12 FG time one rotation of spindle for 8 pole motor. The time difference is converted into charge/discharge current source, and fed to loop filter consisting of external RC network. Loop filter acts ad speed controller and it's output becomes spindle output current set point. If spindle motor speed is greater than target speed, switch s2 is turned on, thus decreasing output voltage of loop filter. Current limiting during start-up is achieved by sensing the voltage across the sense resistor connected PCS (pin 33). This limit the loop filer output. The output of loof filter is compared with internal 2.5V reference. If the difference is over 0.75V, the output is limited and scaled down. When the output of loof filter is 1.75V(2.5V-0.75V), the output of limitter is 0. The maximum output of limitter is 0.4V when the output of loof filter is over 3.25V. So spindle output current is linearly controlled by level shifted current set point driving high side vertical PNP TR of spindle output driver. Overall concept of SPM speed control is shown Figure3.

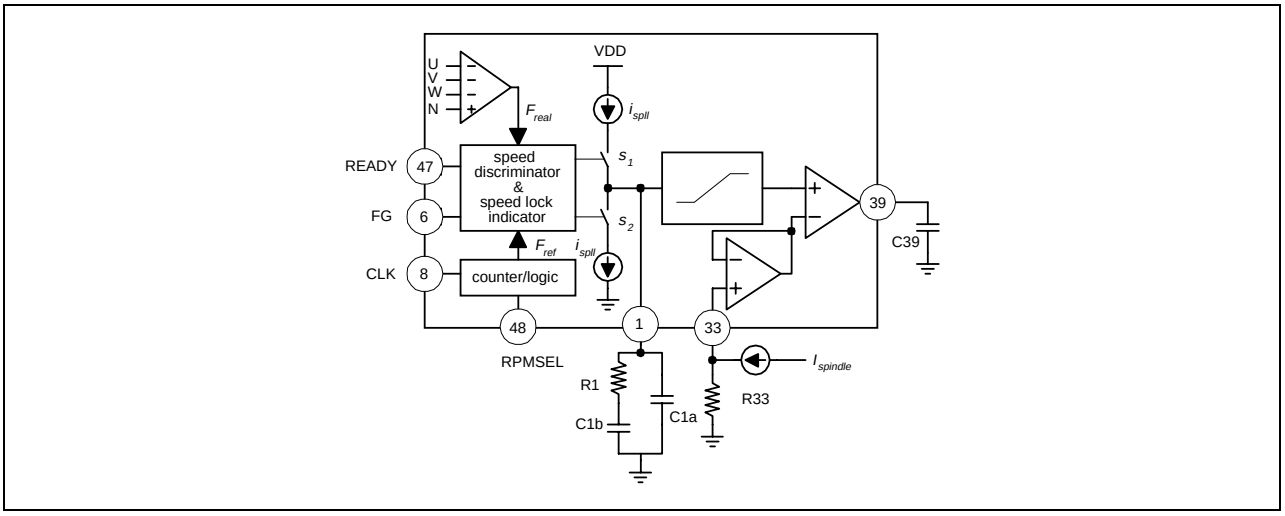


Figure 3. Speed Control of SPM

Indirect Rotor Position Sensing and Commutation

The back-EMF comparator detects the instant at which the back-EMF in the unexcited phase cross as zero. The commutation timing and sequencing for driver outputs is determined by internal commutation logic based on back-EMF ZCP (zero crossing point). Commutation is initiated in advance of ZCP, 30° (electrical) for hard commutation and 1° for soft commutation, respectively. In BLDC motor with trapezoidal type back-EMF, phase current waveforms look like step wave, which generates audible noise. In soft commutation mode (CNTL2 pin45 is LOW), the two phase currents overlap with some current slope. This slope is determined by internal PWM pattern and external capacitor, CSOFT. The soft commutation using current slope of the motor reduce acoustic noise and voltage spark which is generated on the motor coil at the commutation.

Spindle Output Driver

Spindle Output driver contains vertical PNP TR for high side and NPN TR for low side. For one commutation period, PNP TR is controlled linearly by the difference between the current set point VCNT(pin1) and sensed current PCS (pin33), while NPN TR is fully turned on. This scheme provides low voltage drop in linear current control application. The total voltage drop is about 1.8V in 2A current rating. Maximum spindle current is defined as follows;

$$Ispindle(max) = \frac{0.57V}{R33 + Rmetal}$$

Where Rmetal is internal metal resistance(typically 50mΩ). If R33 is 150mΩ, the maximum spindle current is 2A.

Spindle Brake

There are two braking modes; internal and external braking. Spindle is braked when CNTL1 (pin44) is LOW by turning all low side driver on. In case of power failure, brake power is supplied by charged capacitor connected CBRAKE (pin41). Gate signal for two external MOSFET is issued from BRAKE (pin40) with time delay, which is defined by internal resistor (2.8M) and external capacitor.

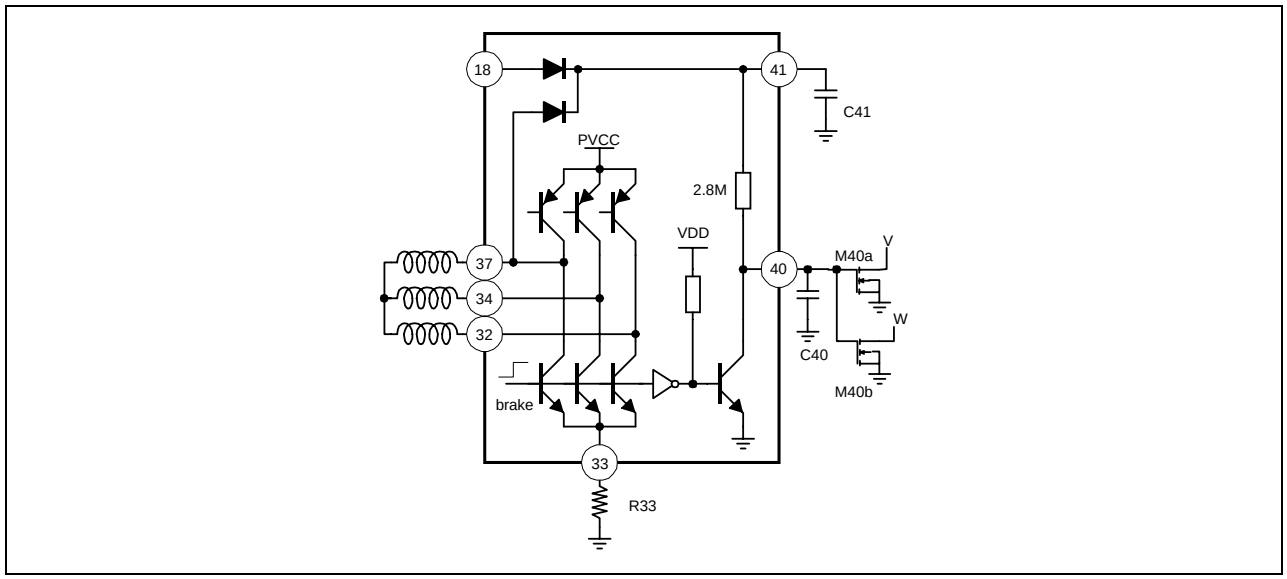


Figure 4. Brake Function Block

Voice Coil Motor Driver

VCM Current Set Point

VCM current set point is defined by two PWM signals. External capacitor connected CFVCM (pin15) is charged and/or discharged depending on status of PWM signals. The voltage, level shifted by 4V, is filtered by an internal 2-nd order filter and converted into DC voltage, FILOUT (pin19) ranging from VCMREF4V+2V to VCMREF4V-2V. The cutoff frequency of the 2nd order filter is about 100KHz, so the PWM frequency must be grater than 100KHz. For more resolution of VCM current set point, the value of two internal current sources for PWMH and PWML is not equal. The weight is 64, so it is good that frequency of PWMH is different that of PWML. When PWM signal is LOW, CFVCM (pin15) voltage increases This voltage is limited by internal 4V reference and resistor, R_{FVCM}.

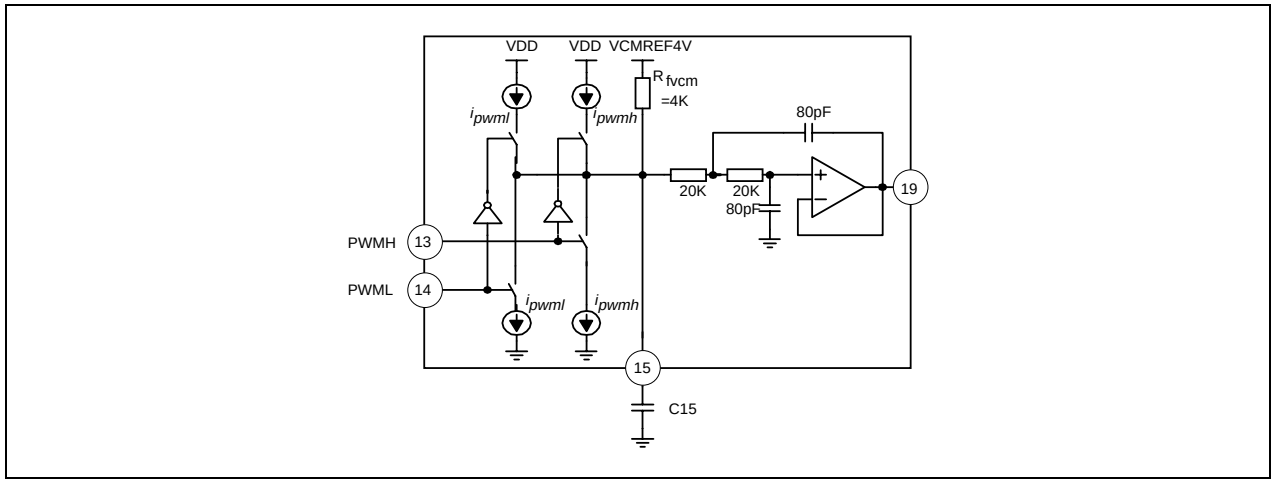


Figure 5. Current Set Point with PWMs

Sense Amplifier

Current sense amplifier amplifies the differential voltage across the sense resistor which is in series with VCM coil. This amplified voltage is level shifted by VCMREF4V. The amplifier gain is set to 2 or 8 depending on GAINSEL. The output of the current sense amplifier is available at SENSEOUT(pin25).

VCM Current Loop Error Amplifier

The inverting input of error amplifier is summing point of VCM current set point (FILOUT) and actual VCM current (SENSEOUT). The output of error amplifier is proportional to the dynamically compensated voltage difference between FILOUT and SENSEOUT. This output voltage is level shifted to VCMREF4V via connecting non-inverting input of error amplifier internally to VCMREF4V. The dynamic compensation is achieved by external RC network connected to ERRIN (pin28) and ERROUT (pin30)

VCM Power Amplifier

The VCM power amplifier is a linear H-bridge type power driver consist of two NPN TR and two vertical PNP TR to reduce voltage drop. Total voltage drop is 1.5V at 0.7A. The differential gain of power amplifier is 14.

If open loop gain of power and error amplifier is very large, the overall DC gain of VCM driver is calculated as follow

$$Gm = \frac{R25}{R19} \cdot \frac{1}{R20 + R_{metal(VCM)}} \cdot \frac{1}{A_{VS}}$$

where R20 is VCM current sense resistor and Avs is gain of sense amplifier. Rmetal(VCM) is internal metal resistance(typically 0.05ohm). If R25 is equal to R19, R20 = 1Ω, and $R_{metal(VCM)} = 0$, then overall DC gain is determined by the gain of sense amplifier. For Example,GAINSEL is low,

$$Gm = \frac{1}{A_{VS}} = \frac{1}{8} = 0.125$$

And if GAINSEL is high, then

$$Gm = \frac{1}{A_{VS}} = \frac{1}{2} = 0.5$$

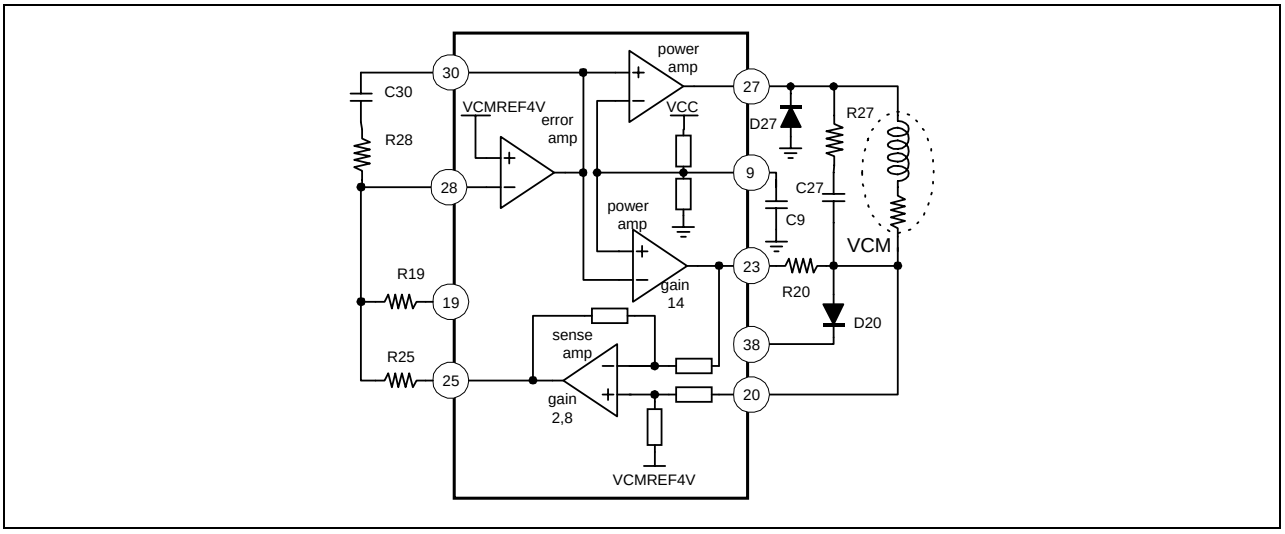


Figure 6. Current Control of VCM

VCM Retract

Power fail condition or when VCM retract command is issued on CNTL3 (pin46) LOW, retract circuit is activated. The retract current is limited by internal and external resistor connected RRET (pin24) and retract delay time is adjusted by external capacitor connected CRET (pin 17). The voltage on CRET2 (pin21) charged by spindle back-EMF serves as retract power.

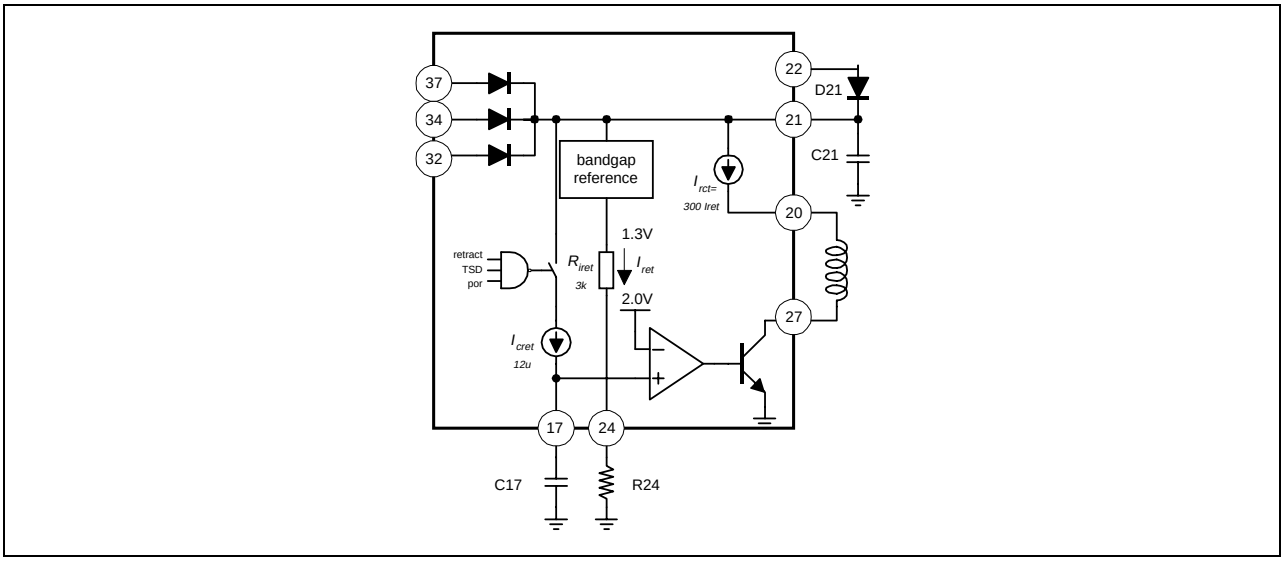


Figure 7. Retract Function Block

Retract delay time and maximum retract current is defined as follows;

$$T_{retdly} = C17 \cdot \frac{1.25}{I_{cret}}$$

$$I_{rct(max)} = 300 \cdot I_{ret} = 300 \cdot \frac{2.0}{3K + R24}$$

Power Management

Supplies Monitoring and Reference

The voltage reference circuit generates precision 1.3V volt reference, other voltage and current reference. Precision low voltage monitor circuitry senses 5V, 12V supplies. These supplies are individually divided down by resistor divider and then compared with internal 2.5V reference to determine the set-point low voltage condition. Low voltage condition can be changed by adding external resistor on SENSE5 (pin4), SENSE12 (42).

Power On Reset (POR)

When low voltage is detected, POR (pin10) is lowered immediately and fed to external controller. The retract and braking sequence is started. If low voltage condition is removed, the POR becomes high with delay. This time delay is based on charging of the CDLY (pin11) capacitor with internal current source.

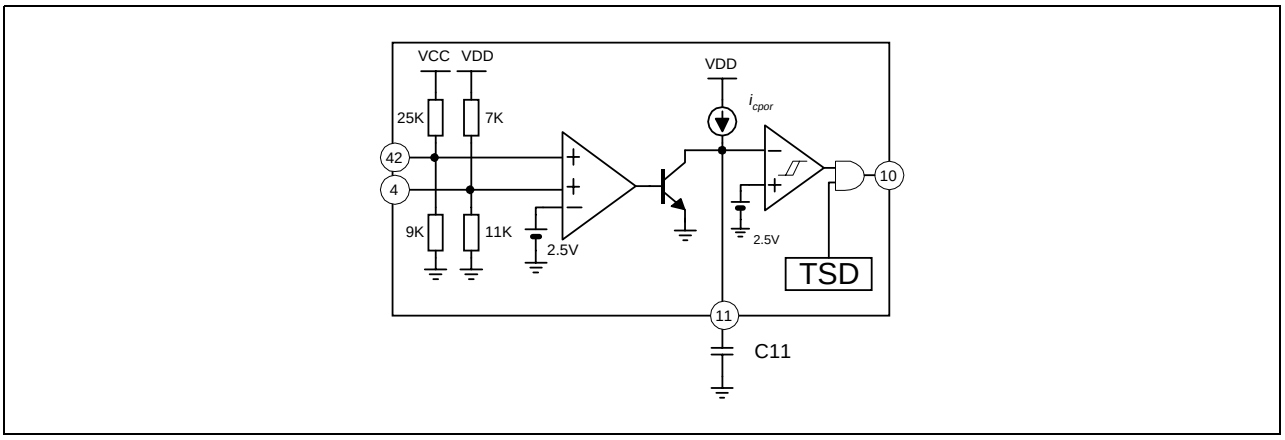


Figure 8. Power Line Sensing and POR

POR delay time is calculated by following formula

$$T_{dly} = C11 \cdot \frac{2.5}{I_{cpor}}$$

Regulator

An external passive element and two resistors generate regulated 3.3V supply suitable for external digital logic operating at the reduced voltage. Regulator output voltage is defined by resistor divider

$$V_{reg} = 1.3\left(1 + \frac{R3a}{R3b}\right)$$

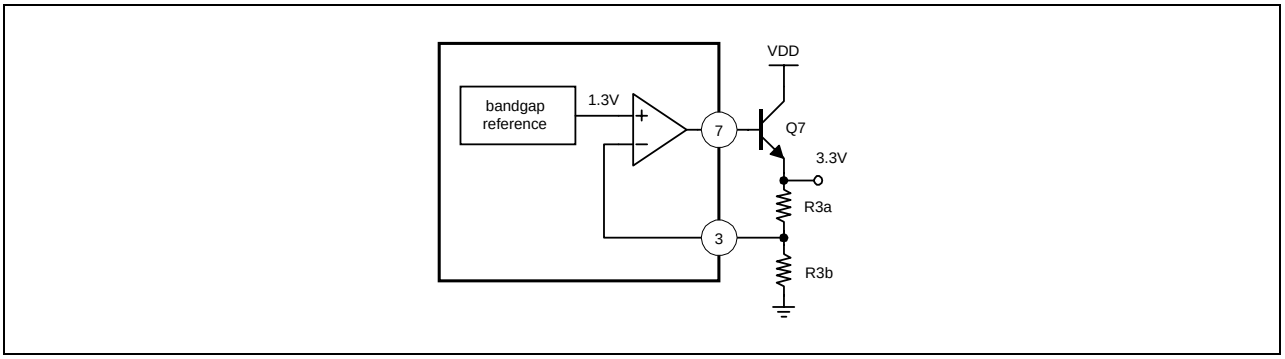
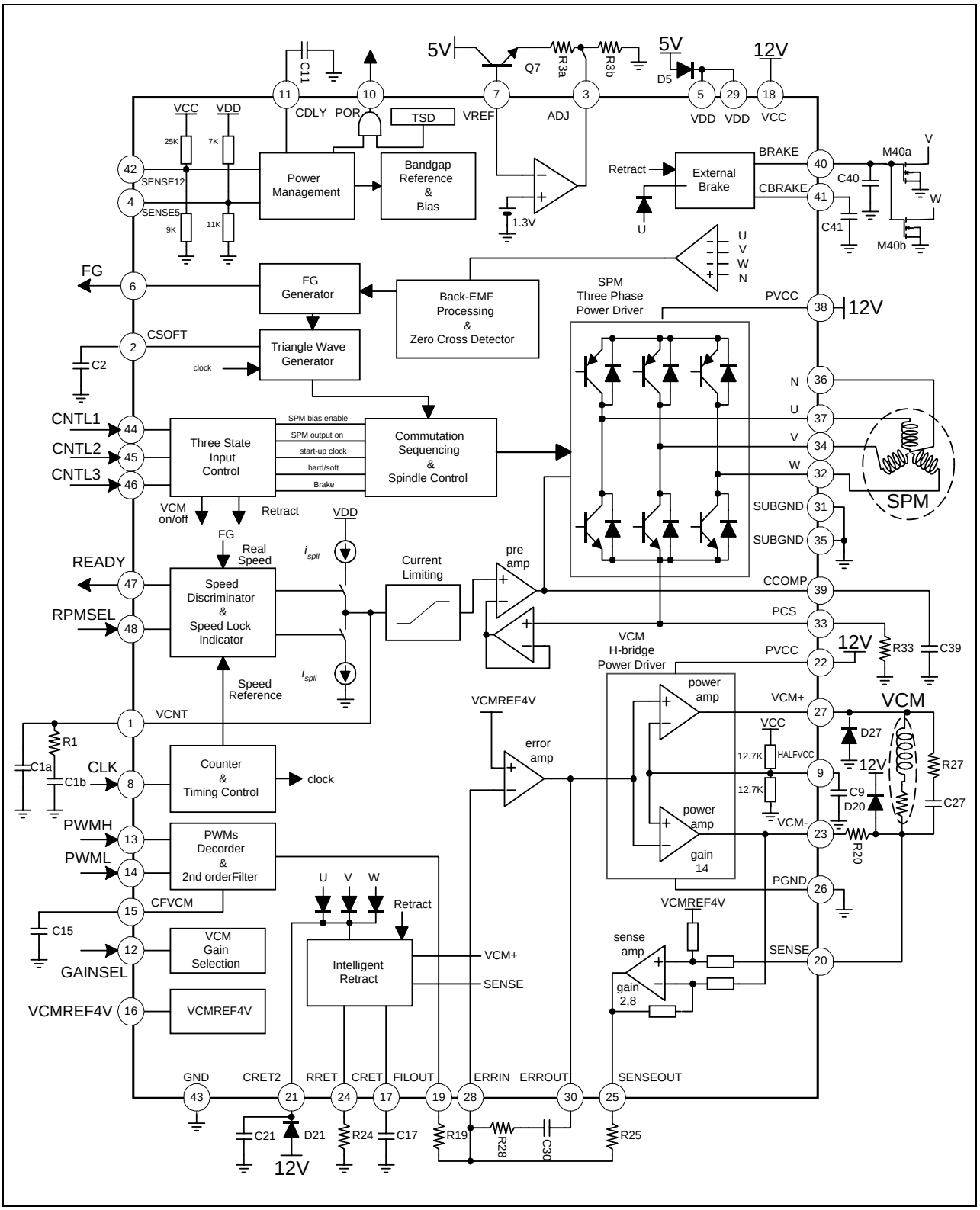


Figure 9. Regulator Output for Digital ASIC

Thermal Shut Down

A TSD circuit is included to protect the chip from damaging during momentary shorts that might occur during prototyping and troubleshooting. The trip temperature is set to 150°C with 30°C hysteresis. A thermal fault starts retract and braking operation and also makes POR pin low.

Typical Application Circuits



Parts List

Part NO.	Value	Type
R1	280K	1/8W
R3A	15K	1/8W
R3B	10K	1/8W
R19	6K	1/8W
R20	1	1/2W
R24	2.2K	1/8W
R25	4K	1/8W
R27	30	1/4W
R28	2.2K	1/4W
R33	0.33	1W
C1A	1μ	ELECTROLYTIC, 6V
C1B	0.22μ	CERAMIC, 6V
C2	27n	CERAMIC, 6V
C11	0.047μ	CERAMIC, 16V
C15	0.68n	CERAMIC, 10V
C17	1μ	ELECTROLYTIC, 16V
C21	2.2μ	ELECTROLYTIC,16V
C30	33n	CERAMIC,16V
C39	0.1μ	CERAMIC,16V
C40	0.47μ	ELECTROLYTIC,16V
C41	2.2μ	ELECTROLYTIC,16V
Q7	KSH29	D-PACK
M40A	SSD2003	8SOP
M40B	SSD2003	8SOP
D5	RB4110	SOT23
D20	RB4110	SOT23
D21	RB4110	SOT23
D27	RB4110	SOT23

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