M6MGB/T166S4BWG

16,777,216-BIT (1,048,576 -WORD BY 16-BIT) CMOS
3.3V-ONLY FLASH MEMORY &
4,194,304-BIT (262,144-WORD BY 16-BIT) CMOS SRAM
Stacked-CSP (Chip Scale Package)

DESCRIPTION

The MITSUBISHI M6MGB/T166S4BWG is a Stacked Chip Scale Package (S-CSP) that contents 16M-bits flash memory and 4M-bits Static RAM in a 72-pin S-CSP.

16M-bits Flash memory is a 1,048,576 words, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR(DIvided bit-line NOR) architecture for the memory cell.

4M-bits SRAM is a 262,144words unsynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MGB/T166S4BWG is suitable for the application of the mobile-communication-system to reduce both the mount space and weight .
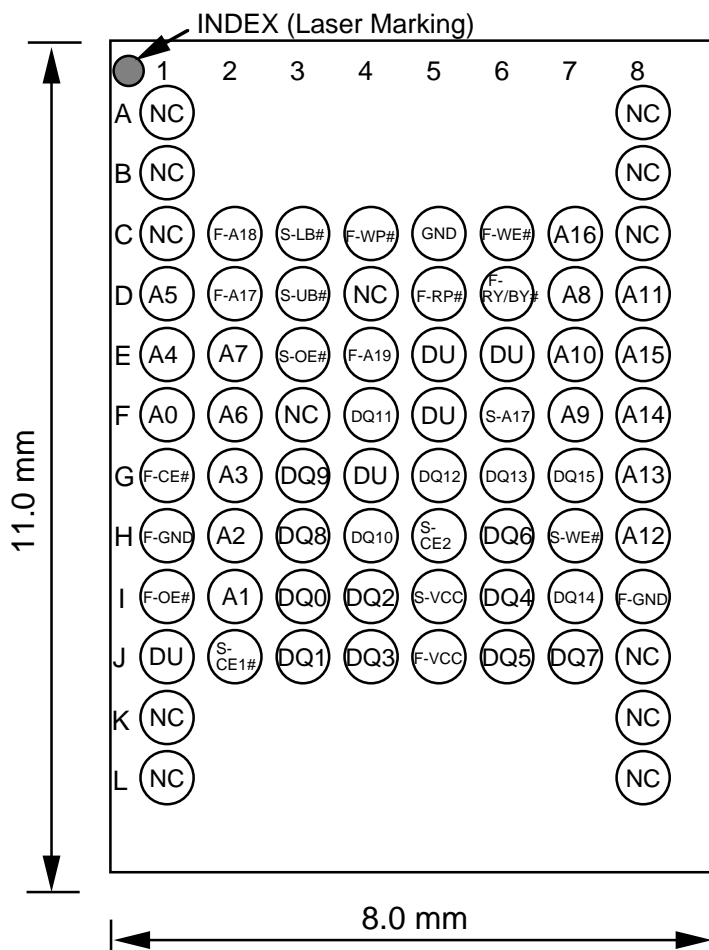
FEATURES

- Access time

Flash Memory	90ns (Max.)
SRAM	85ns (Max.)

- Supply voltage   Vcc=2.7 ~ 3.6V
- Ambient temperature
                I   version   Ta=-40 ~ 85°C
- Package : 72-pin S-CSP , 0.8mm ball pitch

APPLICATION

Mobile communication products

PIN CONFIGURATION (TOP VIEW)


F-VCC	:Vcc for Flash
S-VCC	:Vcc for SRAM
F-GND	:GND for Flash
GND	:Flash/SRAM common GND
A0-A16	:Flash/SRAM common Address
F-A17-F-A19	:Address for Flash
S-A17	:Address for SRAM
DQ0-DQ15	:Flash/SRAM common Data I/O
F-CE#	:Flash Chip Enable
S-CE1#	:SRAM Chip Enable 1
S-CE2	:SRAM Chip Enable 2
F-OE#	:Flash Output Enable
S-OE#	:SRAM Output Enable
F-WE#	:Flash Write Enable
S-WE#	:SRAM Write Enable
F-WP#	:Flash Write Protect
F-RP#	:Flash Reset Power Down
F-RY/BY#	:Flash Ready /Busy
S-LB#	:SRAM Lower Byte
S-UB#	:SRAM Upper Byte

NC:Non Connection
DU:Don't Use (Note: Should be open)

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BLOCK DIAGRAM
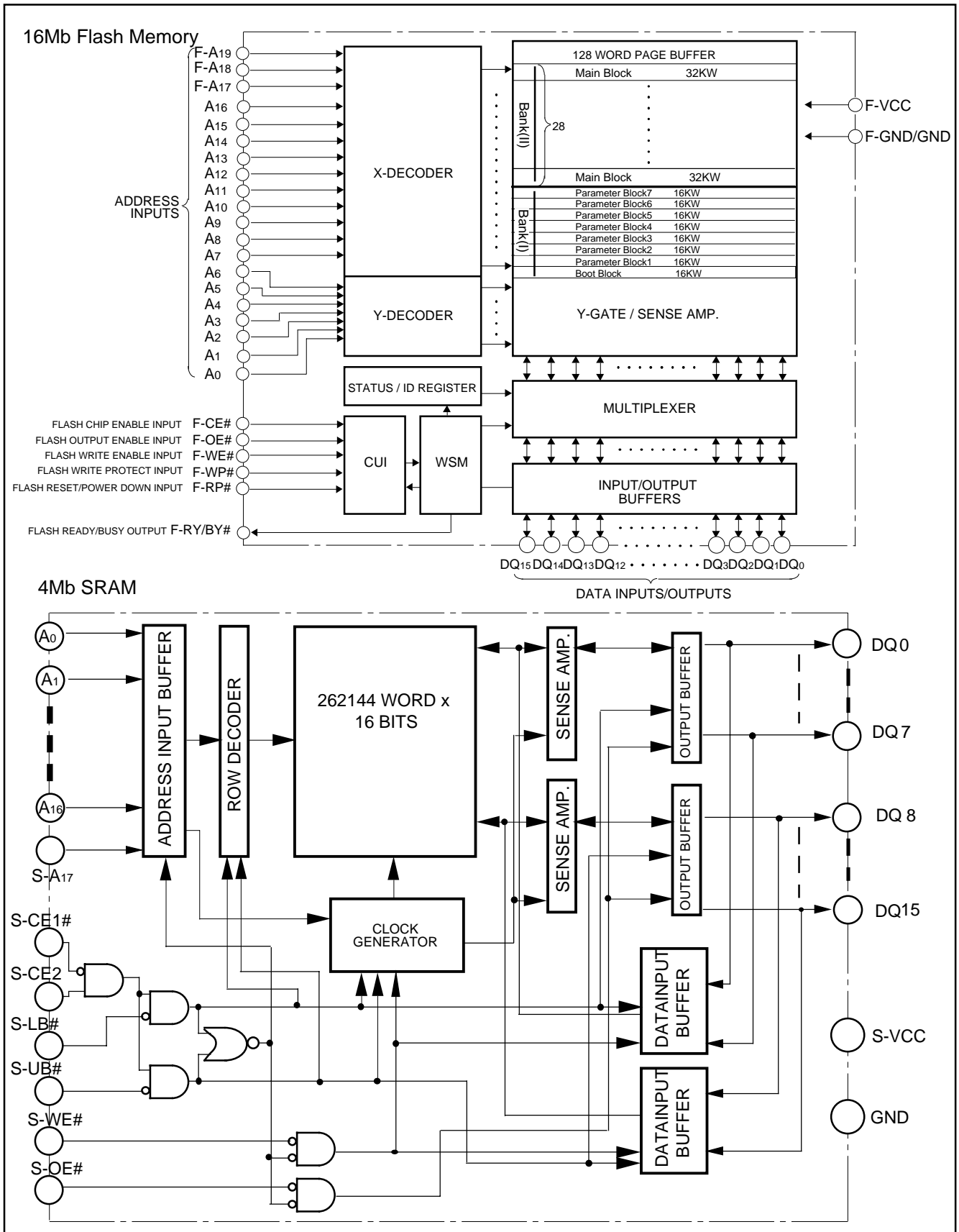
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1. Flash Memory

DESCRIPTION

The Flash Memory of M6MGB/T166S4BWG is 3.3V-only high speed 16,777,216-bit CMOS boot block Flash Memories with alternating BGO (Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for mobile and personal computing, and communication products. The Flash Memory of M6MGB/T166S4BWG is fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells.

FEATURES

- Organization ·······················1048,576 word x 16bit

- Supply voltage ·························· Vcc = 2.7~3.6V

- Access time ························· 90ns (Max.)

- Power Dissipation
  Read ································· 54 mW (Max. at 5MHz)
  (After Automatic Power Down) ········· 0.33μW (typ.)
  Program/Erase ·······················126 mW (Max.)
  Standby ································· 0.33μW (typ.)
  Deep power down mode ····················· 0.33μW (typ.)
- Auto program for Bank(I)
  Program Time ·························· 4ms (typ.)
  Program Unit
    (Byte Program) ·······················1word
    (Page Program) ·······················128word
- Auto program for Bank(II)
  Program Time ·························· 4ms (typ.)
  Program Unit ························· 128word
- Auto Erase
  Erase time ································· 40 ms (typ.)
  Erase Unit
    Bank(I) Boot Block ·················16Kword x 1
             Parameter Block ·········· 16Kword x 7
    Bank(II) Main Block ················32Kword x 28

- Program/Erase cycles ······································100Kcycles

- Boot Block
  M6MGB166S4BWG ························ Bottom Boot
  M6MGT166S4BWG ························ Top Boot

- Other Functions
  Soft Ware Command Control
  Selective Block Lock
  Erase Suspend/Resume
  Program Suspend/Resume
  Status Register Read
  Alternating Back Ground Program/Erase Operation
    Between Bank(I) and Bank(II)
  Auto Power Down Mode

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FUNCTION

The Flash Memory of M6MGB/T166S4BWG includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and byte/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Powerdown mode is enabled when the F-RP# pin is at GND, minimizing power consumption.

Read

The Flash Memory of M6MGB/T166S4BWG has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the Flash Memory automatically resets to read array mode. In the read array mode, low level input to F-CE# and F-OE#, high level input to F-WE# and F-RP#, and address signals to the address inputs (F-A19-F-A17,A16-A0) output the data of the addressed location to the data input/output (D15-D0).

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing F-WE# to low level, while F-CE# is at low level and F-OE# is at high level. Address and data are latched on the earlier rising edge of F-WE# and F-CE#. Standard micro-processor write timings are used.

Alternating Background Operation (BGO)

The Flash Memory of M6MGB/T166S4BWG allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Read array operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

Output Disable

When F-OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby

When F-CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down

When F-RP# is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.

During block erase or program modes, F-RP# low will abort either operation. Memory array data of the block being altered become invalid.

Automatic Power-Down (APD)

The Automatic Power-down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or F-CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. While in this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

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SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep powerdown, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Read Device Identifier Command (90H)

It can normally read device identifier codes when Read Device Identifier Code Command(90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 00000H and 00001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of F-OE# or F-CE#. So F-CE# or F-OE# must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands

A)Word Program (40H)

Word program is executed by a two-command sequence. The Word Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The Word Program Command is valid for only Bank(I).

B)Page Program for Data Blocks (41H)

Page Program for Bank(I) and Bank(II) allows fast programming of 128words of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle, write data must be serially inputted. Address A6-A0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

C)Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programing the data on the page buffer is cleared automatically.
This command is valid for only Bank(I) alike Word Program.

Clear Page Buffer Command (55H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The Flash Memory of M6MGB/T166S4BWG provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the Flash Memory has a master Write Protect pin (F-WP#) which prevents any modifications to memory blocks whose lock-bits are set to "0", when F-WP# is low. When F-WP# is high, all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase. See the BLOCK LOCKING table on P.9 for details.

Power Supply Voltage

When the power supply voltage (F-VCC) is less than V_{LKO}, Low V_{CC} Lock-Out voltage, the device is set to the Read-only mode. Regarding DC electrical characteristics of V_{LKO}, see P.10.
A delay time of $2\mu s$ is required before any device operation is initiated. The delay time is measured from the time F-Vcc reaches F-Vccmin (2.7V).
During power up, F-RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

MEMORY ORGANIZATION

The Flash Memory of M6MGB/T166S4BWG has one 16Kword boot block, seven 16Kword parameter blocks, for Bank(I) and twenty-eight 32Kword main blocks for Bank(II). A block is erased independently of other blocks in the array.

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MEMORY ORGANIZATION

Address	Block	Bank
F8000H-FFFFFH	32Kword MAIN BLOCK 35	BANK(II)
F0000H-F7FFFH	32Kword MAIN BLOCK 34	
E8000H-EFFFFH	32Kword MAIN BLOCK 33	
E0000H-E7FFFH	32Kword MAIN BLOCK 32	
D8000H-DFFFFH	32Kword MAIN BLOCK 31	
D0000H-D7FFFH	32Kword MAIN BLOCK 30	
C8000H-CFFFFH	32Kword MAIN BLOCK 29	
C0000H-C7FFFH	32Kword MAIN BLOCK 28	
B8000H-BFFFFH	32Kword MAIN BLOCK 27	
B0000H-B7FFFH	32Kword MAIN BLOCK 26	
A8000H-AFFFFH	32Kword MAIN BLOCK 25	
A0000H-A7FFFH	32Kword MAIN BLOCK 24	
98000H-9FFFFH	32Kword MAIN BLOCK 23	
90000H-97FFFH	32Kword MAIN BLOCK 22	
88000H-8FFFFH	32Kword MAIN BLOCK 21	
80000H-87FFFH	32Kword MAIN BLOCK 20	
78000H-7FFFFH	32Kword MAIN BLOCK 19	
70000H-77FFFH	32Kword MAIN BLOCK 18	
68000H-6FFFFH	32Kword MAIN BLOCK 17	
60000H-67FFFH	32Kword MAIN BLOCK 16	
58000H-5FFFFH	32Kword MAIN BLOCK 15	
50000H-57FFFH	32Kword MAIN BLOCK 14	
48000H-4FFFFH	32Kword MAIN BLOCK 13	
40000H-47FFFH	32Kword MAIN BLOCK 12	
38000H-3FFFFH	32Kword MAIN BLOCK 11	
30000H-37FFFH	32Kword MAIN BLOCK 10	
28000H-2FFFFH	32Kword MAIN BLOCK 9	
20000H-27FFFH	32Kword MAIN BLOCK 8	
1C000H-1FFFFH	16Kword PARAMETER BLOCK 7	BANK(I)
18000H-1BFFFH	16Kword PARAMETER BLOCK 6	
14000H-17FFFH	16Kword PARAMETER BLOCK 5	
10000H-13FFFH	16Kword PARAMETER BLOCK 4	
0C000H-0FFFFH	16Kword PARAMETER BLOCK 3	
08000H-0BFFFH	16Kword PARAMETER BLOCK 2	
04000H-07FFFH	16Kword PARAMETER BLOCK 1	
00000H-03FFFH	16Kword BOOT BLOCK 0	

$F-A_{19}-F-A_{17}, A_{16}-A_0$
(Word Mode)

**Flash Memory of M6MGB166S4BWG
Memory Map**

Address	Block	Bank
FC000H-FFFFFH	16Kword BOOT BLOCK 35	BANK(I)
F8000H-FBFFFH	16Kword PARAMETER BLOCK 34	
F4000H-F7FFFH	16Kword PARAMETER BLOCK 33	
F0000H-F3FFFH	16Kword PARAMETER BLOCK 32	
EC000H-EFFFFH	16Kword PARAMETER BLOCK 31	
E8000H-EBFFFH	16Kword PARAMETER BLOCK 30	
E4000H-E7FFFH	16Kword PARAMETER BLOCK 29	
E0000H-E3FFFH	16Kword PARAMETER BLOCK 28	
D8000H-DFFFFH	32Kword MAIN BLOCK 27	BANK(II)
D0000H-D7FFFH	32Kword MAIN BLOCK 26	
C8000H-CFFFFH	32Kword MAIN BLOCK 25	
C0000H-C7FFFH	32Kword MAIN BLOCK 24	
B8000H-BFFFFH	32Kword MAIN BLOCK 23	
B0000H-B7FFFH	32Kword MAIN BLOCK 22	
A8000H-AFFFFH	32Kword MAIN BLOCK 21	
A0000H-A7FFFH	32Kword MAIN BLOCK 20	
98000H-9FFFFH	32Kword MAIN BLOCK 19	
90000H-97FFFH	32Kword MAIN BLOCK 18	
88000H-8FFFFH	32Kword MAIN BLOCK 17	
80000H-87FFFH	32Kword MAIN BLOCK 16	
78000H-7FFFFH	32Kword MAIN BLOCK 15	
70000H-77FFFH	32Kword MAIN BLOCK 14	
68000H-6FFFFH	32Kword MAIN BLOCK 13	
60000H-67FFFH	32Kword MAIN BLOCK 12	
58000H-5FFFFH	32Kword MAIN BLOCK 11	
50000H-57FFFH	32Kword MAIN BLOCK 10	
48000H-4FFFFH	32Kword MAIN BLOCK 9	
40000H-47FFFH	32Kword MAIN BLOCK 8	
38000H-3FFFFH	32Kword MAIN BLOCK 7	
30000H-37FFFH	32Kword MAIN BLOCK 6	
28000H-2FFFFH	32Kword MAIN BLOCK 5	
20000H-27FFFH	32Kword MAIN BLOCK 4	
18000H-1FFFFH	32Kword MAIN BLOCK 3	
10000H-17FFFH	32Kword MAIN BLOCK 2	
08000H-0FFFFH	32Kword MAIN BLOCK 1	
00000H-07FFFH	32Kword MAIN BLOCK 0	

$F-A_{19}-F-A_{17}, A_{16}-A_0$
(Word Mode)

**Flash Memory of M6MGT166S4BWG
Memory Map**

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BUS OPERATIONS

Bus Operations for Word-Wide Mode

Mode	Pins	F-CE#	F-OE#	F-WE#	F-RP#	DQ$_{0-15}$	F-RY/BY#
Read	Array	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IH}$	Data out	V$_{OH (Hi-Z)}$
	Status Register	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IH}$	Status Register Data	X [1]
	Lock Bit Status	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IH}$	Lock Bit Data (DQ$_6$)	X
	Identifier Code	V$_{IL}$	V$_{IL}$	V$_{IH}$	V$_{IH}$	Identifier Code	V$_{OH (Hi-Z)}$
Output disable		V$_{IL}$	V$_{IH}$	V$_{IH}$	V$_{IH}$	Hi-Z	X
Stand by		V$_{IH}$	X [2]	X	V$_{IH}$	Hi-Z	X
Write	Program	V$_{IL}$	V$_{IH}$	V$_{IL}$	V$_{IH}$	Command/Data in	X
	Erase	V$_{IL}$	V$_{IH}$	V$_{IL}$	V$_{IH}$	Command	X
	Others	V$_{IL}$	V$_{IH}$	V$_{IL}$	V$_{IH}$	Command	X
Deep Power Down		X	X	X	V$_{IL}$	Hi-Z	V$_{OH (Hi-Z)}$

1) X at F-RY/BY# is V$_{OL}$ or V$_{OH(Hi-Z)}$.
*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.
2) X can be V$_{IH}$ or V$_{IL}$ for control pins.

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SOFTWARE COMMAND DEFINITION

Command List

Command	1st bus cycle			2nd bus cycle			3rd ~129th bus cycles (Word Mode)		
	Mode	Address	Data (DQ15-0)	Mode	Address	Data (DQ15-0)	Mode	Address	Data (DQ15-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA [2]	ID [2]			
Read Status Register	Write	Bank[3]	70H	Read	Bank	SRD[4]			
Clear Status Register	Write	X	50H						
Clear Page Buffer	Write	X	55H	Write	X	D0H [1]			
Word Program [5]	Write	Bank(I) [5]	40H	Write	WA [6]	WD [6]			
Page Program [7]	Write	Bank	41H	Write	WA0 [7]	WD0 [7]	Write	WAn [7]	WDn [7]
Single Data Load to Page Buffer [5]	Write	Bank(I) [5]	74H	Write	WA	WD			
Page Buffer to Flash [5]	Write	Bank(I) [5]	0EH	Write	WA [8]	D0H [1]			
Block Erase / Confirm	Write	Bank	20H	Write	BA [9]	D0H [1]			
Suspend	Write	Bank	B0H						
Resume	Write	Bank	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 [10]			
Lock Bit Program / Confirm	Write	Bank	77H	Write	BA	D0H [1]			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H [1]			

1) Upper byte data (DQ8-DQ15) is ignored.
2) IA=ID Code Address : A0=VIL (Manufacturer's Code) : A0=VIH (Device Code), ID=ID Code
3) Bank = Bank Address (Bank(I) or Bank(II)) : F-A19-F-A17.
4) SRD = Status Register Data
5) Word Program, Single Data Load and Page Buffer to Flash Command is valid for only Bank(I).
6) WA = Write Address,WD = Write Data
7) WA0,WAn=Write Address, WD0,WDn=Write Data.
   Write Address and Write Data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128word (128word x 16bit).
   and also F-A19-F-A17,A16-A7(Block Address, Page Address) must be valid.
8) WA = Write Address : Upper page address, F-A19-F-A17,A16-A7(Block Address, Page Address) must be valid.
9) BA = Block Address : BA = Block Address : F-A19-F-A17,A16-A14(Bank1) F-A19-F-A17,A16-A15(Bank2)
10) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.

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BLOCK LOCKING

F-RP#	F-WP#	Lock Bit (Internally)	Write Protection Provided BANK(I) Boot	Write Protection Provided BANK(I) Parameter	Write Protection Provided BANK(II) Data	Lock Bit	Note
V$_{IL}$	X	X	Locked	Locked	Locked	Locked	Deep Power Down Mode
V$_{IH}$	V$_{IL}$	0	Locked	Locked	Locked	Locked	
		1	Locked	Unlocked	Unlocked	Locked	
	V$_{IH}$	X	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

1) DQ6 provides Lock Status of each block after writing the Read Lock Status command (71H).
F-WP# pins must not be switched during performing Erase / Write operations or WSM Busy (WSMS = 0).
2) Erase/Write command for locked blocks is aborted. At this time read mode is not array read mode but status read mode and 00B0H is read. Please issue Clear Status Register command plus Read Array command to change the mode from status read mode to array read mode.

STATUS REGISTER

Symbol	Status	Definition "1"	Definition "0"
SR.7 (DQ7)	Write State Machine Status	Ready	Busy
SR.6 (DQ6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (DQ5)	Erase Status	Error	Successful
SR.4 (DQ4)	Program Status	Error	Successful
SR.3 (DQ3)	Block Status after Program	Error	Successful
SR.2 (DQ2)	*Reserved*	-	-
SR.1 (DQ1)	*Reserved*	-	-
SR.0 (DQ0)	*Reserved*	-	-

*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.

*DQ3 indicates the block status after the page programming, word programming and page buffer to flash. When DQ3 is "1", the page has the over-programed cell . If over-program occurs, the device is block fail. However if DQ3 is "1", please try the block erase to the block. The block may revive.

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DEVICE IDENTIFIER CODE

Code \ Pins	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Manufacturer Code	VIL	0	0	0	1	1	1	0	0	1CH
Device Code (-T166S4BWG)	VIH	1	0	1	0	0	0	0	0	A0H
Device Code (-B166S4BWG)	VIH	1	0	1	0	0	0	0	1	A1H

The upper data(D_{15-8}) is "0".

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
F-Vcc	Flash Vcc voltage	With respect to Ground	-0.2	4.6	V
VI1	All input or output voltage 1)		-0.6	4.6	V
Ta	Ambient temperature		-40	85	°C
Tbs	Temperature under bias		-50	95	°C
Tstg	Storage temperature		-65	125	°C
I OUT	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is (F-Vcc)+0.5V which, during transitions, may overshoot to (F-Vcc)+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CIN	Input capacitance (Address, Control Pins)	Ta = 25°C, f = 1MHz, Vin = Vout = 0V			8	pF
COUT	Output capacitance				12	pF

Note: The value of common pins to Flash Memory is the sum of Flash Memory and SRAM.

DC ELECTRICAL CHARACTERISTICS (Ta = -40~ 85°C, F-Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Min	Typ1)	Max	Unit
ILI	Input leakage current	0V≤VIN≤F-Vcc				±2.0	μA
ILO	Output leakage current	0V≤VOUT≤F-Vcc				±11	μA
ISB1		F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH			50	200	μA
ISB2	F-Vcc standby current	F-Vcc = 3.6V, VIN=GND or F-Vcc, F-CE# = F-RP# = F-WP# = (F-Vcc)±0.3V			0.1	5	μA
ISB3	F-Vcc deep powerdown current	F-Vcc = 3.6V, VIN=VIL/VIH, F-RP# = VIL			5	15	μA
ISB4		F-VCC = 3.6V, VIN=GND or F-VCC, F-RP# =GND±0.3V			0.1	5	μA
ICC1	F-Vcc read current for Word or Byte	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = VIL, F-RP#=F-OE#=VIH, IOUT = 0mA	5MHz		8	15	mA
			1MHz		2	4	
ICC2	F-Vcc Write current for Word or Byte	F-Vcc = 3.6V,VIN=VIL/VIH, F-CE# =F-WE#= VIL, F-RP#=F-OE#=VIH				15	mA
ICC3	F-Vcc program current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				35	mA
ICC4	F-Vcc erase current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				35	mA
ICC5	F-Vcc suspend current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				200	μA
VIL	Input low voltage			– 0.5		0.8	V
VIH	Input high voltage			2.0		(F-Vcc)+0.5	V
VOL	Output low voltage	IOL = 4.0mA				0.45	V
VOH1	Output high voltage	IOH = −2.0mA		0.85X(F-Vcc)			V
VOH2		IOH = −100μA		(F-Vcc)−0.4			V
VLKO	Low Vcc Lock-Out voltage 2)			1.5		2.2	V

All currents are in RMS unless otherwise noted.
1) Typical values at F-Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during F-Vcc power-up/ down, a write cycle is locked out for F-Vcc less than VLKO.
   If F-Vcc is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if F-Vcc is less than VLKO, the alteration of memory contents may occur.

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Stacked-CSP (Chip Scale Package)**

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~85°C, F-Vcc = 2.7V ~3.6V)
Read-Only Mode

Symbol		Parameter	Limits F-Vcc=2.7-3.6V 90ns			Unit
			Min	Typ	Max	
tRC	tAVAV	Read cycle time	90			ns
ta (AD)	tAVQV	Address access time			90	ns
ta (CE)	tELQV	Chip enable access time			90	ns
ta (OE)	tGLQV	Output enable access time			30	ns
tCLZ	tELQX	Chip enable to output in low-Z	0			ns
tDF(CE)	tEHQZ	Chip enable high to output in high Z			25	ns
tOLZ	tGLQX	Output enable to output in low-Z	0			ns
tDF(OE)	tGHQZ	Output enable high to output in high Z			25	ns
tPHZ	tPLQZ	F-RP# low to output high-Z			150	ns
tOH	tOH	Output hold from F-CE#, OE#, addresses	0			ns
tPS	tPHEL	F-RP# recovery to F-CE# low	150			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~85°C, F-Vcc = 2.7V ~3.6V)
Write Mode (F-WE# control)

Symbol		Parameter	Limits F-Vcc=2.7-3.6V 90ns			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	90			ns
tAS	tAVWH	Address set-up time	50			ns
tAH	tWHAX	Address hold time	0			ns
tDS	tDVWH	Data set-up time	50			ns
tDH	tWHDX	Data hold time	0			ns
tOEH	tWHGL	F-OE# hold from F-WE# high	10			ns
tRE	-	Latency between Read and Write FFH or 71H	30			ns
tCS	tELWL	Chip enable set-up time	0			ns
tCH	tWHEH	Chip enable hold time	0			ns
tWP	tWLWH	Write pulse width	50			ns
tWPH	tWHWL	Write pulse width high	30			ns
tGHWL	tGHWL	F-OE# hold to F-WE# Low	0			ns
tBLS	tPHHWH	Block Lock set-up to write enable high	90			ns
tBLH	tQVPH	Block Lockhold from valid SRD	0			ns
tDAP	tWHRH1	Duration of auto-program operation		4	80	ms
tDAE	tWHRH2	Duration of auto-block erase operation		40	600	ms
tWHRL	tWHRL	Write enable high to F-RY/BY# low			90	ns
tPS	tPHWL	F-RP# high recovery to write enable low	150			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at F-Vcc=3.3V, Ta=25°C

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AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~ 85°C, F-Vcc = 2.7V ~ 3.6V)

Write Mode (F-CE# control)

Symbol		Parameter	Limits F-Vcc=2.7-3.6V 90ns			Unit
			Min	Typ	Max	
tWC	tAVAV	Write cycle time	90			ns
tAS	tAVWH	Address set-up time	50			ns
tAH	tEHAX	Address hold time	0			ns
tDS	tDVWH	Data set-up time	50			ns
tDH	tEHDX	Data hold time	0			ns
tOEH	tEHGL	F-OE# hold from F-CE# high	10			ns
tRE	-	Latency between Read and Write FFH or 71H	30			ns
tWS	tWLEL	Write enable set-up time	0			ns
tWH	tEHWH	Write enable hold time	0			ns
tCEP	tELEH	F-CE# pulse width	60			ns
tCEPH	tEHEL	F-CE# pulse width high	30			ns
tGHEL	tGHEL	F-OE# hold to F-CE# Low	90			ns
tBLS	tPHHEH	Block Lock set-up to write enable high	90			ns
tBLH	tQVPH	Block Lockhold from valid SRD	0			ns
tDAP	tEHRH1	Duration of auto-program operation		4	80	ms
tDAE	tEHRH2	Duration of auto-block erase operation		40	600	ms
tEHRL	tEHRL	F-CE# high to F-RY/BY# low			90	ns
tPS	tPHWL	F-RP# high recovery to write enable low	150			ns

Read timing parameters during command write operation mode are the same as during read-only operation mode.
Typical values at F-Vcc=3.3V, Ta=25°C

Erase and Program Performance

Parameter	Min	Typ	Max	Unit
Block Erase Time		40	600	ms
Main Block Write Time (Page Mode)		1.0	1.8	sec
Page Write Time		4	80	ms

Program Suspend Latency / Erase Suspend Time

Parameter	Min	Typ	Max	Unit
Program Suspend Latency			15	μs
Erase Suspend Time			15	μs

Please see page 20.

Vcc Power Up / Down Timing

| Symbol	Parameter	Min	Typ	Max	Unit
tVCS	F-RP# =VIH set-up time from Vccmin	2			μs

Please see page 13.

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2μsec is always required before read operation or write operation is initiated from the time F-Vcc reaches F-Vccmin
during power up/down.
By holding F-RP# VIL, the contents of memory is protected during F-Vcc power up/down.
During power up, F-RP# must be held VIL for min.2μs from the time F-Vcc reaches F-Vccmin.
During power down, F-RP# must be held VIL until Vcc reaches GND.
F-RP# doesn't have latch mode ,therefore F-RP# must be held VIH during read operation or erase/program operation.
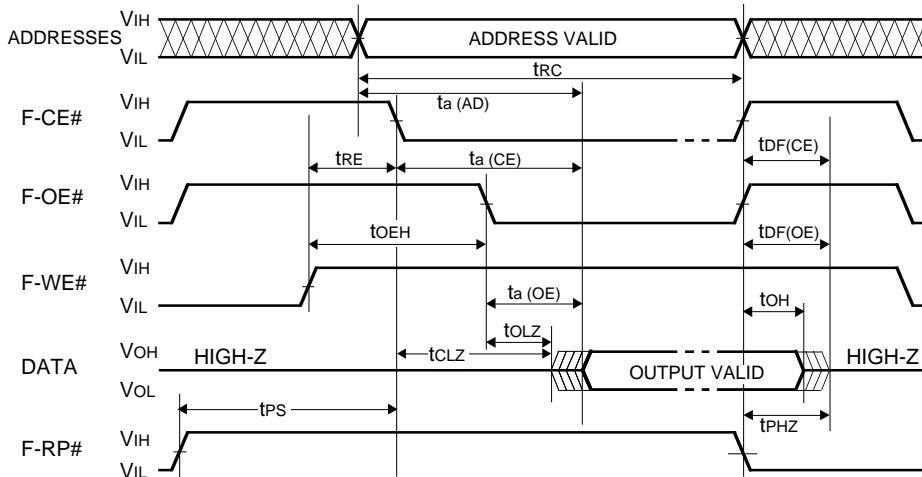
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Vcc POWER UP / DOWN TIMING
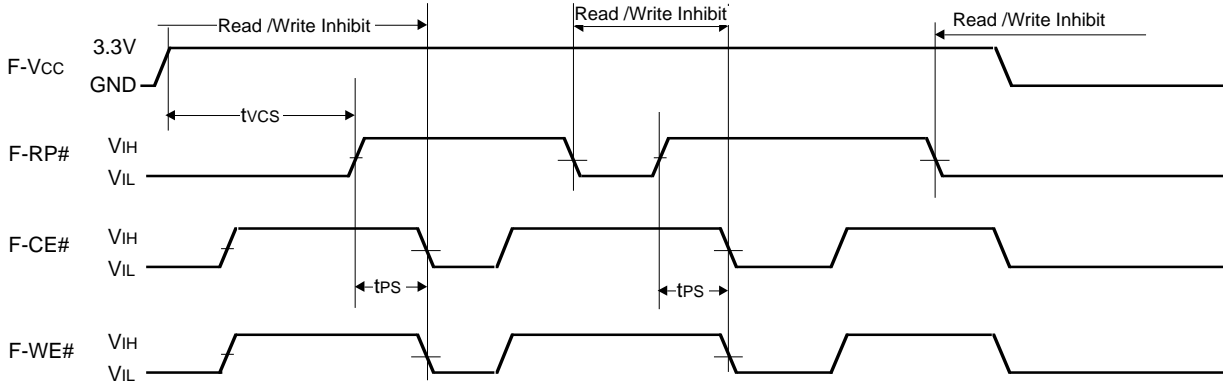
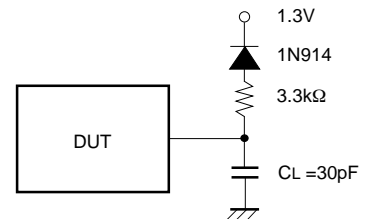

AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS
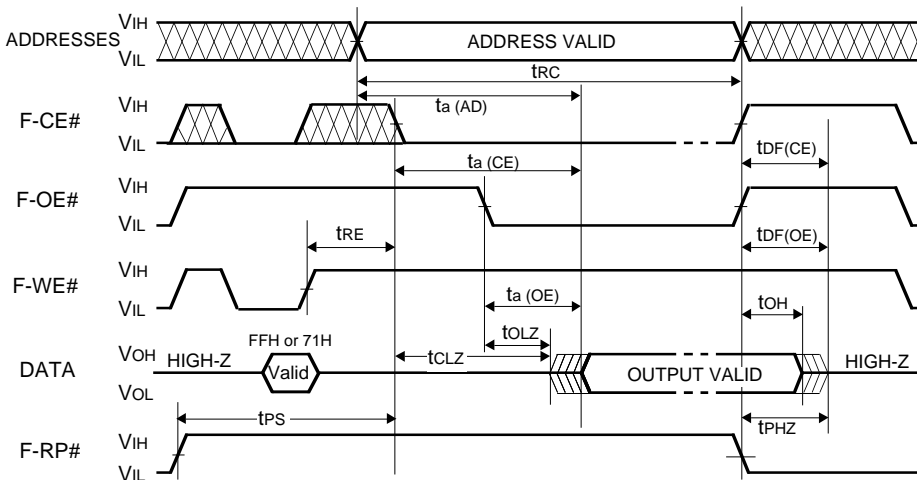

TEST CONDITIONS
  FOR AC CHARACTERISTICS

Input voltage : V_{IL} = 0V, V_{IH} = 3.0V
Input rise and fall times : ≤5ns
Reference voltage
at timing measurement : 1.5V

Output load : 1TTL gate +
                    CL(30pF)
or

AC WAVEFORMS FOR WRITE FFH or 71H AND READ OPERATION

In the case of use F-CE# is Low fixed, it is allowed to define a timming specification of tRE
from rising edge of F-WE# to falling edge of F-OE#, and valid data is read after spec of tRE+ta(CE).
(This is only for FFH,71H program and read)

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AC WAVEFORMS FOR PAGE PROGRAM OPERATION (F-WE# control)
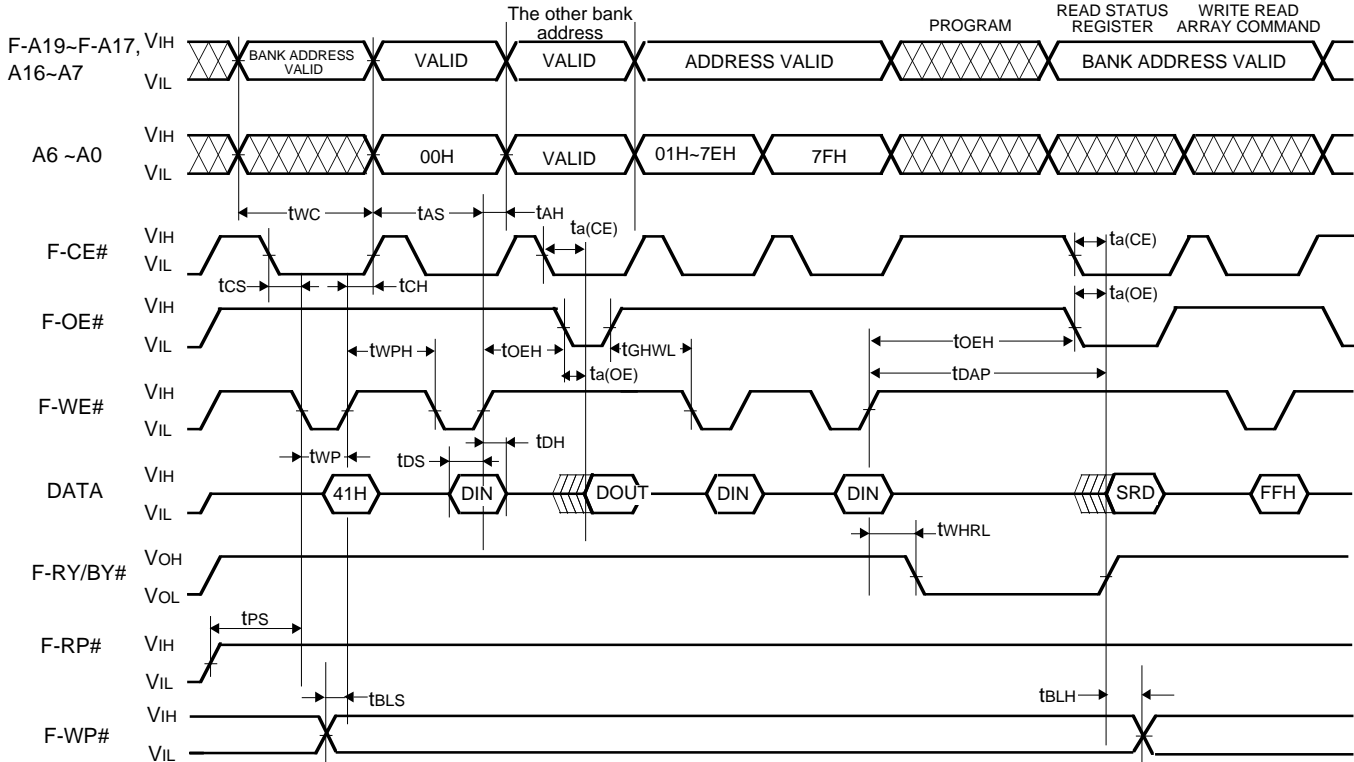
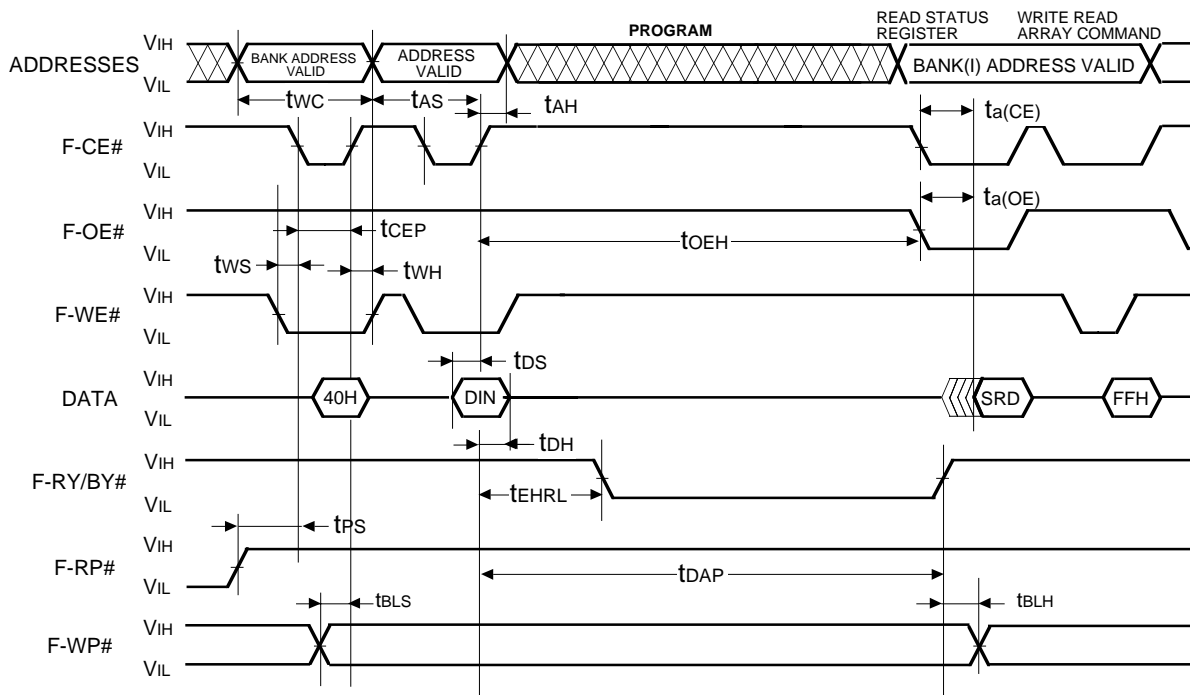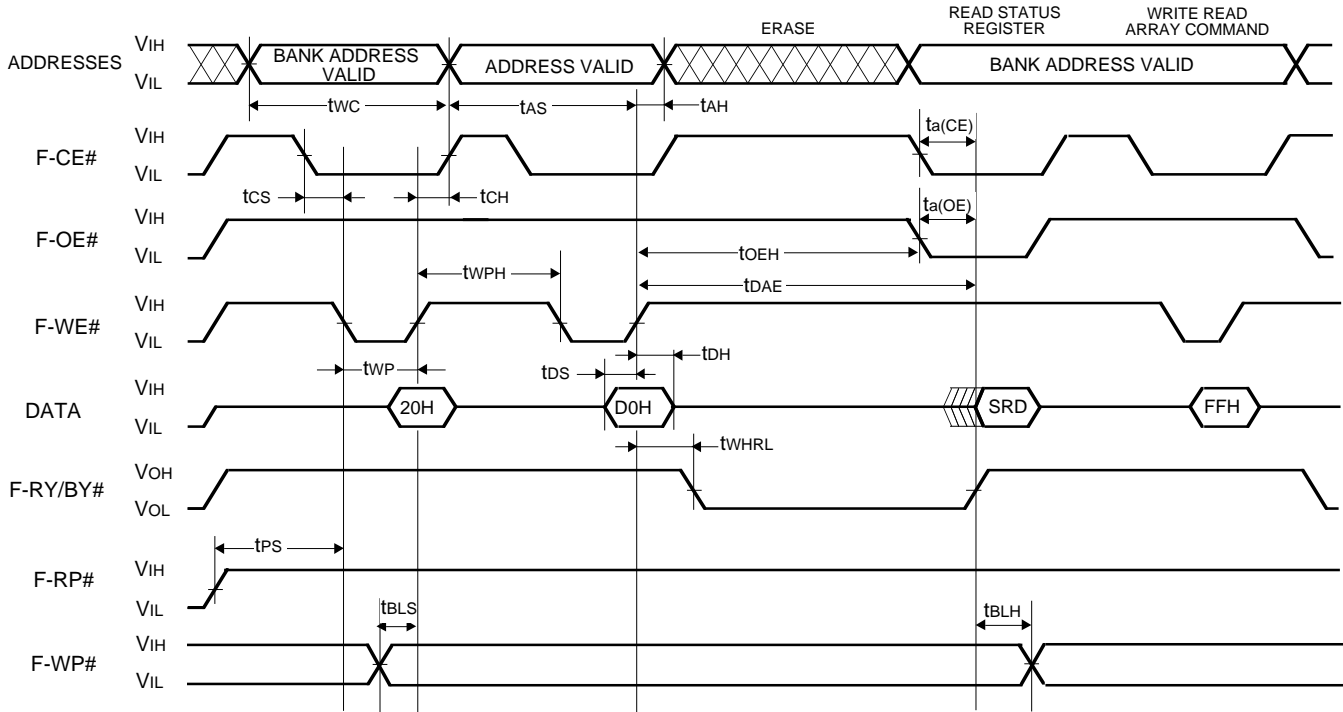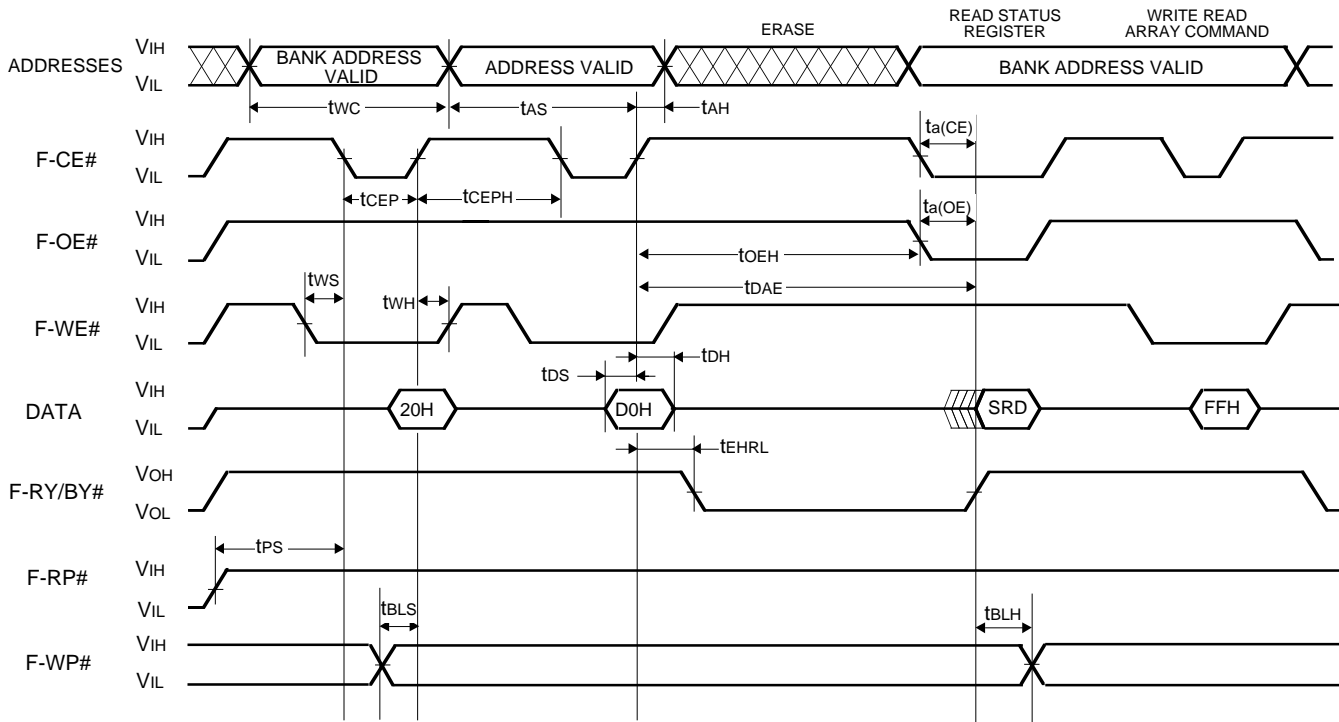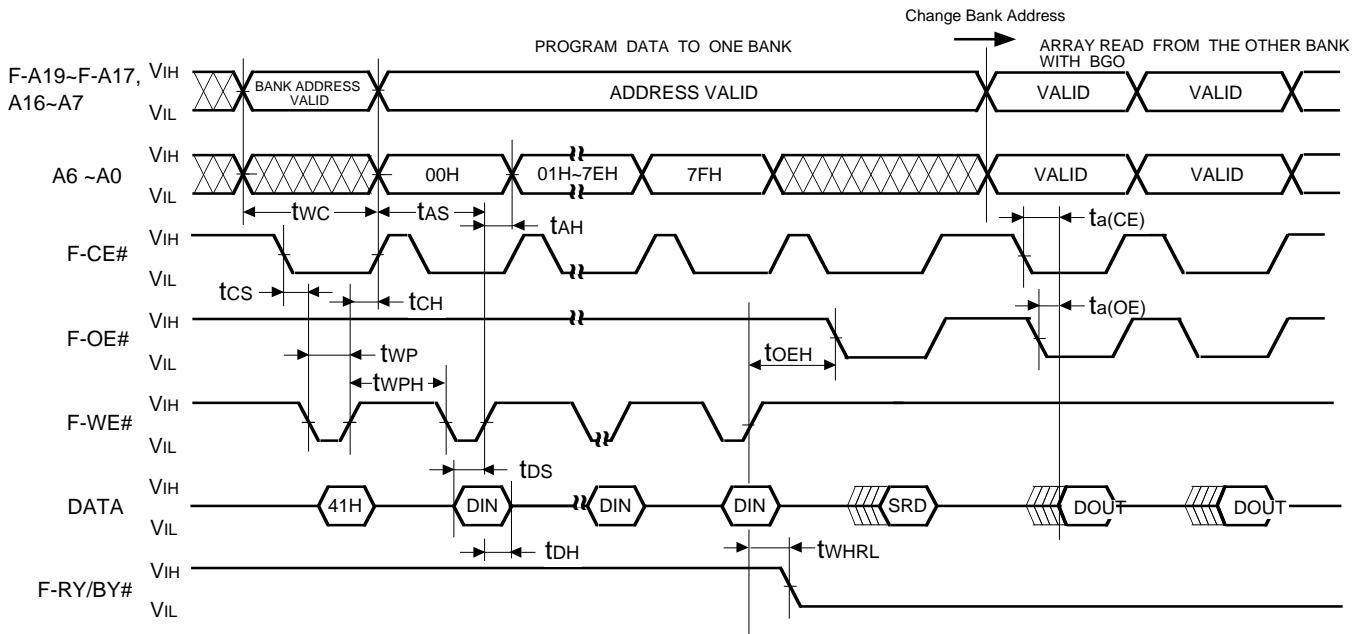## AC WAVEFORMS FOR PAGE PROGRAM OPERATION (F-CE# control)
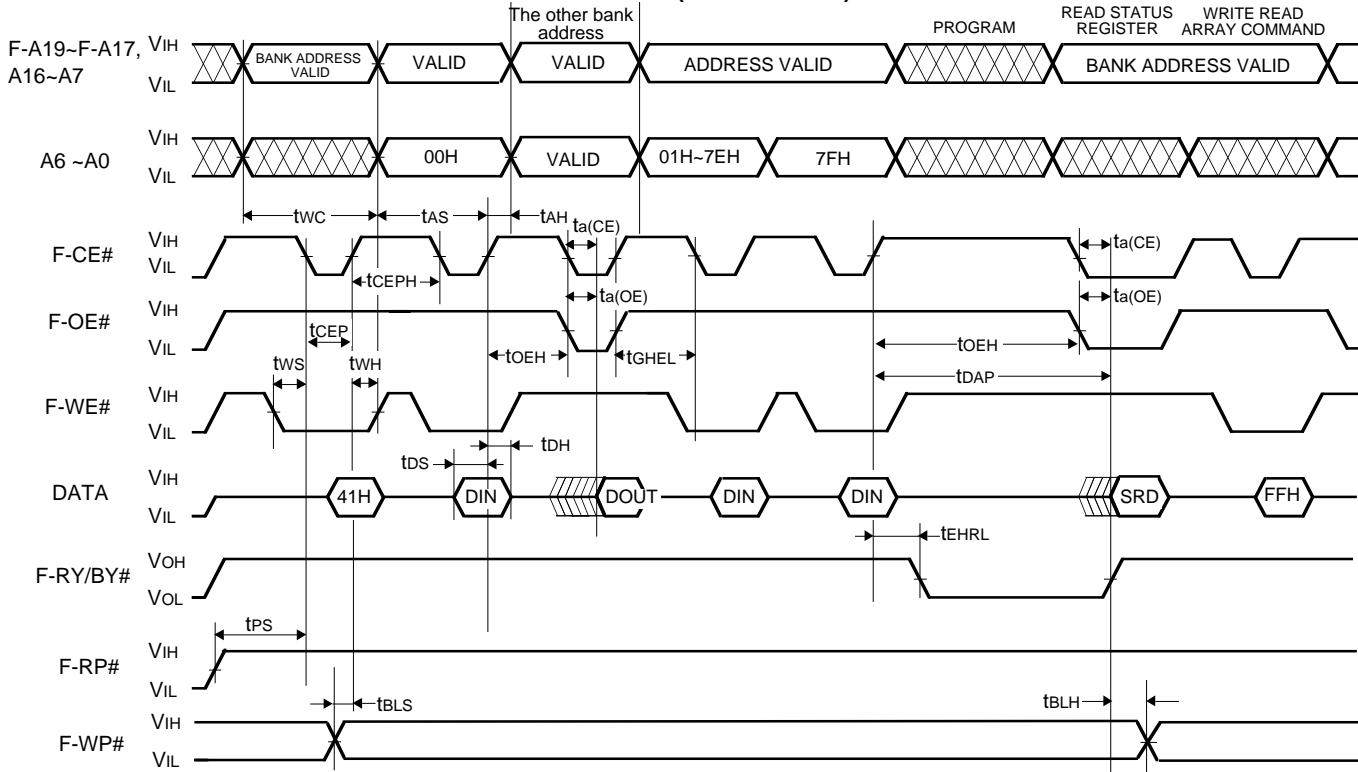
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AC WAVEFORMS FOR WORD PROGRAM OPERATION (F-WE# control) (to only BANK(I))
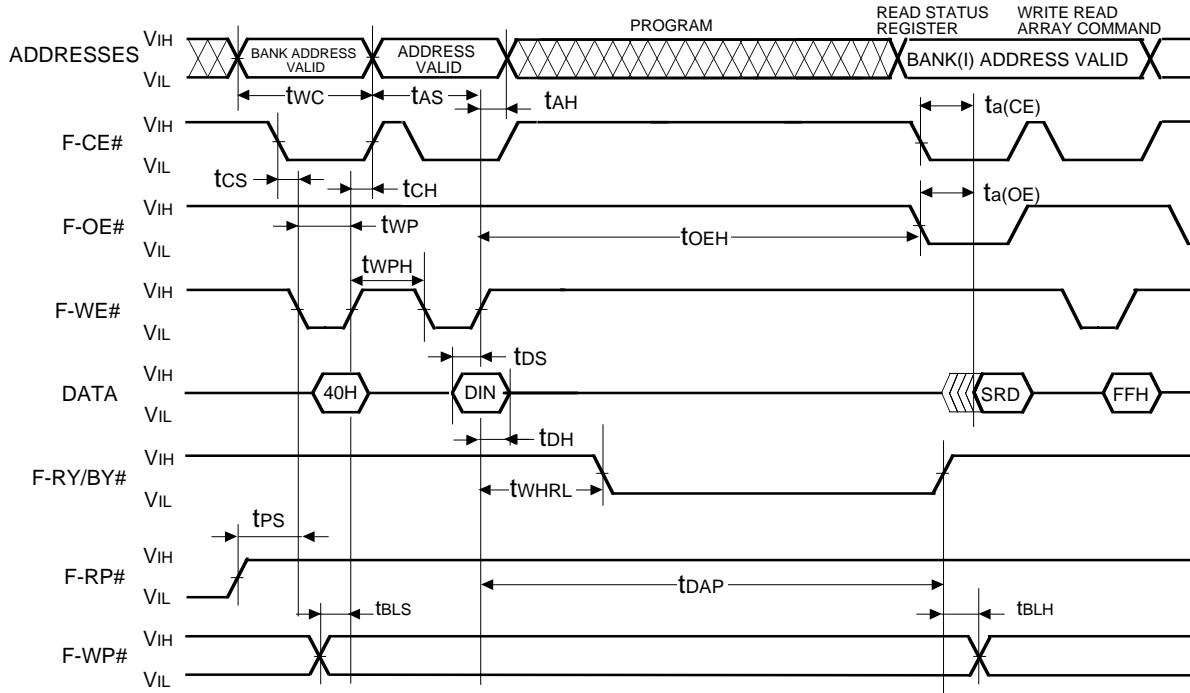
AC WAVEFORMS FOR WORD PROGRAM OPERATION (F-CE# control) (to only BANK(I))
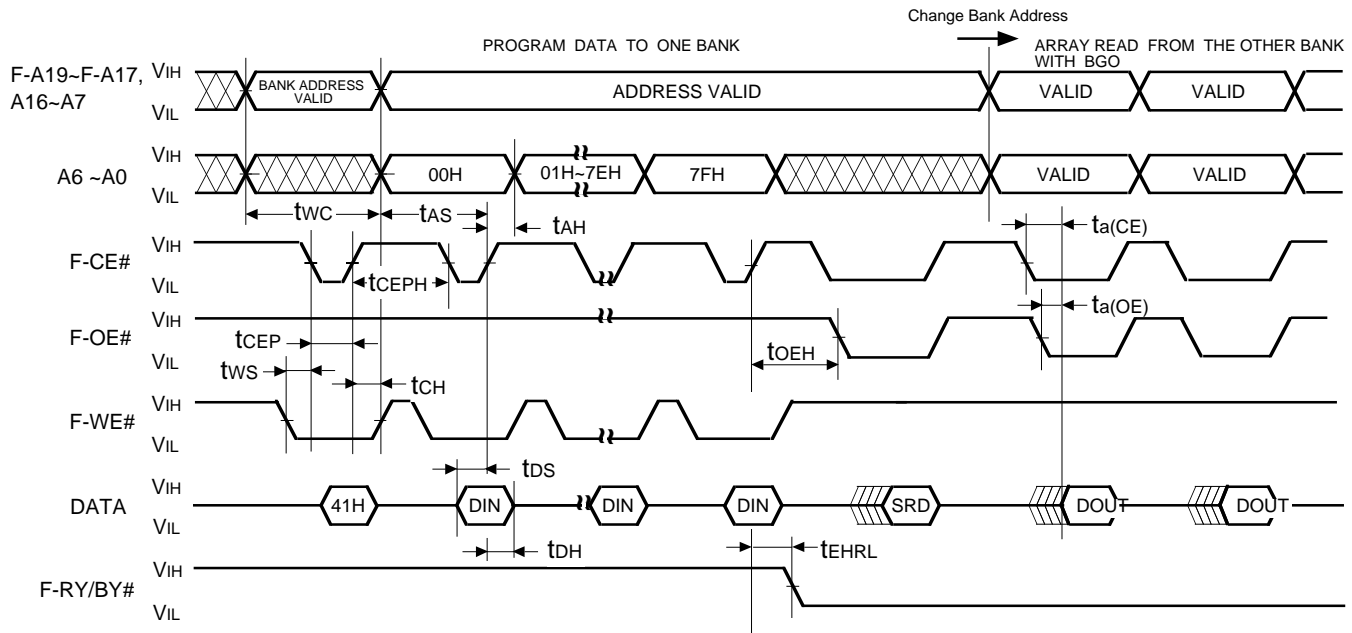
MITSUBISHI LSIs
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AC WAVEFORMS FOR ERASE OPERATIONS (F-WE# control)

AC WAVEFORMS FOR ERASE OPERATIONS (F-CE# control)

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Stacked-CSP (Chip Scale Package)

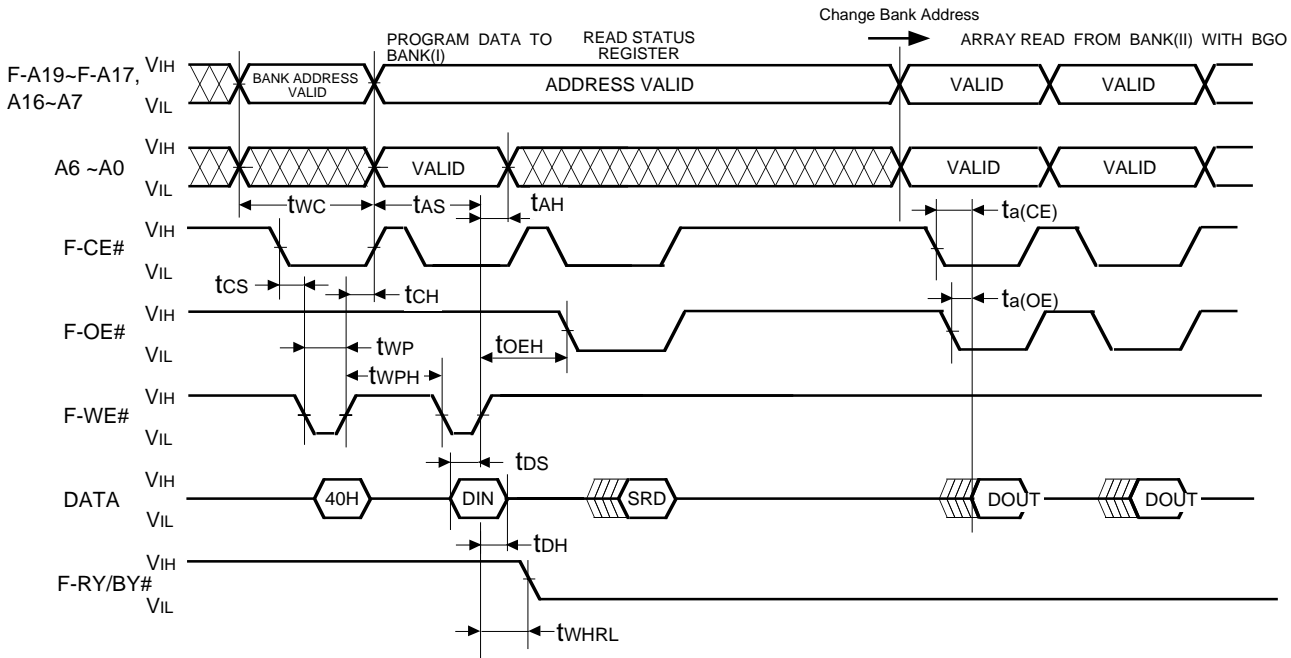## AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (F-WE# control)

AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (F-CE# control)
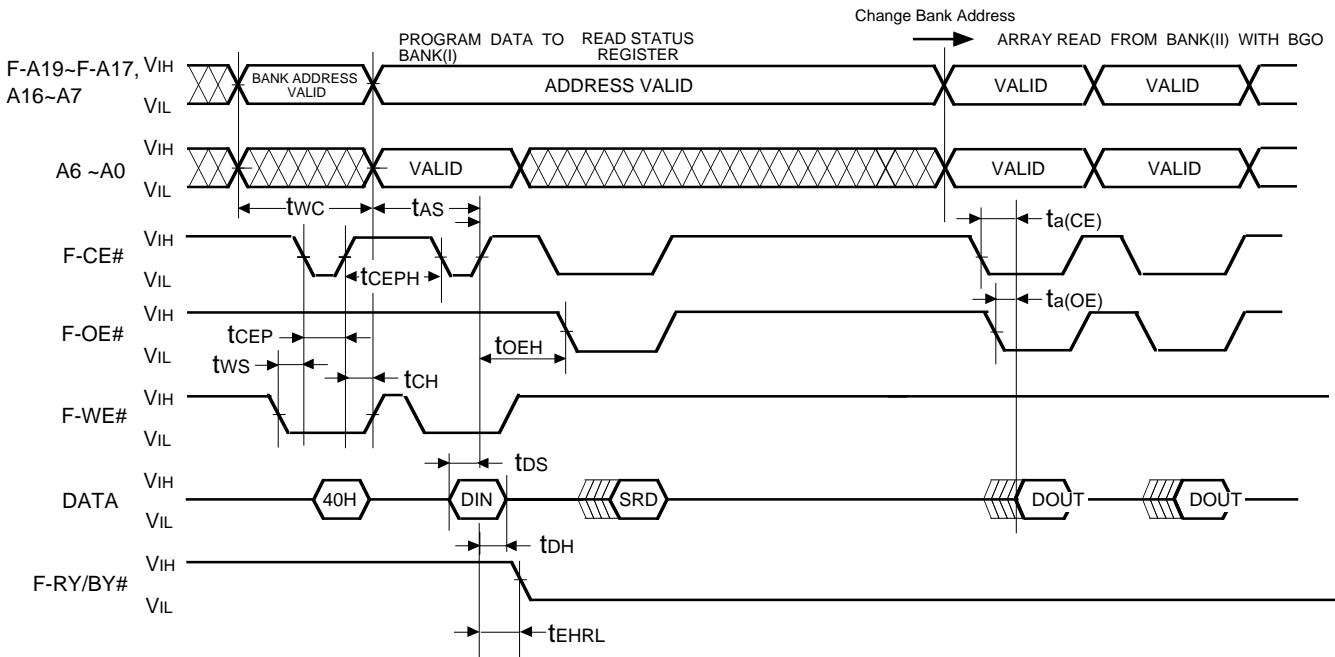
MITSUBISHI LSIs
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4,194,304-BIT (262,144-WORD BY 16-BIT) CMOS SRAM
Stacked-CSP (Chip Scale Package)**

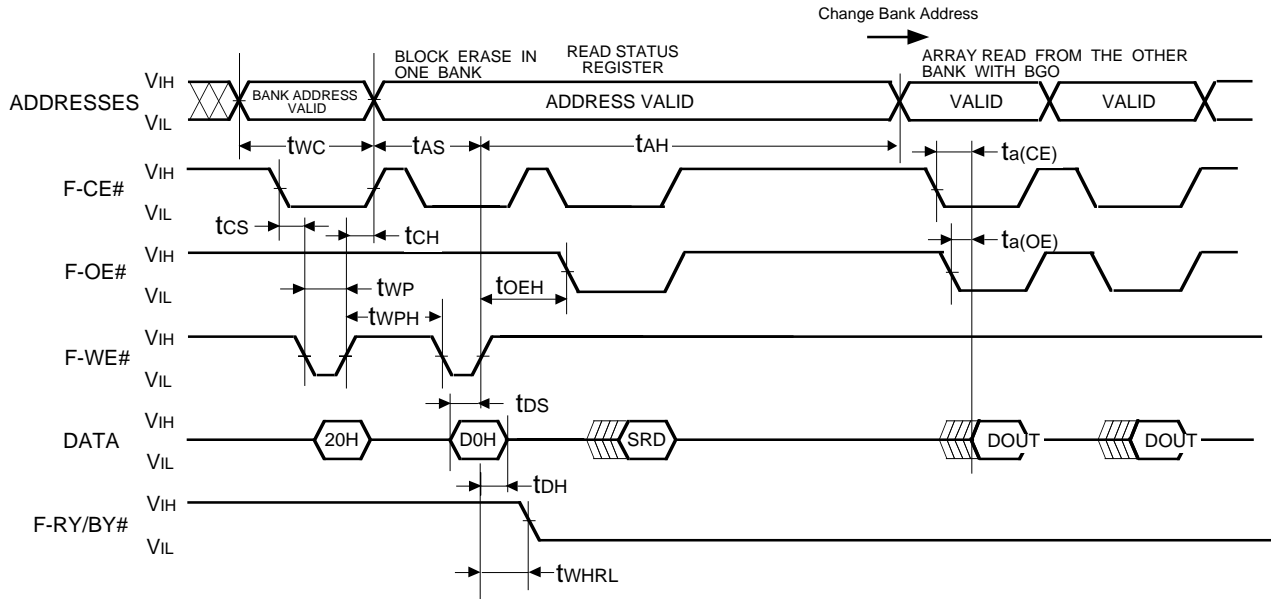## AC WAVEFORMS FOR WORD PROGRAM OPERATION WITH BGO (F-WE# control)

AC WAVEFORMS FOR WORD PROGRAM OPERATION WITH BGO (F-CE# control)

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Stacked-CSP (Chip Scale Package)

AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (F-WE# control)

AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (F-CE# control)
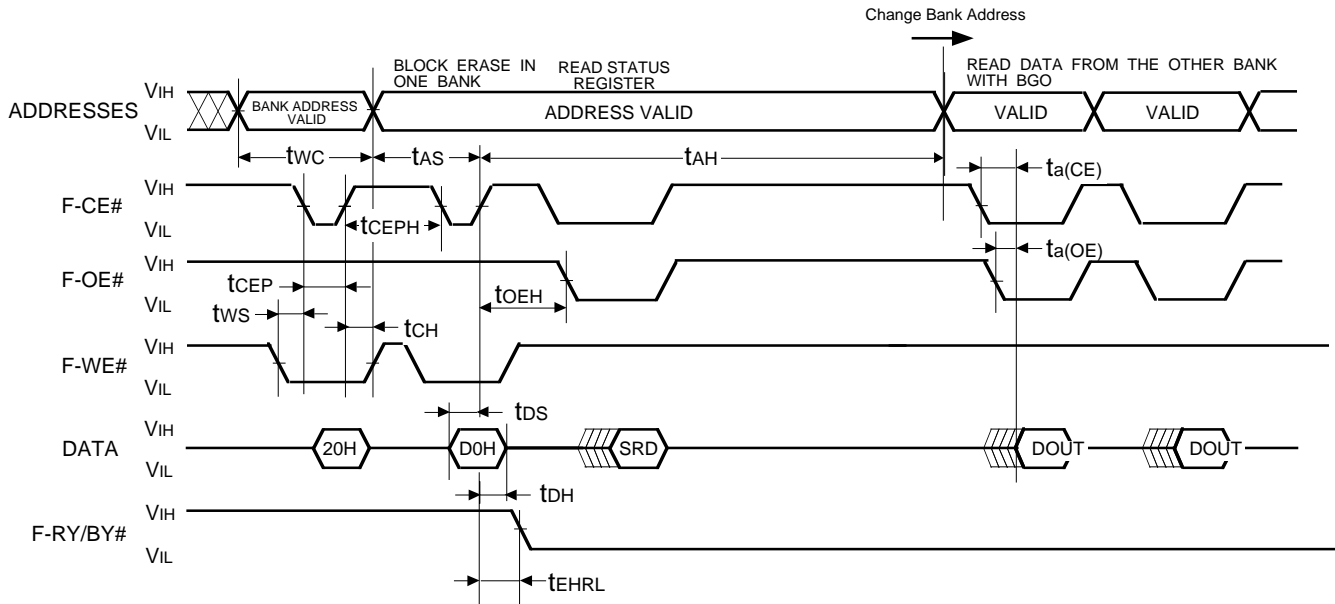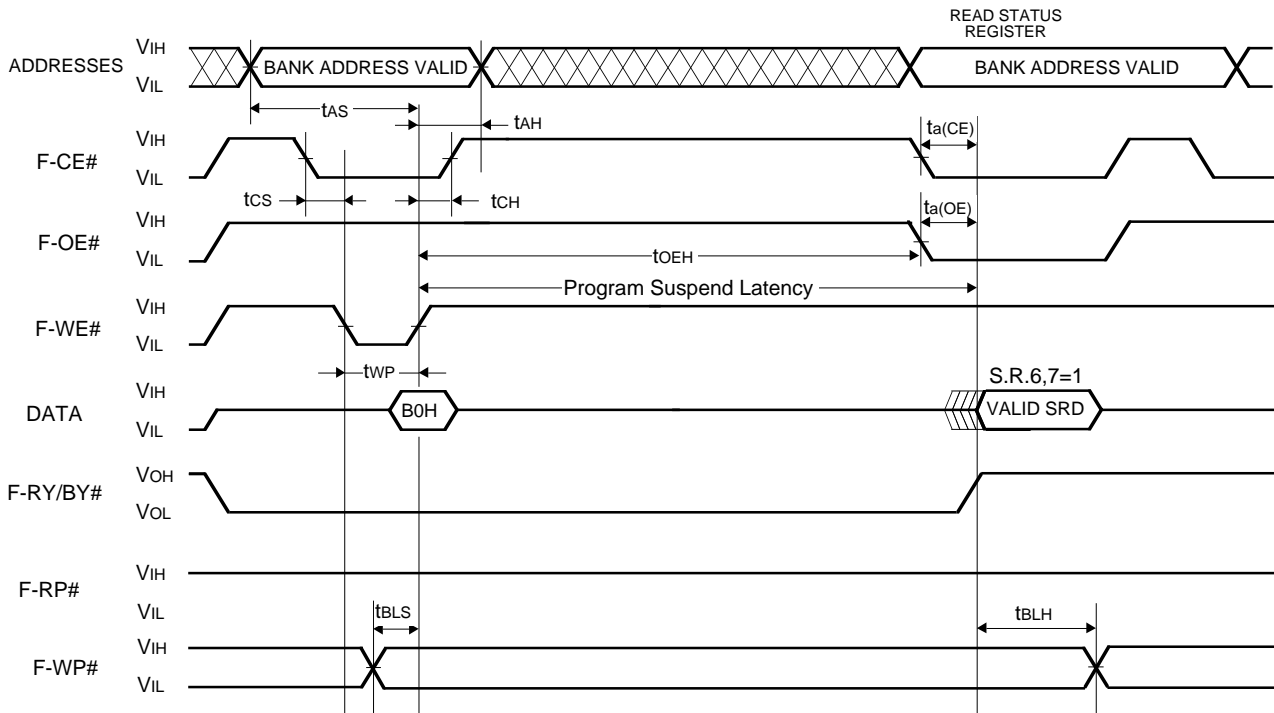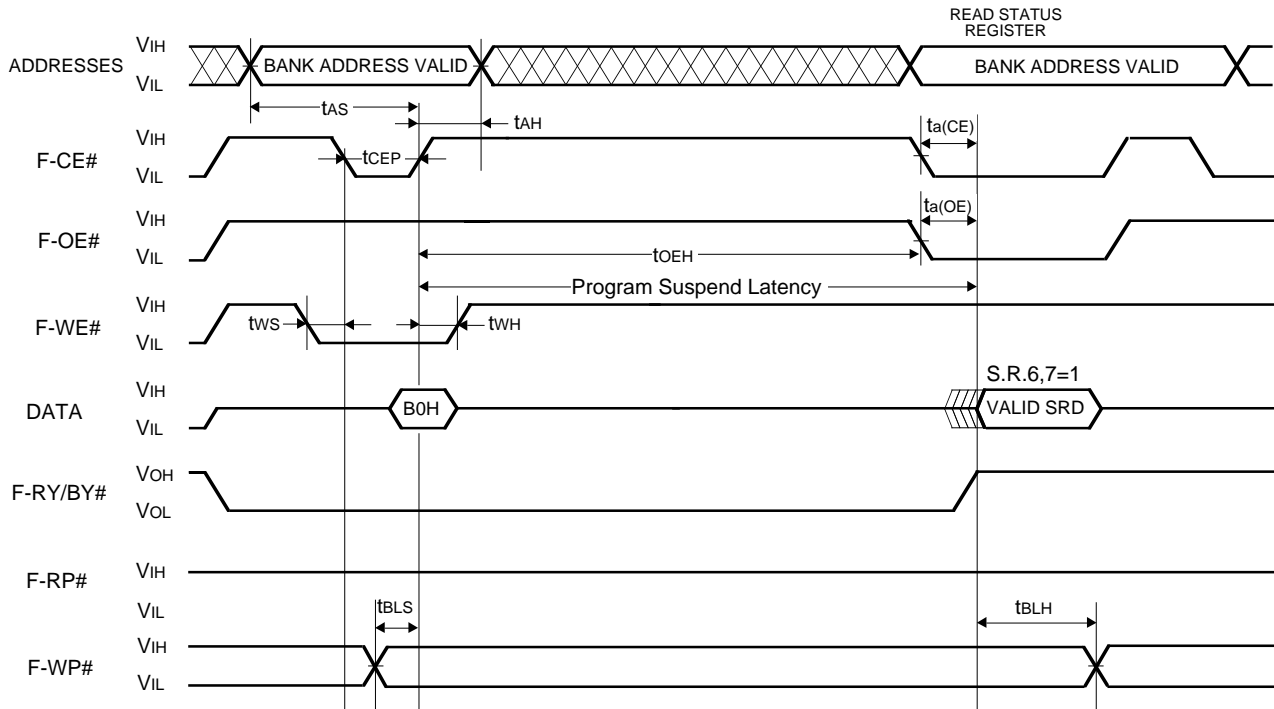
MITSUBISHI LSIs
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**16,777,216-BIT (1,048,576 -WORD BY 16-BIT) CMOS
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Stacked-CSP (Chip Scale Package)**

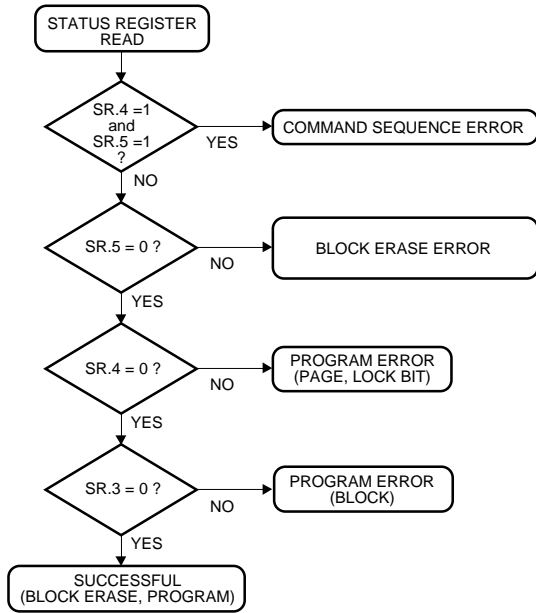## AC WAVEFORMS FOR SUSPEND OPERATION (F-WE# control)

AC WAVEFORMS FOR SUSPEND OPERATION (F-CE# control)

MITSUBISHI LSIs
M6MGB/T166S4BWG
16,777,216-BIT (1,048,576 -WORD BY 16-BIT) CMOS
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Stacked-CSP (Chip Scale Package)

FULL STATUS CHECK PROCEDURE

STATUS REGISTER READ

SR.4 =1 and SR.5 =1 ? — YES → COMMAND SEQUENCE ERROR

NO

SR.5 = 0 ? — NO → BLOCK ERASE ERROR

YES

SR.4 = 0 ? — NO → PROGRAM ERROR (PAGE, LOCK BIT)

YES

SR.3 = 0 ? — NO → PROGRAM ERROR (BLOCK)

YES

SUCCESSFUL (BLOCK ERASE, PROGRAM)

LOCK BIT PROGRAM FLOW CHART

START

WRITE 77H

WRITE D0H BLOCK ADDRESS

SR.7 = 1 ? — NO

YES

SR.4 = 0 ? — NO → LOCK BIT PROGRAM FAILED

YES

LOCK BIT PROGRAM SUCCESSFUL

WORD PROGRAM FLOW CHART

START

WRITE 40H

WRITE ADDRESS , DATA

STATUS REGISTER READ

SR.7 = 1 ? — NO → WRITE B0H ? — NO

YES

FULL STATUS CHECK IF DESIRED

WORD PROGRAM COMPLETED

WRITE B0H ? — YES → SUSPEND LOOP / WRITE D0H — YES

* Word program is admitted to only BANK(I).

PAGE PROGRAM FLOW CHART
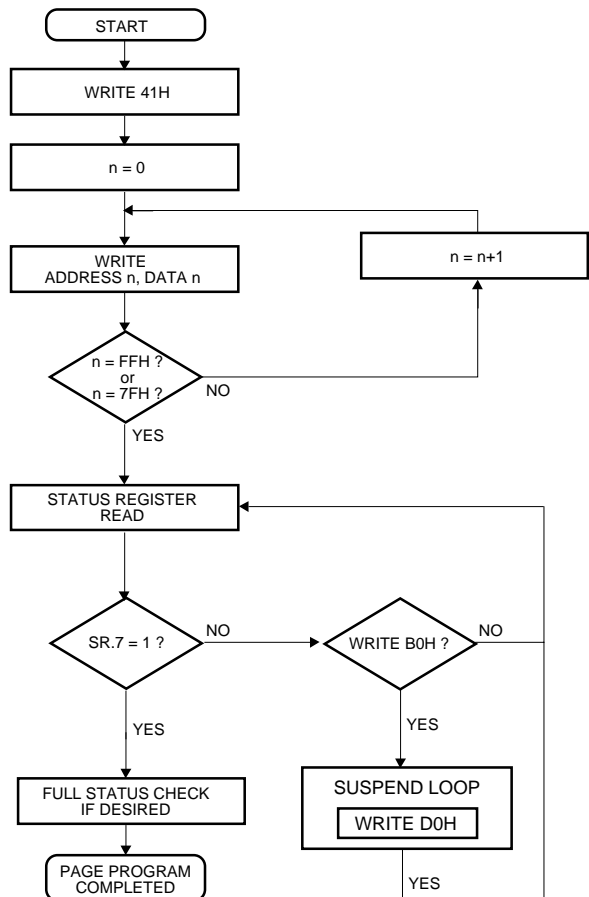
START

WRITE 41H

n = 0

WRITE ADDRESS n, DATA n

n = FFH ? or n = 7FH ? — NO → n = n+1

YES

STATUS REGISTER READ

SR.7 = 1 ? — NO → WRITE B0H ? — NO

YES

FULL STATUS CHECK IF DESIRED

PAGE PROGRAM COMPLETED

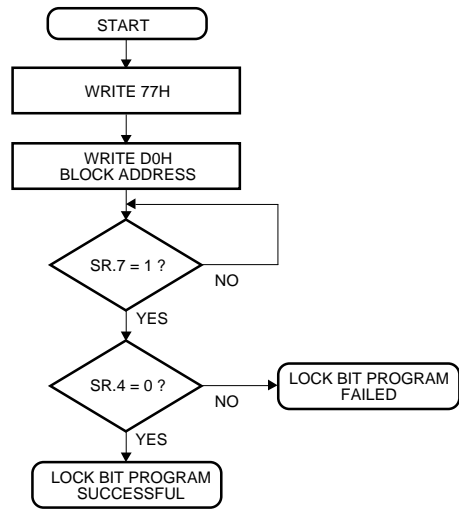WRITE B0H ? — YES → SUSPEND LOOP / WRITE D0H — YES

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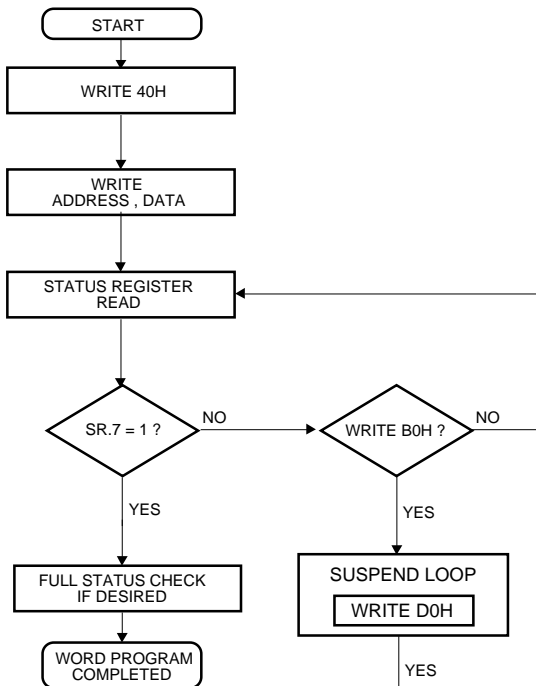Stacked-CSP (Chip Scale Package)**

CLEAR PAGE BUFFER

START

WRITE 55H

WRITE   D0H

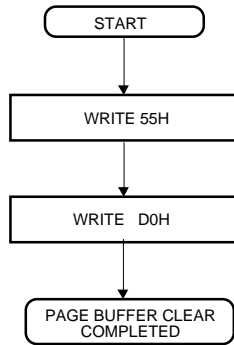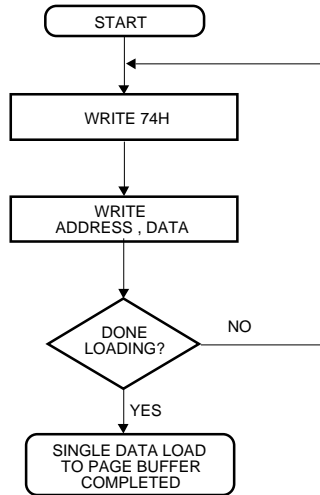PAGE BUFFER CLEAR
COMPLETED

SINGLE DATA LOAD TO PAGE BUFFER

START

WRITE 74H

WRITE
ADDRESS , DATA

DONE
LOADING?   — NO

YES

SINGLE DATA LOAD
TO PAGE BUFFER
COMPLETED

PAGE BUFFER TO FLASH

START

WRITE 0EH

WRITE D0H
PAGE ADDRESS

STATUS REGISTER
READ

SR.7 = 1 ?   — NO →   WRITE B0H ?   — NO

YES

FULL STATUS CHECK
IF DESIRED

PAGE BUFFER TO FLASH
COMPLETED

YES

SUSPEND LOOP
WRITE D0H

YES

SUSPEND / RESUME FLOW CHART

START

WRITE B0H   **SUSPEND**

STATUS REGISTER
READ

SR.7 = 1?   NO

YES

SR.6 =1?   NO →   PROGRAM / ERASE
COMPLETED

YES

WRITE FFH

READ ARRAY DATA

DONE
READING ?   NO

YES

WRITE D0H   **RESUME**

OPERATION
RESUMED

* The bank address is required when writing this command. Also, there is
  no need to suspend the erase or program operation when reading data
  from the other bank. Please use BGO function.

BLOCK ERASE FLOW CHART

START

WRITE 20H

WRITE D0H
BLOCK ADDRESS

STATUS REGISTER
READ

SR.7 = 1 ?   — NO →   WRITE B0H ?   — NO

YES

FULL STATUS CHECK
IF DESIRED

BLOCK ERASE
COMPLETED

YES

SUSPEND LOOP
WRITE D0H

YES
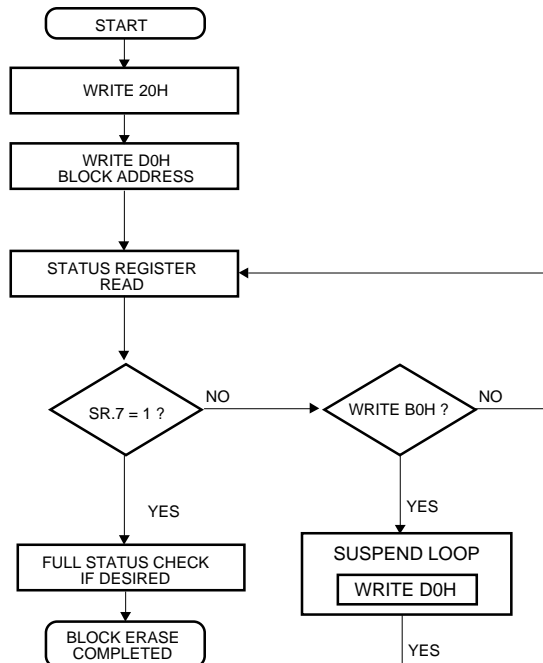
OPERATION STATUS and EFFECTIVE COMMAND

MITSUBISHI LSIs
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16,777,216-BIT (1,048,576 -WORD BY 16-BIT) CMOS
3.3V-ONLY FLASH MEMORY &
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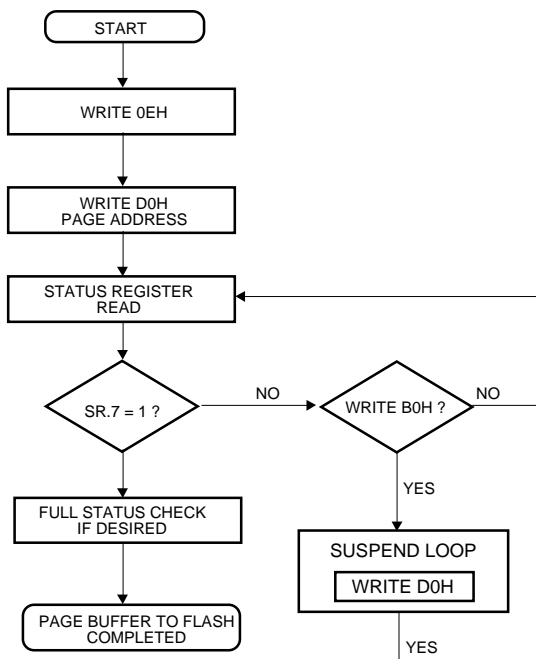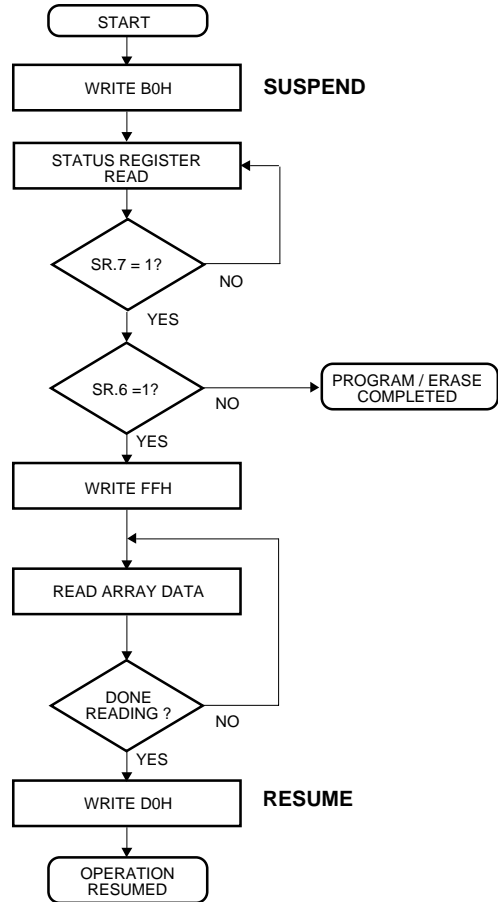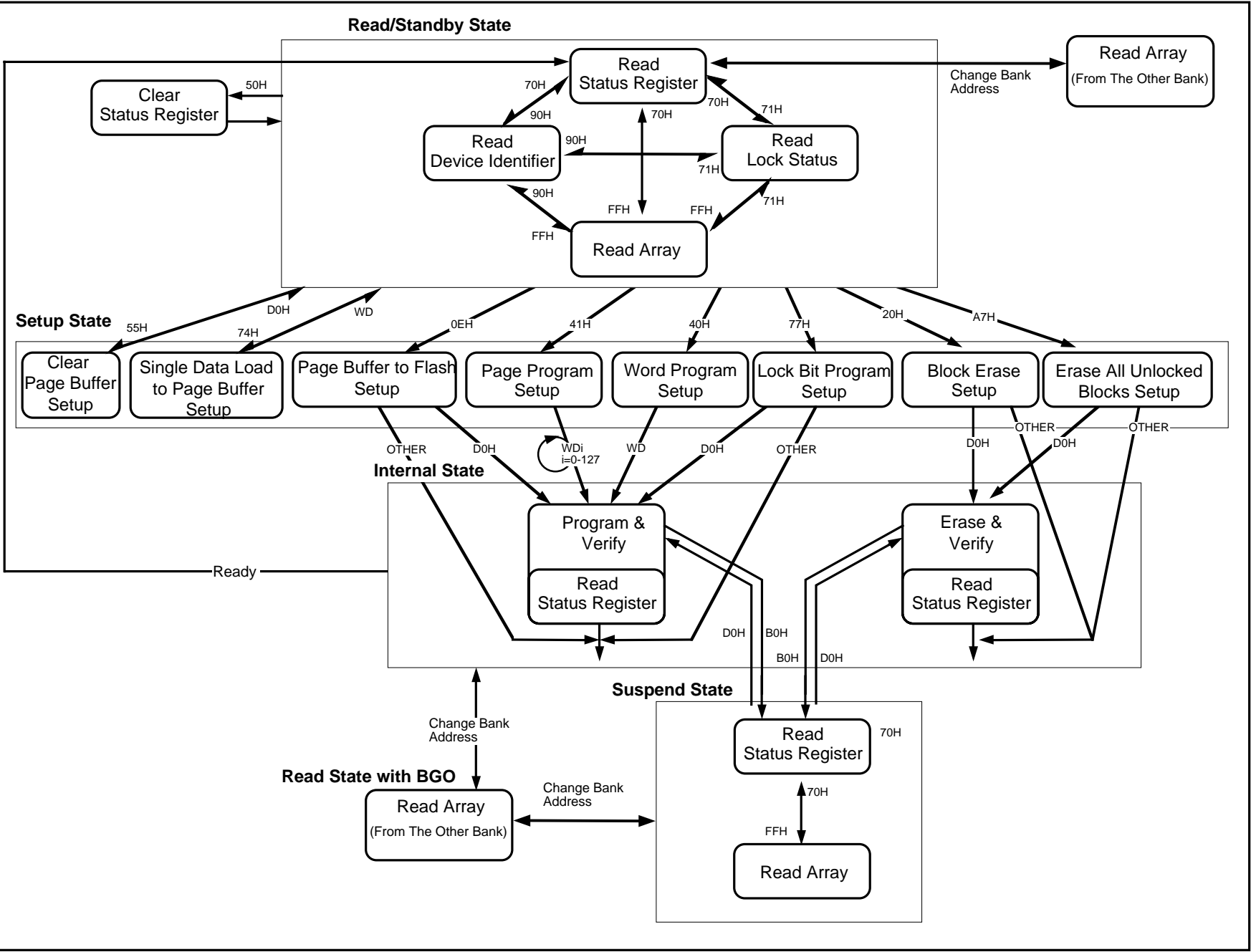Stacked-CSP (Chip Scale Package)

Read/Standby State

Clear Status Register

Read Status Register

Read Device Identifier

Read Lock Status

Read Array

Read Array (From The Other Bank)

Change Bank Address

50H

70H

90H

90H

70H

70H

71H

90H

FFH

FFH

71H

71H

FFH

Setup State

Clear Page Buffer Setup

Single Data Load to Page Buffer Setup

Page Buffer to Flash Setup

Page Program Setup

Word Program Setup

Lock Bit Program Setup

Block Erase Setup

Erase All Unlocked Blocks Setup

55H

74H

D0H

WD

0EH

41H

40H

77H

20H

A7H

OTHER

D0H

WDi i=0-127

WD

D0H

OTHER

D0H

OTHER

D0H

OTHER

Internal State

Program & Verify

Read Status Register

Erase & Verify

Read Status Register

Ready

D0H

B0H

B0H

D0H

Suspend State

Read Status Register

70H

70H

FFH

Read Array

Read State with BGO

Read Array (From The Other Bank)

Change Bank Address

Change Bank Address

Change Bank Address

MITSUBISHI LSIs
M6MGB/T166S4BWG
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3.3V-ONLY FLASH MEMORY &
4,194,304-BIT (262,144-WORD BY 16-BIT) CMOS SRAM
Stacked-CSP (Chip Scale Package)

2. SRAM

The SRAM of M6MGB/T166S4BWG is organized as 262,144-word by 16-bit. These devices operate on a single +2.7~3.6V powersupply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs , S-LB#,S-UB#,S-CE1#,S-CE2, S-WE# and S-OE#. Each mode is summarized in the function table.

A write operation is executed whenever the low level S-WE# overlaps with the low level S-LB# and/or S-UB# and the low level S-CE1#the high level S-CE2. The address A0~A16,SA-17 must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting S-WE# at a high level and S-OE# at a low level while S-LB# and/or S-UB# and S-CE1# and S-CE2 are in an active state(S-CE1#=L,S-CE2=H).

When setting S-LB# at the high level and other pins are in an active stage, upper-byte are in selectable mode in which both reading and writing are enabled, and lower-byte are in non-selectable mode. And when setting S-UB# at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

When setting S-LB# and S-UB# at a high level or S-CE1# at high level or S-CE2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by S-LB#,S-UB# and S-CE1#,S-CE2.

The power supply current is reduced as low as 0.3μA(25°C,typical), and the memory data can be held at +2V powersupply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S-CE1#	S-CE2	S-LB#	S-UB#	S-WE#	S-OE#	Mode	DQ0~7	DQ8~15	Icc
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	———	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	———	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	———	High-Z	High-Z	Active

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
S-V_{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V_I	Input voltage	With respect to GND	-0.5* ~ (S-Vcc) + 0.5	
V_O	Output voltage	With respect to GND	0 ~ S-Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	I-version	- 40 ~ +85°C	°C
T_{stg}	Storage temperature		- 65 ~ +150°C	°C

* -3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS

(S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-level input voltage			2.2		(S-Vcc)+0.3V	V
V_{IL}	Low-level input voltage			-0.3 *		0.6	
V_{OH1}	High-level output voltage 1	I_{OH}= -0.5mA		2.4			
V_{OH2}	High-level output voltage 2	I_{OH}= -0.05mA		(S-Vcc)-0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	
I_I	Input leakage current	V_I =0 ~ S-Vcc				+1 -	µA
I_O	Output leakage current	S-LB# and S-UB#=VIH or S-CE1#=VIH or S-CE2=VIH or S-OE#=VIH, VI/O=0 ~ S-Vcc				+1 -	
I_{cc1}	Active supply current (AC,MOS level)	S-LB# and S-UB#≦ 0.2V,S-CE1# ≦ 0.2V, S-CE2 ≧ (S-Vcc)-0.2V other inputs ≦ 0.2V or ≧ (S-Vcc)-0.2V Output-open(duty 100%)	f= 10MHz	-	50	70	mA
			f= 1MHz	-	7	15	
I_{cc2}	Active supply current (AC,TTL level)	S-LB# and S-UB#=VIL,S-CE1#=VIL, S-CE2=VIH other inputs=VIH or VIL Output-open(duty 100%)	f= 10MHz	-	50	70	
			f= 1MHz	-	7	15	
I_{cc3}	Stand by supply current (AC,MOS level)	S-CE2 ≦ 0.2V Other inputs=0~S-Vcc	+70 ~ +85 °C	-	-	40	µA
			+40 ~ +70 °C	-	-	20	
			+25 ~ +40 °C	-	1	3.6	
			- 40 ~ +25 °C	-	0.3	1.2	
I_{cc4}	Stand by supply current (AC,TTL level)	1)S-CE2=VIL,Other inputs=0 - S-Vcc 2)S-CE1#=VIH, S-CE2=VIH or VIL,Other inputs=0 - S-Vcc 3)S-LB# and S-UB#=VIH , S-CE1#=VIH or VIL S-CE2=VIH or VIL, Other inputs=0 - S-Vcc		-	-	1.0	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

Note 2: Typical value is for S-Vcc=3.0V and Ta=25°C

* -3.0V in case of AC (Pulse width≦ 30ns)

CAPACITANCE

(S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			10	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	

Note: The value of common pins to SRAM is the sum of Flash Memory and SRAM.

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AC ELECTRICAL CHARACTERISTICS

(S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	2.7V~3.6V
Input pulse	V_{IH}=2.4V, V_{IL}=0.4V
Input rise time and fall time	5ns
Reference level	V_{OH}=V_{OL}=1.5V Transition is measured $\pm$ 500mV from steady state voltage.(for t_{en},t_{dis})
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)

Fig.1 Output load

Including scope and jig capacitance
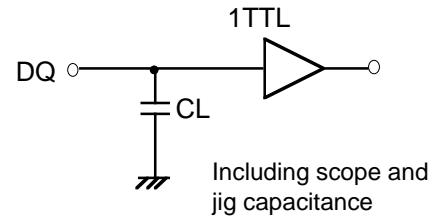
(2) READ CYCLE

Symbol	Parameter	Limits SRAM Min	Max	Units
t_{CR}	Read cycle time	85		ns
t_a(A)	Address access time		85	ns
t_a(CE1)	Chip select 1 access time		85	ns
t_a(CE2)	Chip select 2 access time		85	ns
t_a(LB)	Lower Byte control access time		85	ns
t_a(UB)	Upper Byte control access time		85	ns
t_a(OE)	Output enable access time		45	ns
t_{dis}(CE1)	Output disable time after S-CE1# high		30	ns
t_{dis}(CE2)	Output disable time after S-CE2 low		30	ns
t_{dis}(LB)	Output disable time after S-LB# high		30	ns
t_{dis}(UB)	Output disable time after S-UB# high		30	ns
t_{dis}(OE)	Output disable time after S-OE high		30	ns
t_{en}(CE1)	Output enable time after S-CE1# low	10		ns
t_{en}(CE2)	Output enable time after S-CE2 high	10		ns
t_{dis}(LB)	Output enable time after S-LB# low	10		ns
t_{dis}(UB)	Output enable time after S-UB# low	10		ns
t_{en}(OE)	Output enable time after S-OE low	5		ns
t_V(A)	Data valid time after address	10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits SRAM Min	Max	Units
t_{CW}	Write cycle time	85		ns
t_w(W)	Write pulse width	50		ns
t_{su}(A)	Address setup time	0		ns
t_{su}(A-WH)	Address setup time with respect to S-WE#	70		ns
t_{su}(LB)	Lower Byte control setup time	70		ns
t_{su}(UB)	Upper Byte control setup time	70		ns
t_{su}(CE1)	Chip select 1 setup time	70		ns
t_{su}(CE2)	Chip select 2 setup time	70		ns
t_{su}(D)	Data setup time	35		ns
t_h(D)	Data hold time	0		ns
t_{rec}(W)	Write recovery time	0		ns
t_{dis}(W)	Output disable time from S-WE# low		30	ns
t_{dis}(OE)	Output disable time from S-OE# high		30	ns
t_{en}(W)	Output enable time from S-WE# high	5		ns
t_{en}(OE)	Output enable time from S-OE# low	5		ns

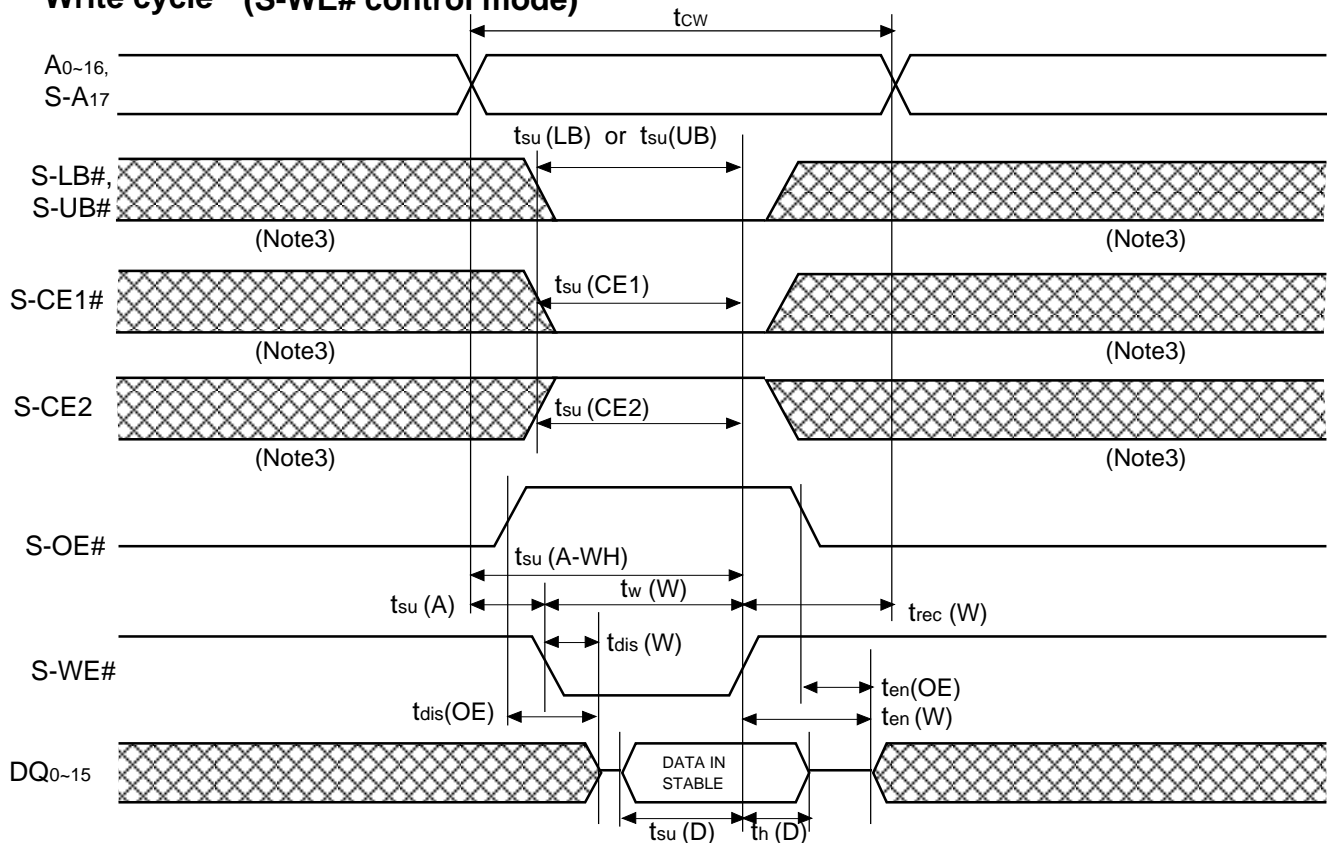MITSUBISHI LSIs
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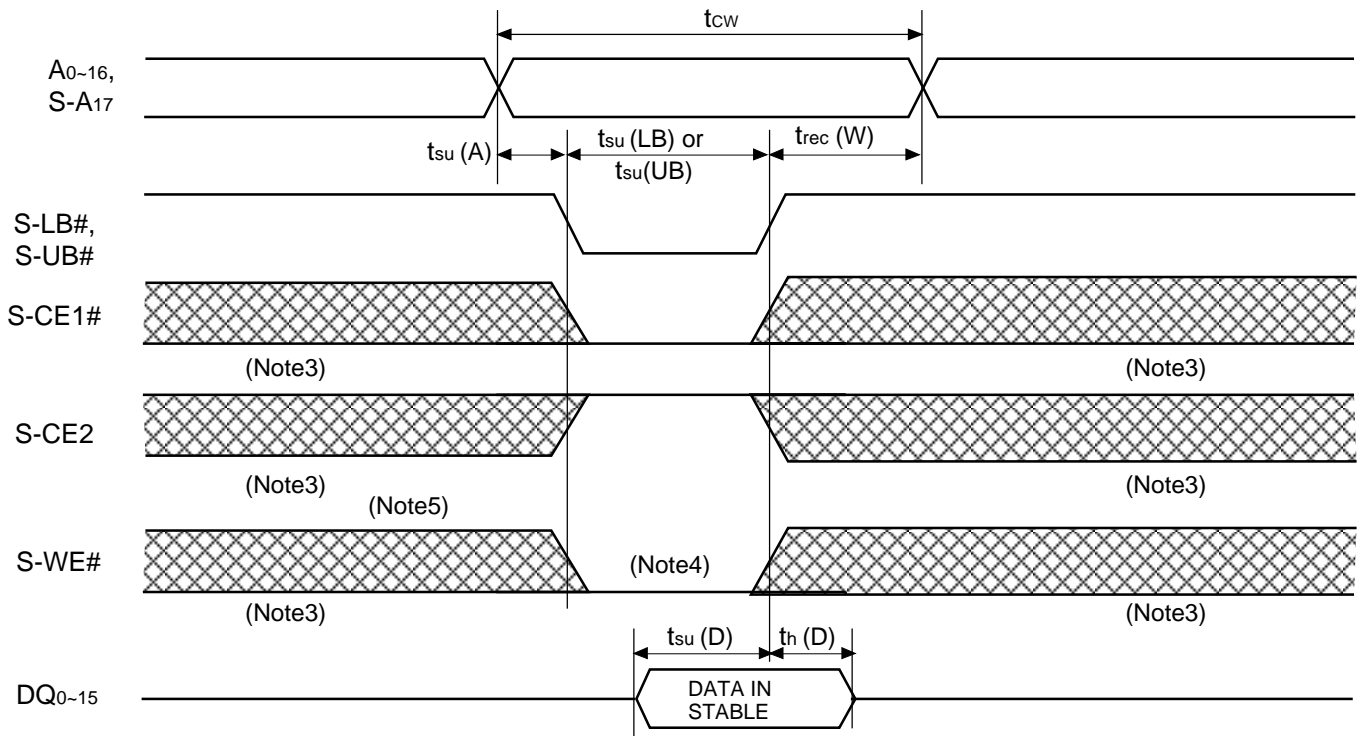Stacked-CSP (Chip Scale Package)

(4)TIMING DIAGRAMS
Read cycle

S-WE# = "H" level
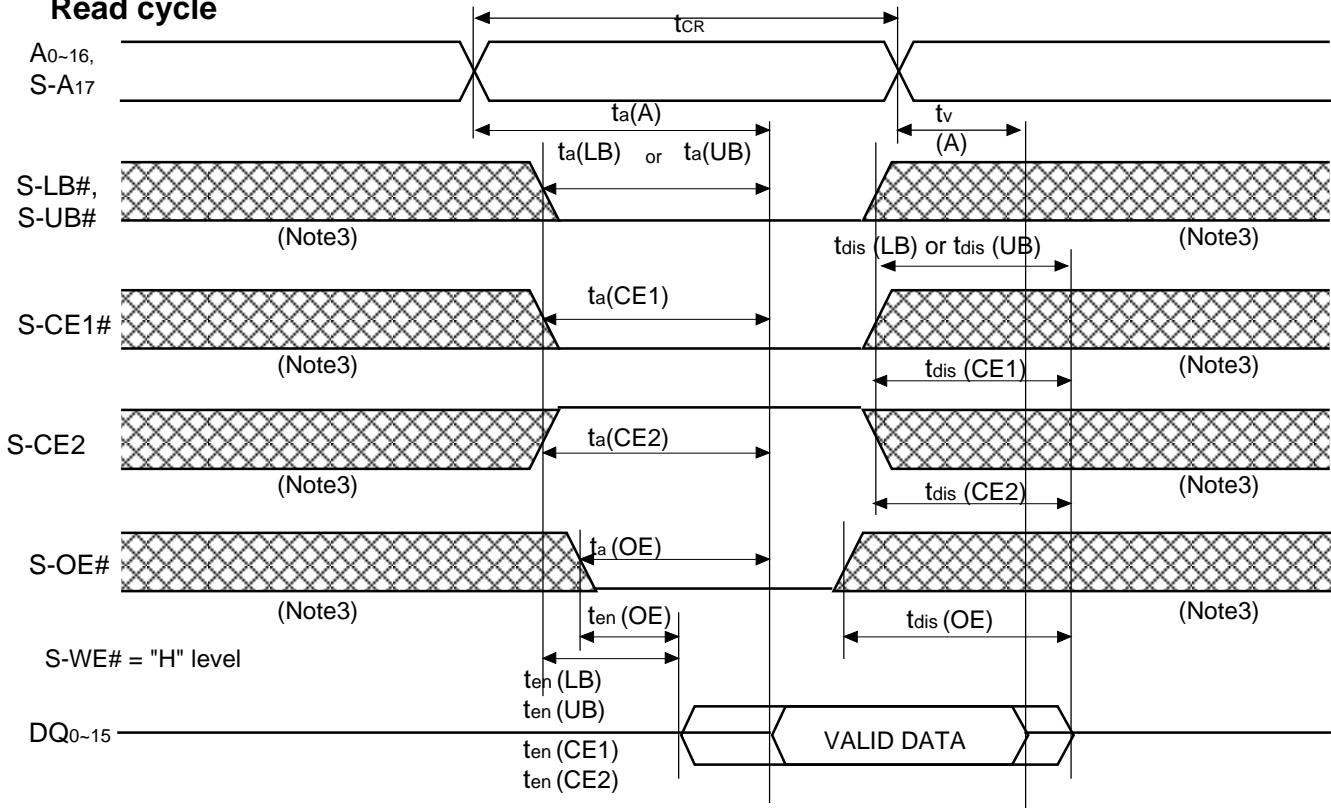
Write cycle (S-WE# control mode)

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Write cycle (S-LB#,S-UB# control mode)

Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during S-CE1# low, S-CE2 high overlaps S-LB# and/or S-UB# low and W low.

Note 5: When the falling edge of S-WE# is simultaneously or prior to the falling edge of S-LB# and/or S-UB# or the falling edge of S-CE1# or rising edge of S-CE2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.
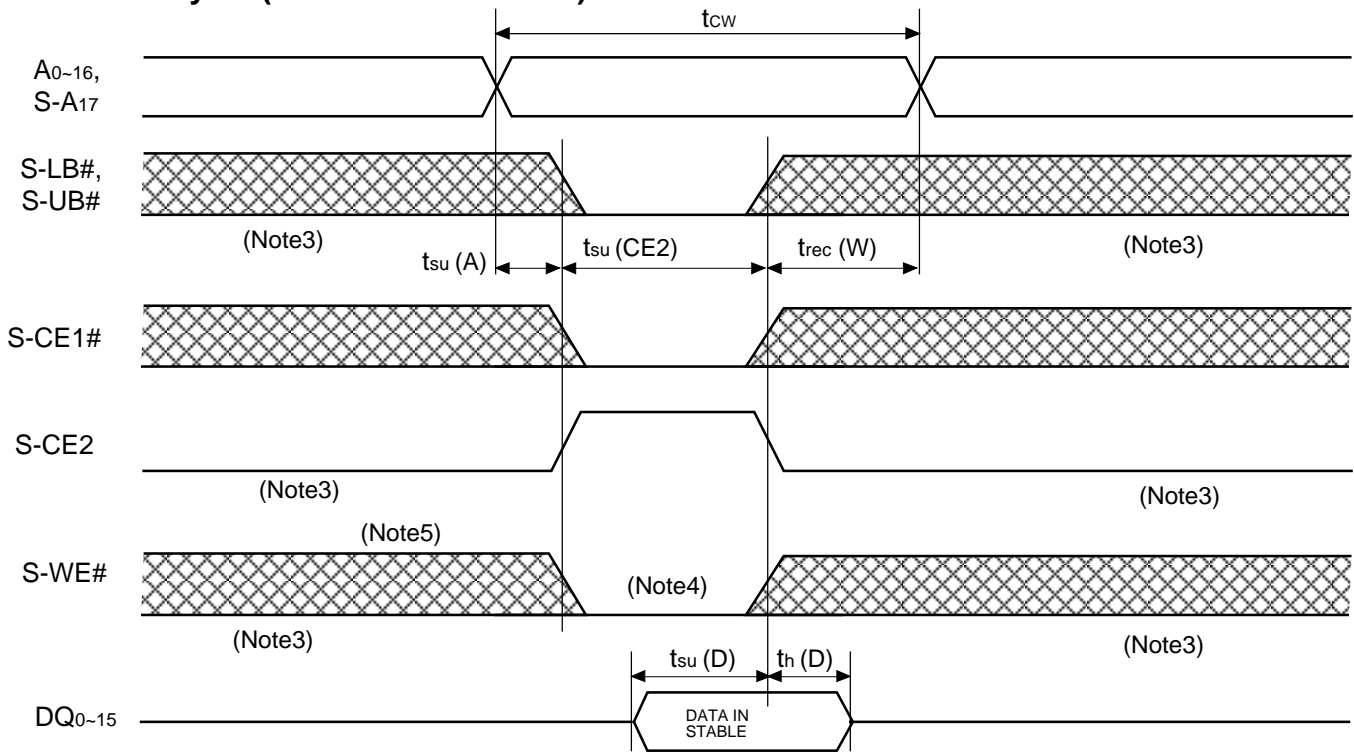
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Write cycle (S-CE1# control mode)
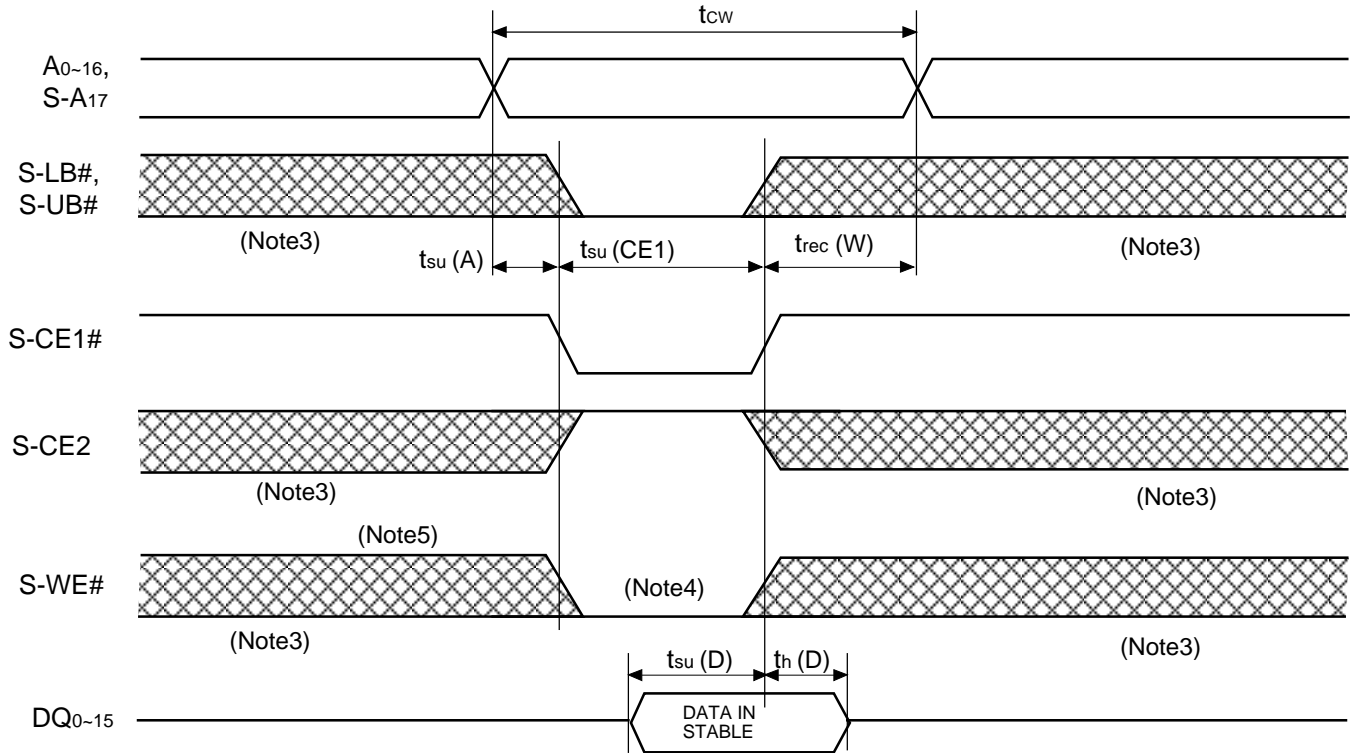
Write cycle (S-CE2 control mode)

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits			Units
				Min	Typ	Max	
S-Vcc (PD)	Power down supply voltage			2.0			V
VI (S-BC)	Byte control input S-LB#,S-UB#			2.0			V
VI (S-CE1#)	Chip select input S-CE1#			2.0			V
VI (S-CE2)	Chip select input S-CE2					0.2	V
Icc (PD)	Power down supply current	S-Vcc=3.0V S-CE2≦0.2V other inputs=0~3V	-I +70 ~ +85 °C	-	-	30	μA
			+40 ~ +70 °C	-	-	15	
			+25 ~ +40 °C	-	1	3	
			- 40 ~ +25 °C	-	0.3	1	

Typical value is for Ta=25°C

(2) TIMING REQUIREMINTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
tsu (PD)	Power down set up time		0			ns
trec (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

S-LB#,S-UB# control mode
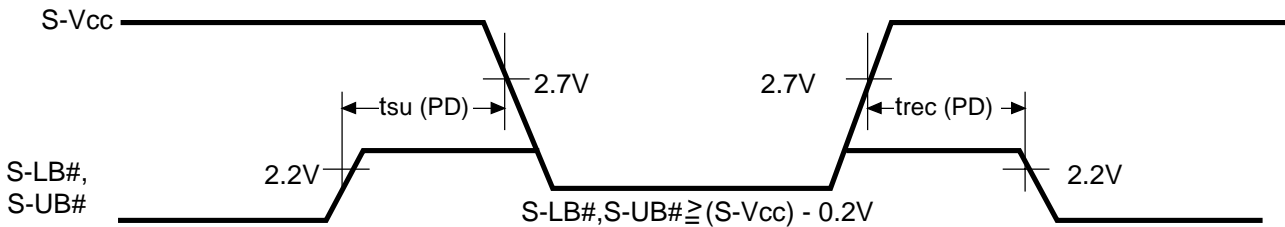
S-CE1# control mode

S-CE2 control mode