FUJITSU

MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8266A-10
MB 8266A-12
MB 8266A-15

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

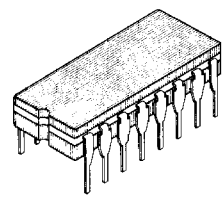
The Fujitsu MB 8266A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8266A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MB 8266A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh provides an on-chip refresh capability that is acceptable upward to 256K dynamic RAMs, as pin 1 is left no-connect. The MB 8266A also features "Nibble Mode" which allows high speed serial access to up to 4 bits of data.

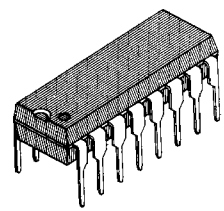
The MB 8266A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8266A-10)
  120 ns max (MB 8266A-12)
  150 ns max (MB 8266A-15)
- Cycle time,
  190 ns min (MB 8266A-10)
  230 ns min (MB 8266A-12)
  260 ns min (MB 8266A-15)
- Nibble cycle time,
  60 ns min (MB 8266A-10)
  70 ns min (MB 8266A-12)
  90 ns min (MB 8266A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8266A-10)
  248 mW max (MB 8266A-12)
  220 mW max (MB 8266A-15)
  25 mW standby (max)
- 2 ms/128 refresh cycles
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, Hidden and $\overline{\text{RAS}}$-only refresh capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows two-dimensional chip
- Read-Modify-Write capability
- On-chip latches for Addresses and Data-in
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Surfix-Z
  Standard 16-pin Plastic DIP: Surfix-P
  Standard 18-pad Ceramic LCC: Surfix-TV



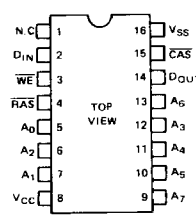
CERAMIC PACKAGE
DIP-16C-C04

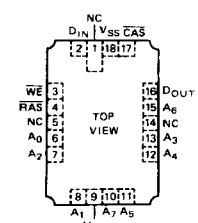


PLASTIC PACKAGE
DIP-16P-M03

LCC-18C-F02 : See Page 1-237

PIN ASSIGNMENT





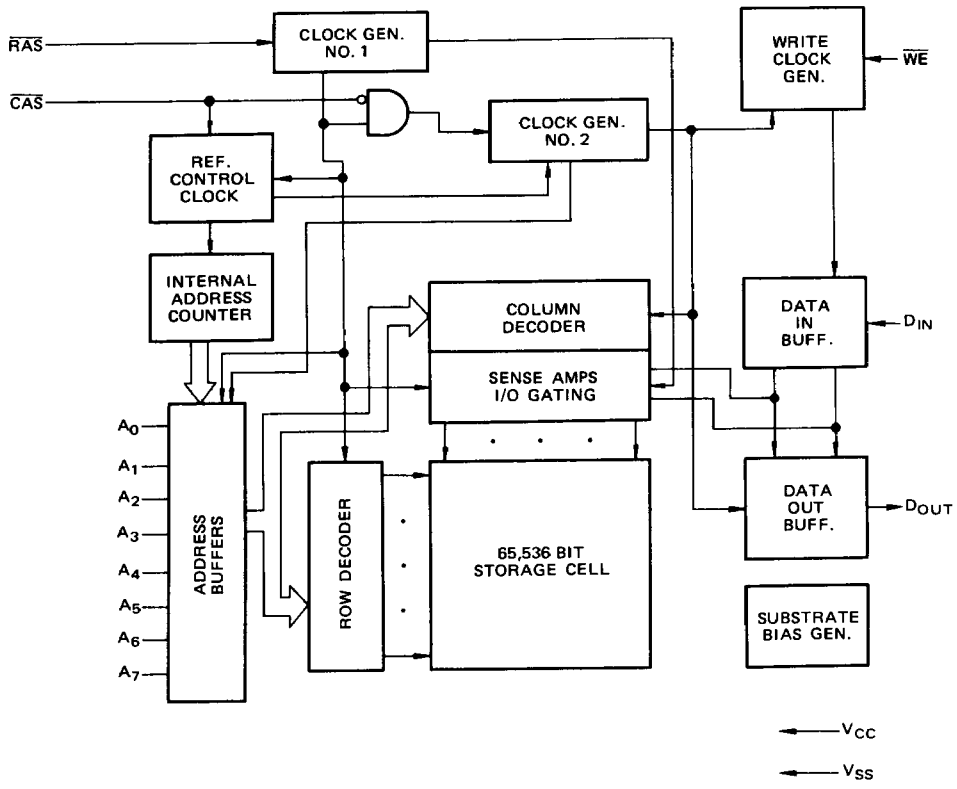
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 8266A BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$, D_{IN}	C_{IN1}		5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}*	−1.0		0.8	V	

Note * : The device can withstand undershoots to the −2V level with a pulse width of 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 8266A-10	I_{CC1}		50	mA
	MB 8266A-12			45	
	MB 8266A-15			40	
STANDBY CURRENT Standby Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 8266A-10	I_{CC3}		38	mA
	MB 8266A-12			35	
	MB 8266A-15			31	
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	MB 8266A-10	I_{CC4}		21	mA
	MB 8266A-12			21	
	MB 8266A-15			21	
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$)	MB 8266A-10	I_{CC5}		42	mA
	MB 8266A-12			38	
	MB 8266A-15			34	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0 \leqq V_{IN} \leqq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not test = 0 V)		$I_{I(L)}$	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		$I_{O(L)}$	−10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	0.4	V

Note * : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	MB 8266A-10		MB 8266A-12		MB 8266A-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2		2	ms
Random Read/Wire Cycle Time		t_{RC}	190		230		260		ns
Read-Write Cycle Time		t_{RWC}	230		265		280		ns
Access Time from $\overline{RAS}$	4, 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5, 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	30	0	35	0	40	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time		t_{CP}	40		50		60		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	40	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7, 8	t_{RCD}	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	30		30		30		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		10		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		15		20		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced To $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced To $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		0		ns
Write Command Hold Time		t_{WCH}	20		25		30		ns
Write Command Pulse Width		t_{WP}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	20		25		30		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	40		50		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	90		110		120		ns

AC CHARACTERISTICS

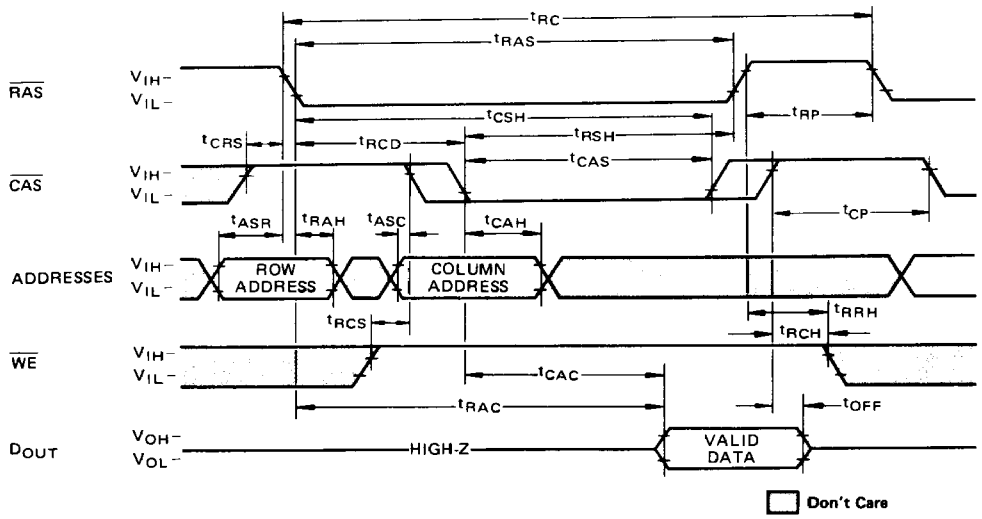
(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 8266A-10		MB 8266A-12		MB 8266A-15		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	20		25		30		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh Cycles)	t_{RPC}	20		20		20		ns
Nibble Mode Read/Write Cycle Time	t_{NC}	60		70		90		ns
Nibble Mode Read-Write Cycle Time	t_{NRWC}	75		90		120		ns
Nibble Mode Access Time	t_{NCAC}		25		30		40	ns
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCAS}	25		30		40		ns
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	25		30		40		ns
Nibble Mode Read $\overline{RAS}$ Hold Tim	t_{NRRSH}	25		30		40		ns
Nibble Mode Write $\overline{RAS}$ Hold Time	t_{NWRSH}	35		40		45		ns
Nibble Mode Write Command Set Up Tim	t_{NWCS}	0		0		0		ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	20		25		35		ns
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	15		20		30		ns
Refresh Counter Test Cycle Time 11	t_{RTC}	300		350		405		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width 11	t_{TRAS}	200		240		295		ns

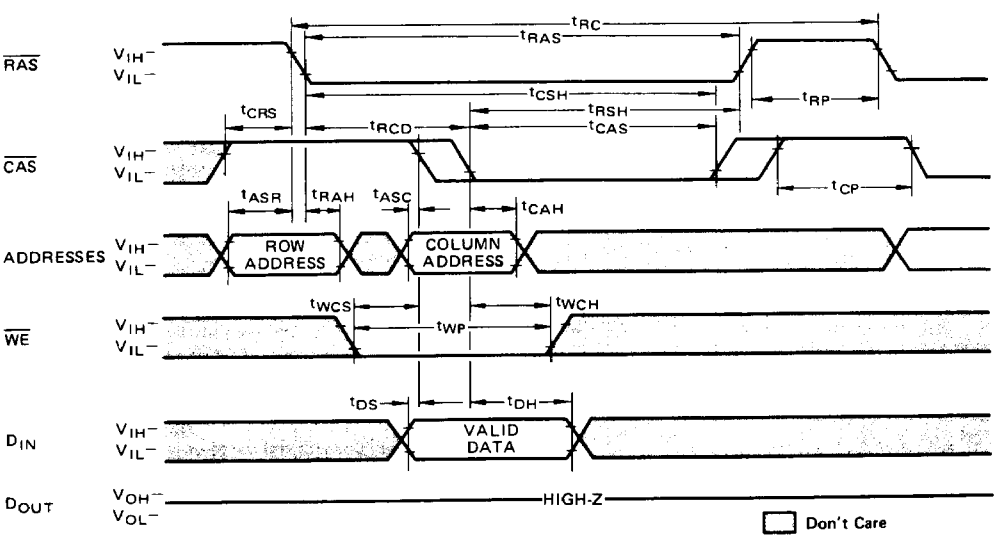
Notes:

1. An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. Refresh counter test cycle only.

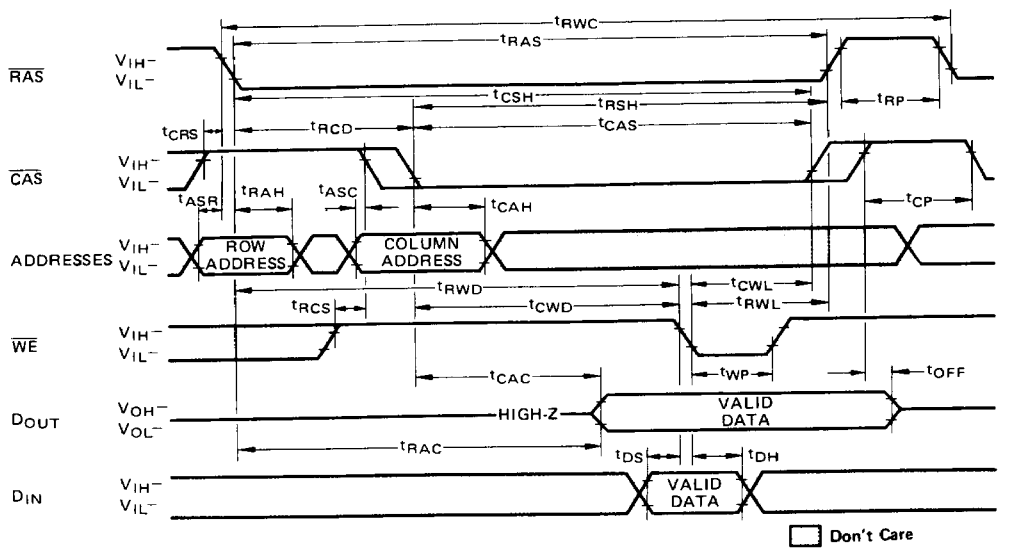
Read Cycle



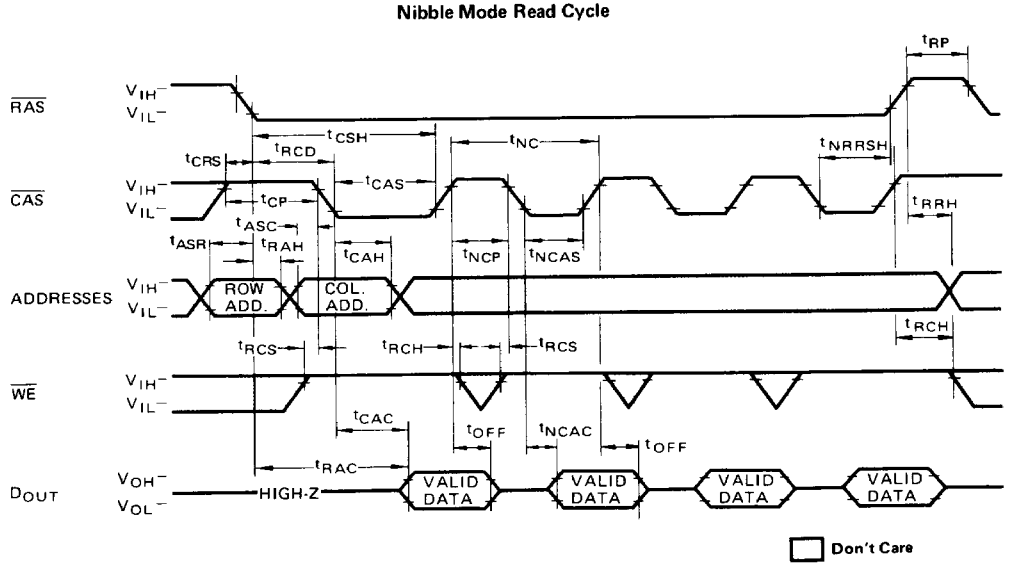
Write Cycle (Early Write)



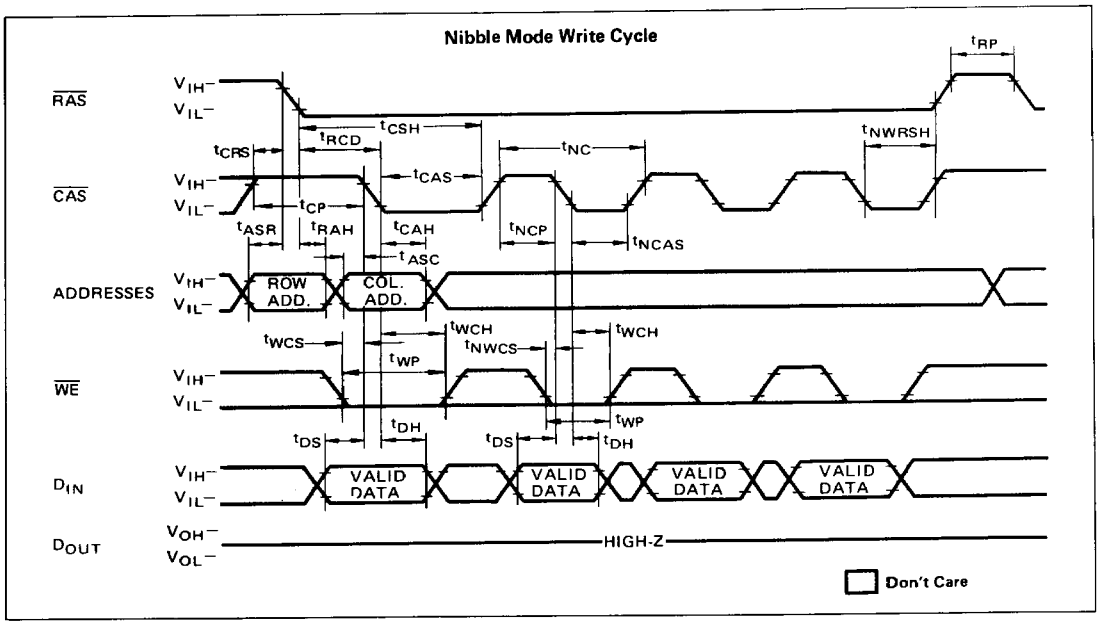
Read–Write/Read–Modify–Write Cycle



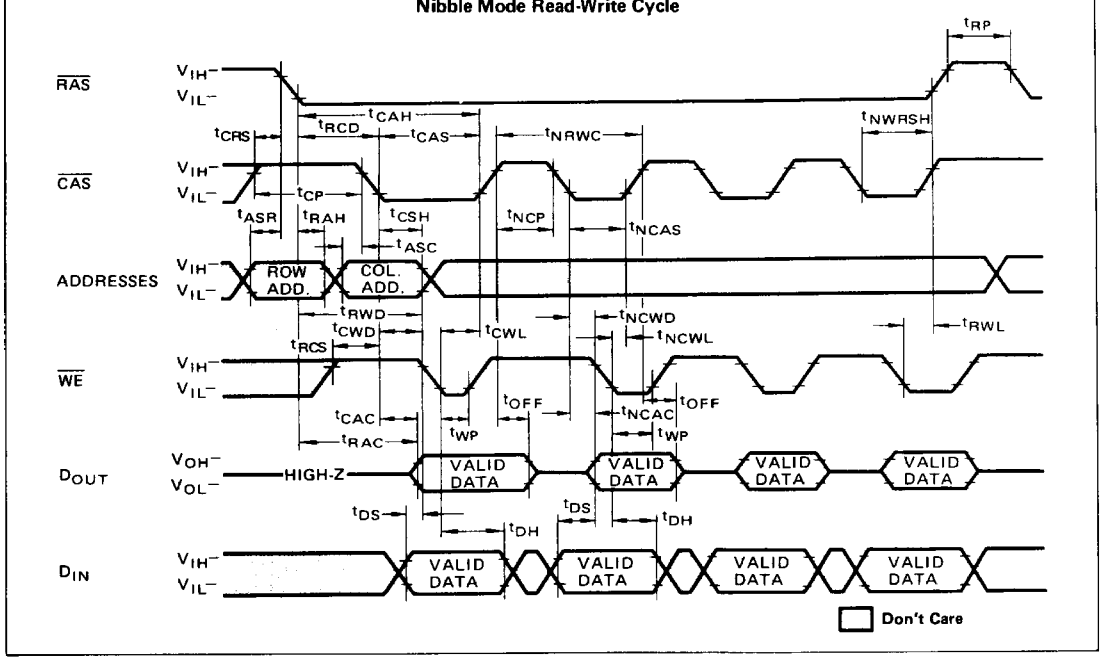
Nibble Mode Read Cycle



Nibble Mode Write Cycle

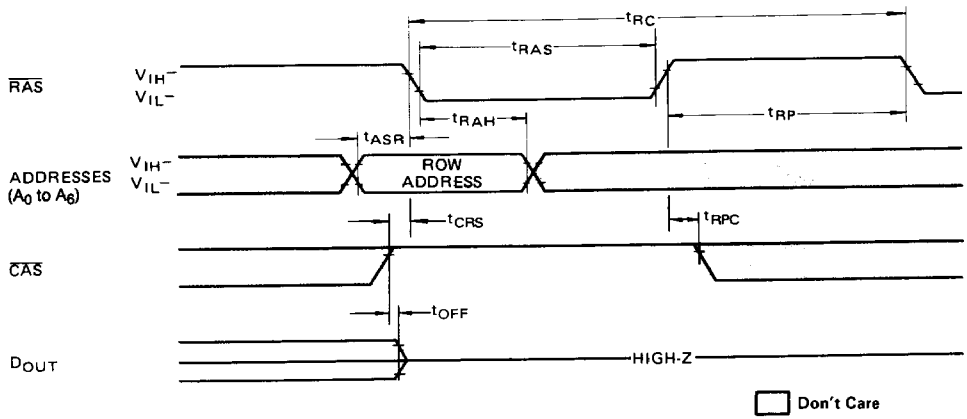


Nibble Mode Read-Write Cycle



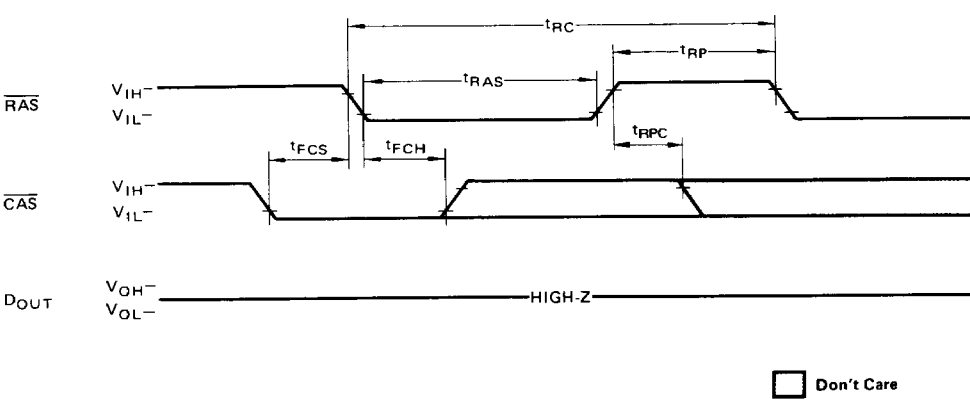
$\overline{RAS}$-only Refresh Cycle

Note: $\overline{WE}$, D_{IN} = Don't care, $A_7 = V_{IH}$ or V_{IL}

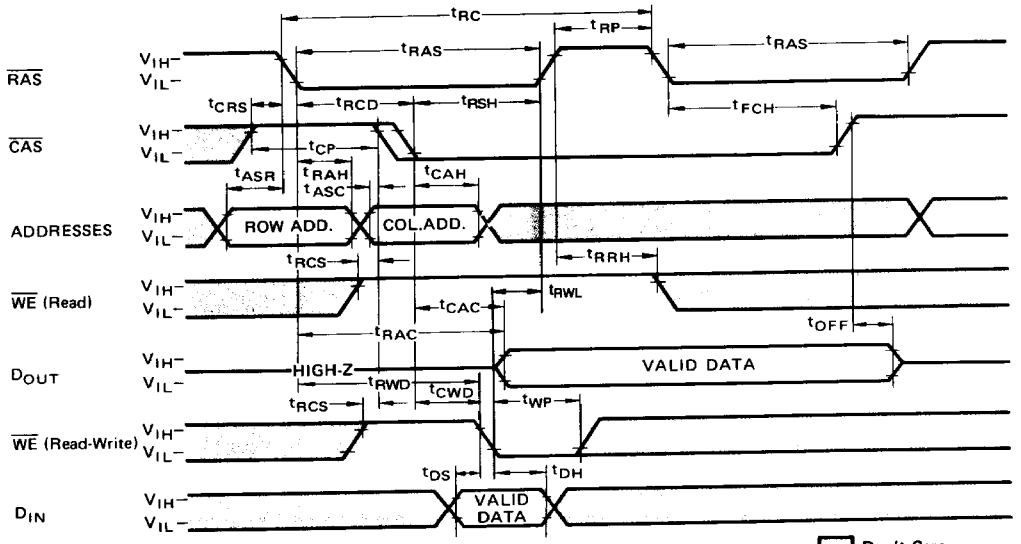


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

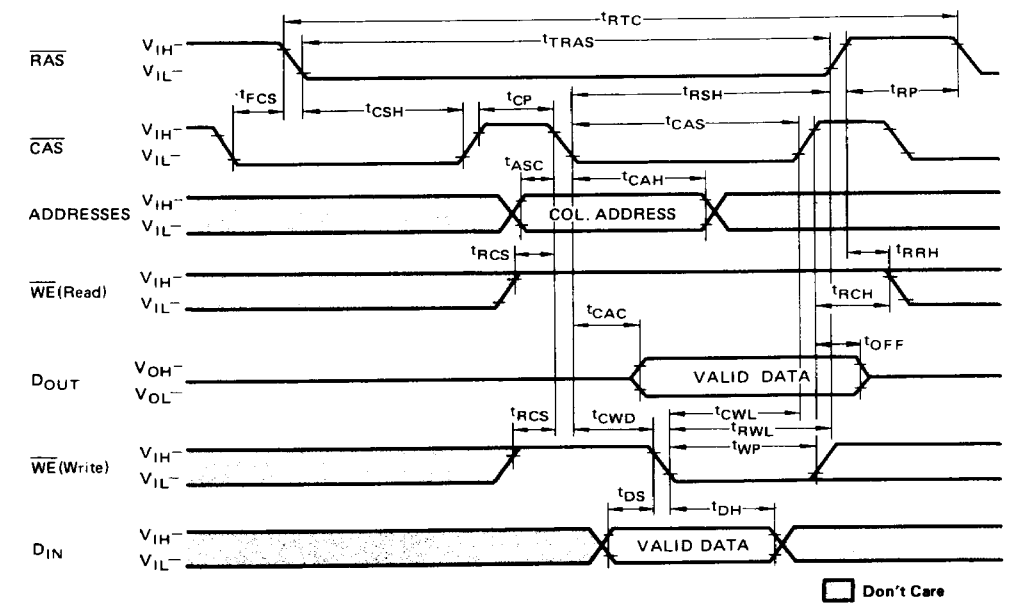
Note: Address, $\overline{WE}$, D_{IN} = Don't care



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8266A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selectes read mode and low selectes write mode. Data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 8266A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transistion occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Nibble Mode:
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 6 column addresses. The 2 bits of column addresses (A_3, A_6) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_6 and A_3 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).
If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent accesses. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location. Using Fujitsu's nibble mode along with shift registers allows some interesting application possibilities. For instance it is possible to use an MB 8266A and a 4-bit universal shift register as a 16K x 4 dynamic RAM. This approach provides 16K granularity with the density and cost savings of 64K DRAMs. Refer to the Fig. 2 for example of 16K x 4 DRAM with MB 8266A.
Another application is to use Fujitsu's MB 8266As to generate a high speed serial bit stream for video display systems. In the example shown in Fig. 3 the eight MB 8266As are operating in nibble mode with each successive byte of data loaded into its appropriate shift register. The shift registers are then unloaded serially to form a data stream with rates for this example as fast as 12ns per bit. Only 220ns are required to load the four registers. While the 32 bits are being unloaded the MB 8266As are available to the system for other functions.

Refresh:
Refresh of the dynamic memory alls is accomplished by performing a memory cycle at each of the 128 row addresses ($A_0 \sim A_6$) at least every two milliseconds. The MB 8266A offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh:
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$ only refresh cycle, either V_{IL} or V_{IH} is permitted to A_7.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh:
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 8266A offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. The $\overline{CAS}$-before-$\overline{RAS}$ refresh mode eliminates the need to provide refresh address inputs.

Hidden Refresh:
Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB 8266A, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-

before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed, can be defined as follows:

*A ROW ADDRESS – Bits A_0 through A_6 are defined by the refresh counter. The other bit A_7 is set low internally.

*A COLUMN ADDRESS – All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

SUGGESTED $\overline{CAS}$-before-$\overline{RAS}$ REFRESH COUNTER TEST PROCEDURE

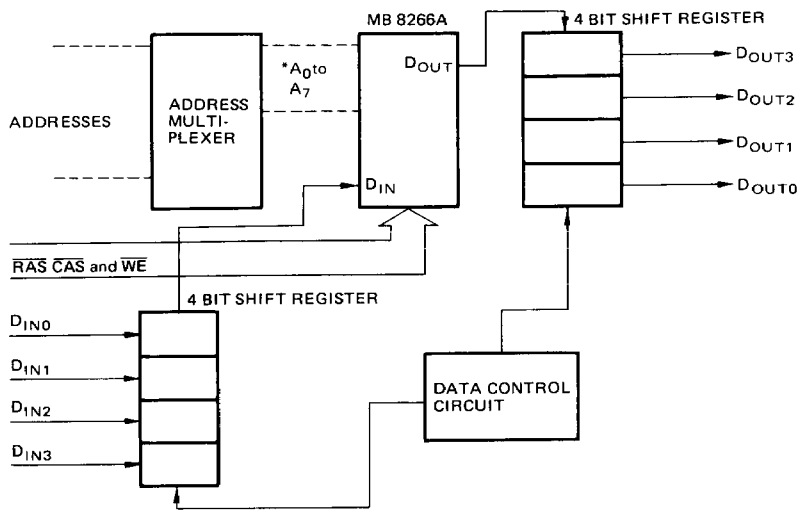
The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 128 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 128 times, and highs are written into the 128 memory cells.
(4) Read the highs written at the last operation (Step (3)).
(5) Compliment the test pattern and repeat the steps (2), (3) and (4).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

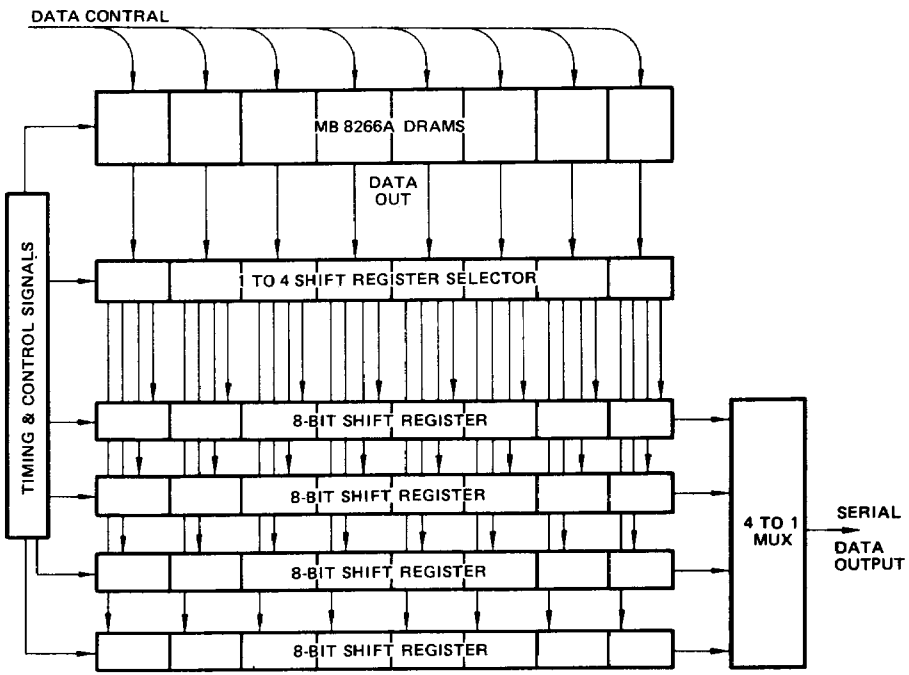
SEQUENCE	NIBBLE BIT	ROW ADDRESS	COLUMN ADDRESS			
				A_3	A_6	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	10101010	101010	1	0	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	10101010	101010	1	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	10101010	101010	0	0	
toggle $\overline{CAS}$ (nibble mode)	4	10101010	101010	0	1	
toggle $\overline{CAS}$ (nibble mode)	1	10101010	101010	1	0	sequence repeats

Fig. 2 – EXAMPLE OF 16K x 4 DRAM WITH MB 8266A



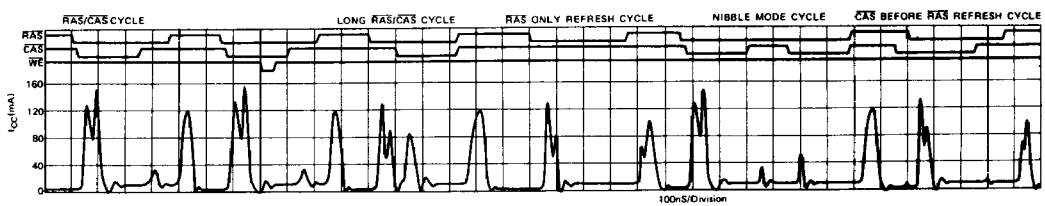
* The column address inputs for A_3 and A_6 should be Low because these addresses are used for nibble address.

Fig. 3 – VIDEO DISPLAY SYSTEM EXAMPLE



MB 8266A's operating in nibble mode provide a high speed serial output for video display system.

Fig. 4 – CURRENT WAVE FORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 5 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

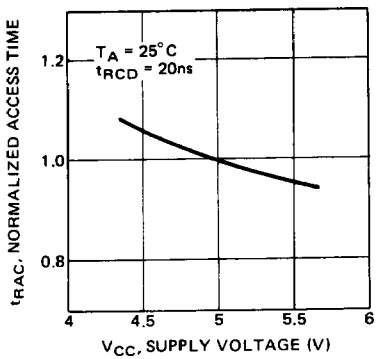


Fig. 6 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

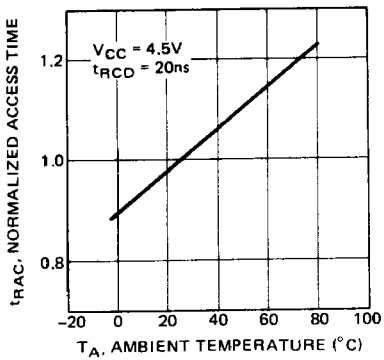


Fig. 7 – NORMALIZED NIBBLE ACCESS TIME vs SUPPLY VOLTAGE

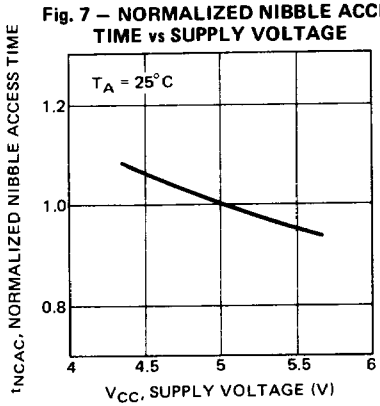


Fig. 8 – NORMALIZED NIBBLE ACCESS TIME vs AMBIENT TEMPERATURE

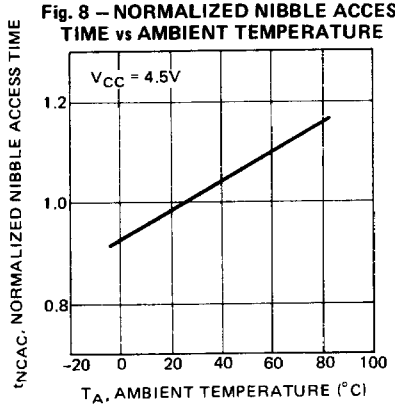


Fig. 9 – OPERATING CURRENT vs CYCLE RATE

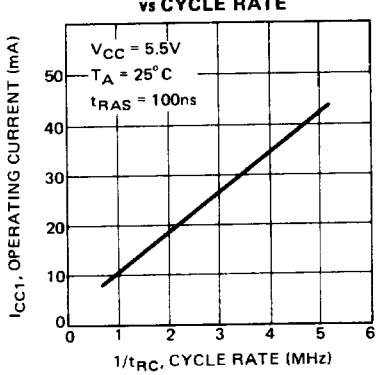


Fig. 10 – OPERATING CURRENT vs SUPPLY VOLTAGE

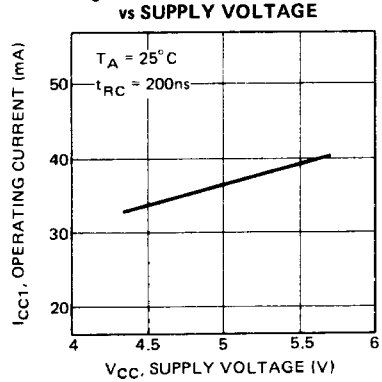


Fig. 11 – OPERATING CURRENT vs AMBIENT TEMPERATURE

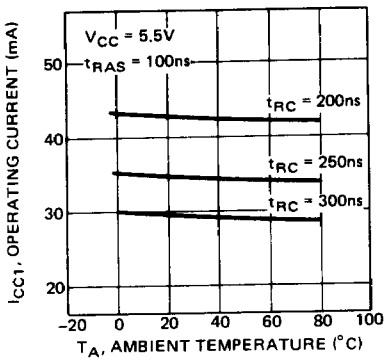


Fig. 12 – STANDBY CURRENT vs SUPPLY VOLTAGE

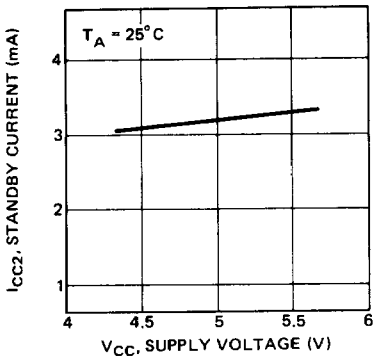


Fig. 13 – STANDBY CURRENT vs AMBIENT TEMPERATURE

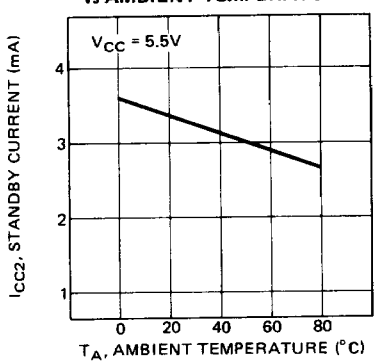


Fig. 14 – REFRESH CURRENT 1 vs CYCLE RATE

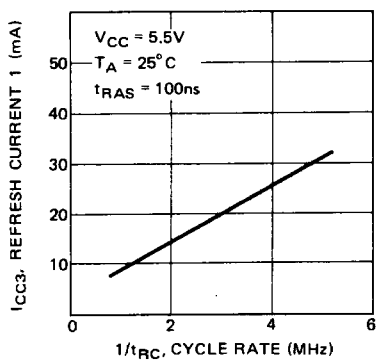


Fig. 15 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

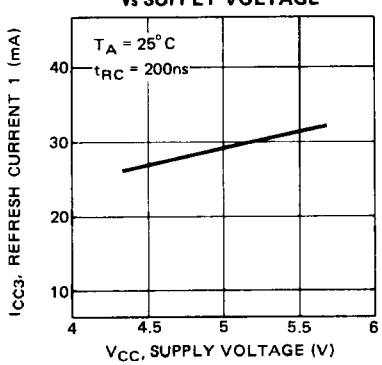


Fig. 16 – REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

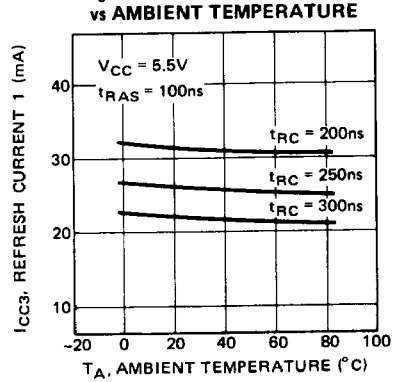


Fig. 15 – NIBBLE MODE CURRENT vs CYCLE RATE

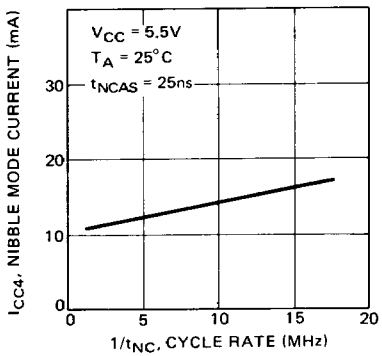


Fig. 16 – NIBBLE MODE CURRENT vs SUPPLY CURRENT

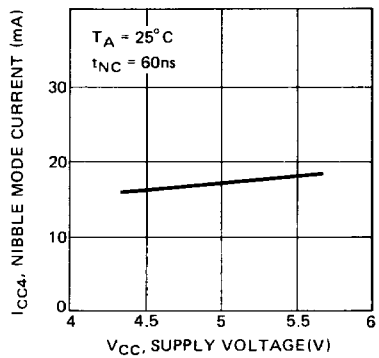


Fig. 17 – NIBBLE MODE CURRENT vs AMBIENT TEMPERATURE

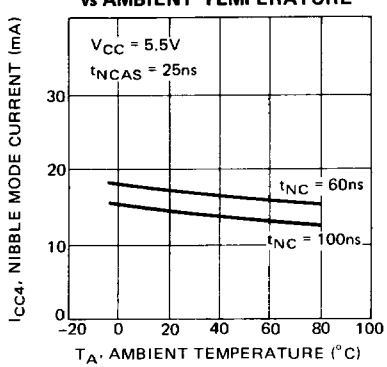


Fig. 18 – REFRESH CURRENT 2 vs CYCLE RATE

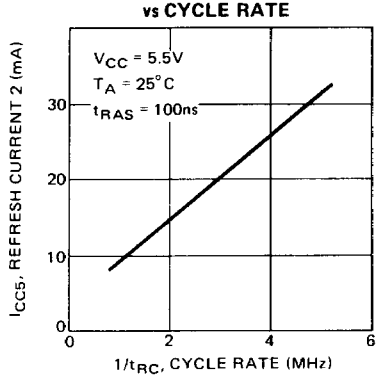


Fig. 19 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

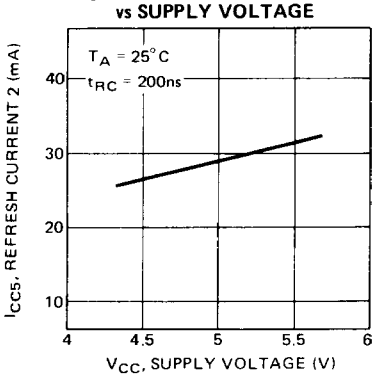


Fig. 20 – REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

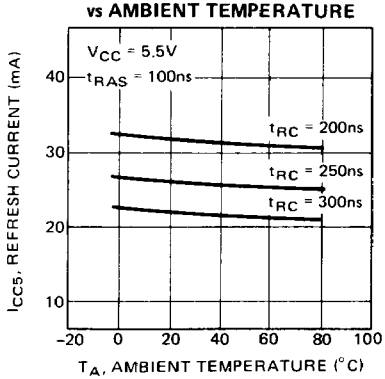


Fig. 21 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

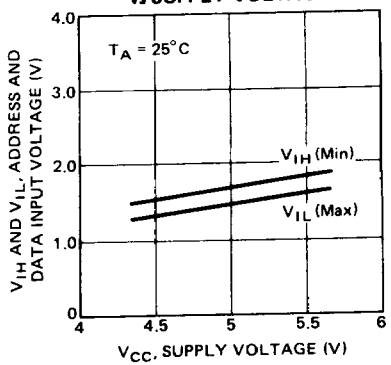


Fig. 22 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

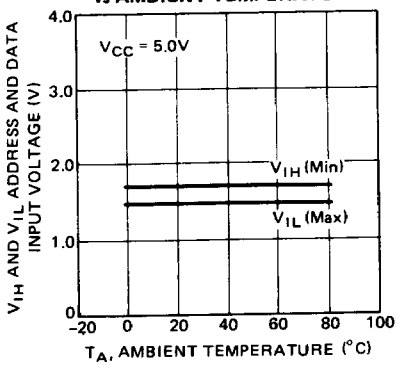


Fig. 23 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

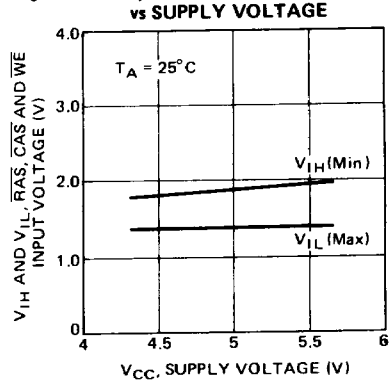


Fig. 24 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE

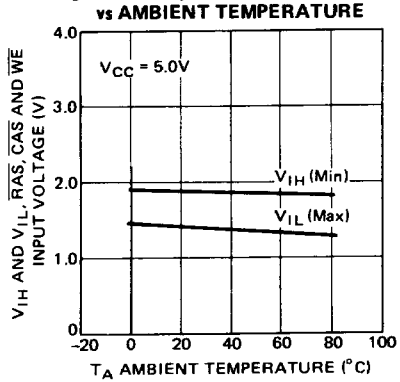


Fig. 27 – CURRENT WAVE FORM DURING POWER UP

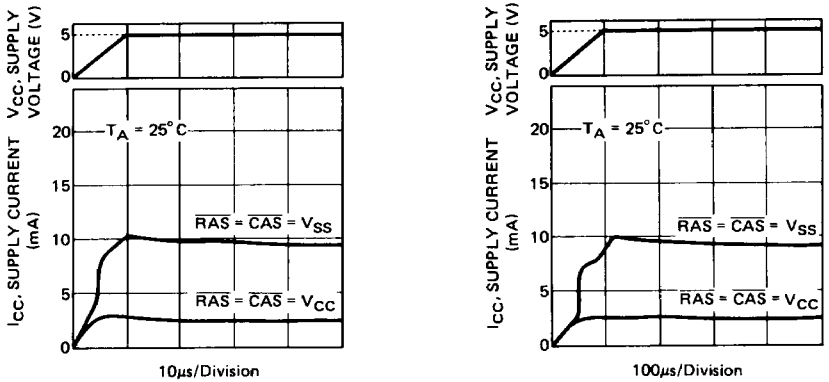


Fig. 28 – CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)

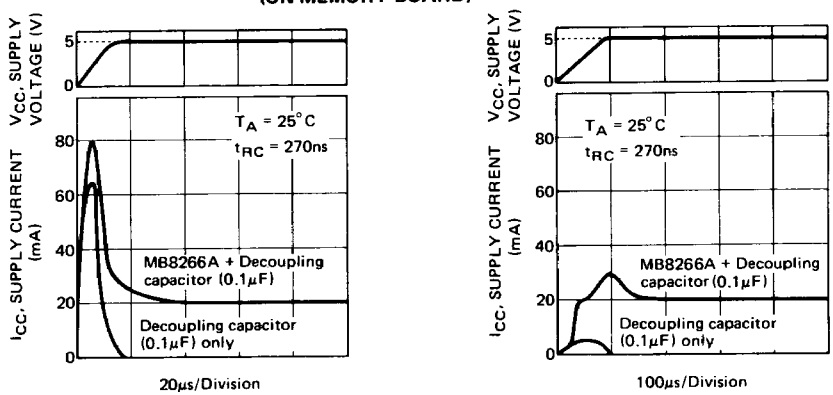
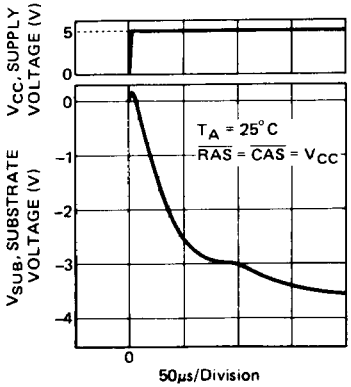
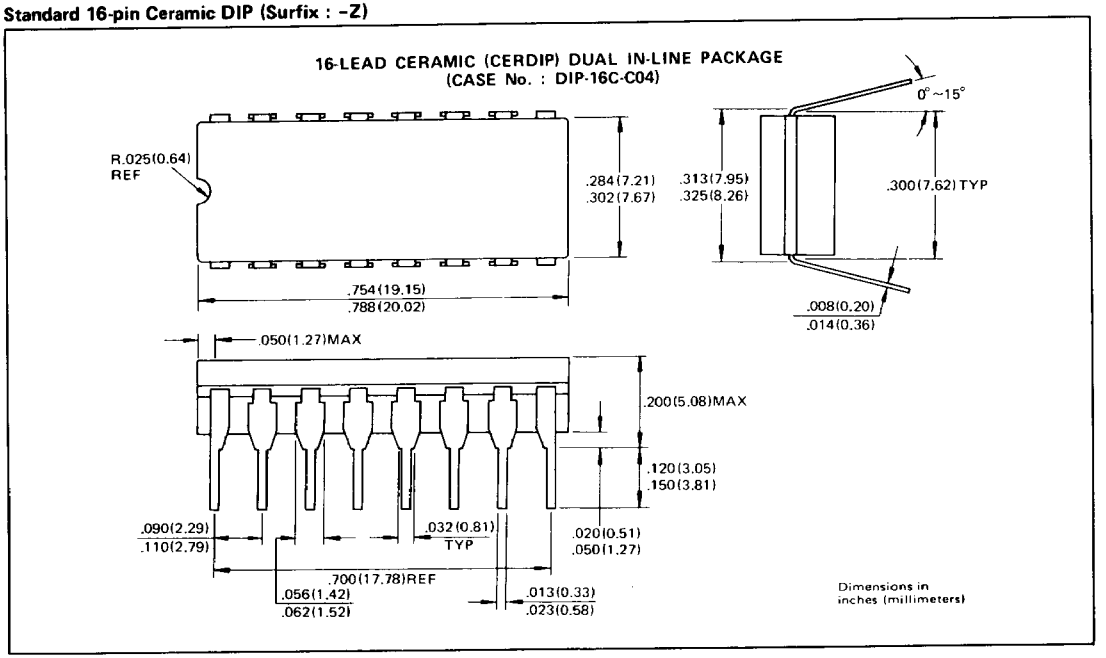


Fig. 29 – SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)

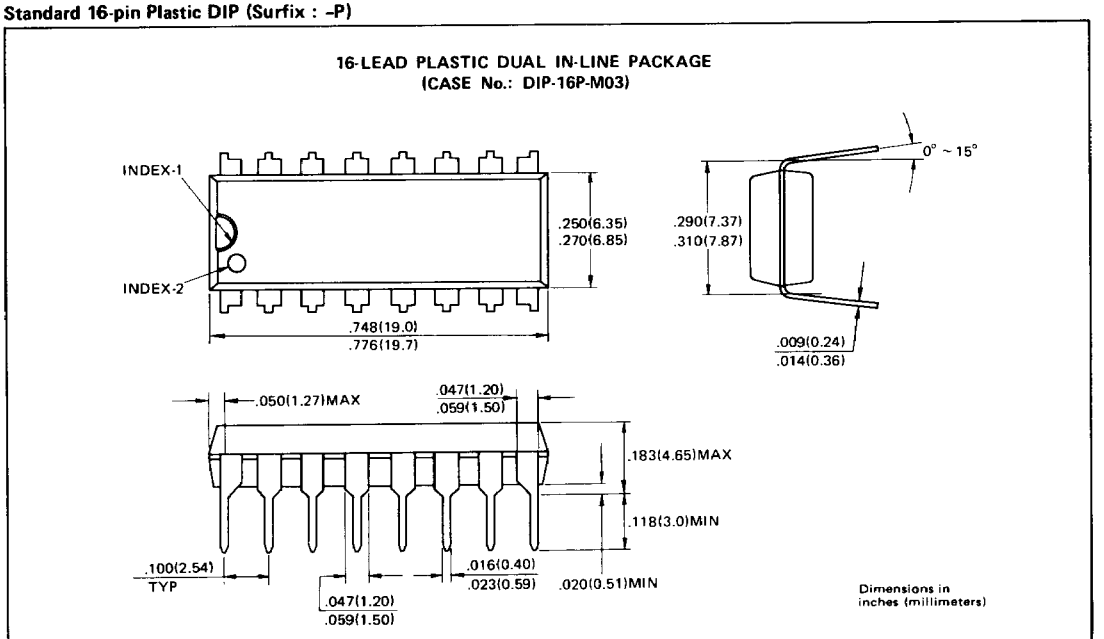


PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Surfix : -Z)

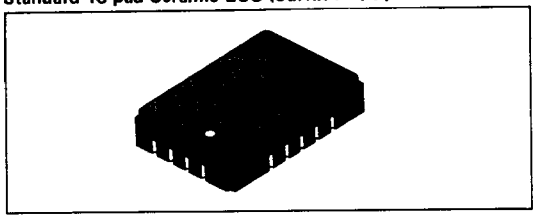


Standard 16-pin Plastic DIP (Surfix : -P)

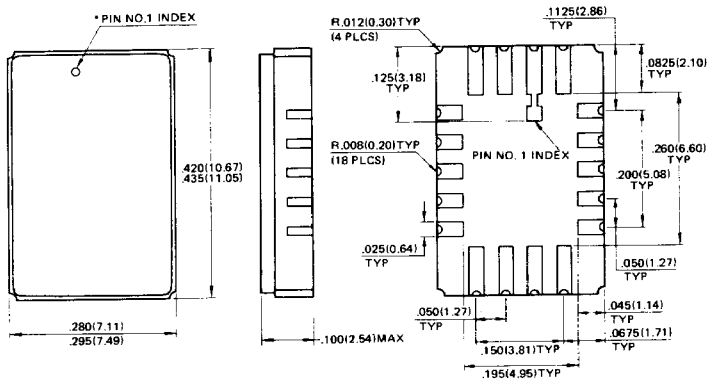


PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Surfix : -TV)



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)