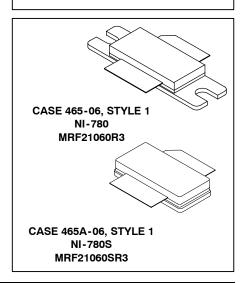
The RF MOSFET Line **RF Power Field Effect Transistors**N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2.1 to 2.2 GHz. Suitable for W-CDMA, CDMA, TDMA, GSM and multicarrier amplifier applications.

- Typical W-CDMA Performance: 2140 MHz, 28 Volts 5 MHz Offset @ 4.096 MHz BW, 15 DTCH Output Power — 6.0 Watts Power Gain — 12.5 dB Drain Efficiency — 15%
- · Internally Matched, Controlled Q, for Ease of Use
- · High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- · Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF21060R3 MRF21060SR3

2170 MHz, 60 W, 28 V LATERAL N-CHANNEL RF POWER MOSFETs



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	180 0.98	Watts W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{ heta JC}$	1.02	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

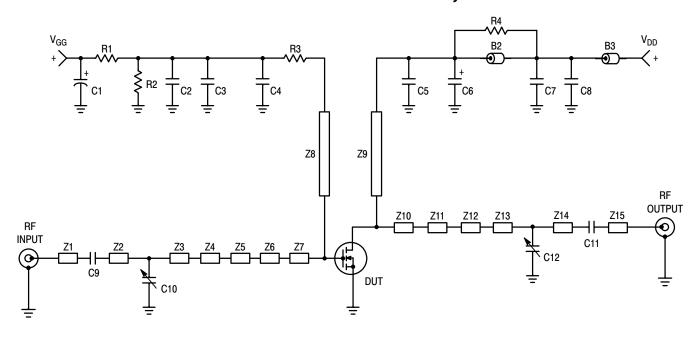




ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•			•	
Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	_	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}		_	6	μAdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}		_	1	μAdc
N CHARACTERISTICS					
Gate Threshold Voltage $(V_{DS}=10 \text{ Vdc}, I_D=300 \ \mu\text{Adc})$	V _{GS(th)}	2	_	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain-Source On-Voltage $(V_{GS} = 10 \text{ Vdc}, I_D = 2 \text{ Adc})$	V _{DS(on)}	_	0.27	_	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	9fs	_	4.7	_	S
YNAMIC CHARACTERISTICS	•		-	•	
Reverse Transfer Capacitance (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	_	2.7	_	pF
UNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	G _{ps}	11	12.5	_	dB
Two-Tone Drain Efficiency $(V_{DD}=28\ Vdc,\ P_{out}=60\ W\ PEP,\ I_{DQ}=500\ mA, f=2110\ MHz\ and\ 2170\ MHz,\ Tone\ Spacing=100\ kHz)$	η	31	34	_	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IMD	=	-30	-28	dBc
Input Return Loss $(V_{DD} = 28 \text{ Vdc}, P_{out} = 60 \text{ W PEP}, I_{DQ} = 500 \text{ mA}, f = 2110 \text{ MHz} and 2170 \text{ MHz}, Tone Spacing = 100 kHz)$	IRL	_	-12	_	dB
P _{out} , 1 dB Compression Point (V _{DD} = 28 Vdc, P _{out} = 60 W CW, f = 2170 MHz)	P1dB	_	60	_	W
Output Mismatch Stress $(V_{DD}=28\ Vdc,\ P_{out}=60\ W\ CW,\ I_{DQ}=500\ mA,\\ f=2110\ MHz,\ VSWR=10:1,\ All\ Phase\ Angles\ at\ Frequency\ of\ Tests)$	Ψ	No	Degradation Before and	In Output Po d After Test	wer

⁽¹⁾ Part is internally matched both on input and output.



B2 - B3	Ferrite Beads, Fair Rite #2743019447	Z 3	0.180" x 0.100" Microstrip
C1	10 μF, 50 V Electrolytic Chip Capacitor, Panasonic #ECEV1HV100R	Z4	0.152" x 0.293" Microstrip
C2, C7	1000 pF Chip Capacitors, ATC #100B102JCA500X	Z 5	0.216" x 0.100" Microstrip
C3, C8	0.10 μF Chip Capacitors, Kemet #CDR33BX104AKWS	Z6	0.114" x 0.410" Microstrip
C4, C5	4.7 pF Chip Capacitors, ATC #100B4R7JCA500X	Z 7	0.626" x 0.872" Microstrip
C6	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Sprague	Z8	1.050" x 0.050" Microstrip
C9, C11	9.1 pF Chip Capacitors, ATC #100B9R1JCA500X	Z 9	0.830" x 0.050" Microstrip
C10	0.8 pF - 8.0 pF Variable Capacitor, Johanson Gigatrim	Z10	0.596" x 1.040" Microstrip
C12	0.4 pF - 4.5 pF Variable Capacitor, Johanson Gigatrim	Z11	0.186" x 0.315" Microstrip
R1	1 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z12	0.097" x 0.525" Microstrip
R2	560 kΩ, 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z13	0.353" x 0.138" Microstrip
R3	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z14	0.112" x 0.080" Microstrip
R4	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z15	0.722" x 0.080" Microstrip
Z1	0.743" x 0.080" Microstrip	Board	0.030" Glass Teflon®, Arlon
Z2	0.070" x 0.100" Microstrip		GX-0300-55-22, 2 oz Cu

Figure 1. MRF21060 Test Circuit Schematic

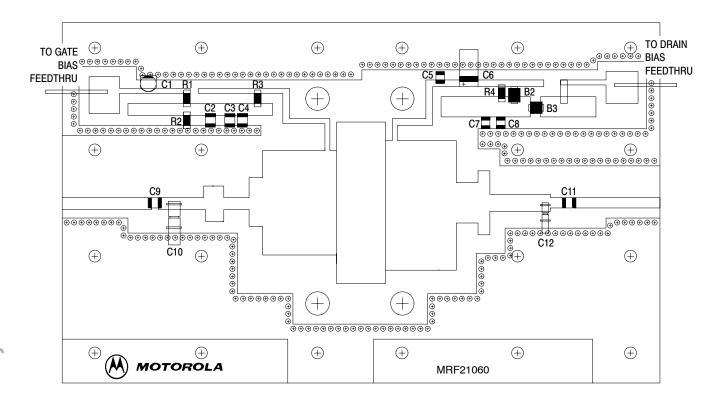
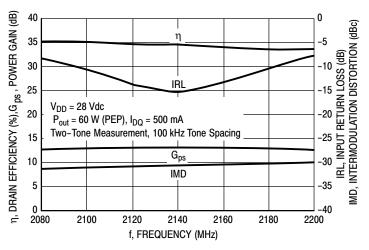


Figure 2. MRF21060 Test Circuit Component Layout

TYPICAL CHARACTERISTICS



-20 8 45 V_{DD} = 28 Vdc ps, POWER GAIN 40 I_{DQ} = 700 mA, f = 2140 MHz, Channel Spacing (Channel Bandwidth): 5 MHz @ 4.096 MHz BW 35 15 DTCH 30 (%),G 25 ACPR η, DRAIN EFFICIENCY 20 15 G_{ps} -60 8 10 12 14 16 Pout, OUTPUT POWER (WATTS Avg.) W-CDMA

Figure 3. Class AB Broadband Circuit Performance

Figure 4. W-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

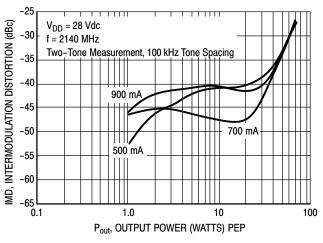


Figure 5. Intermodulation Distortion versus Output Power

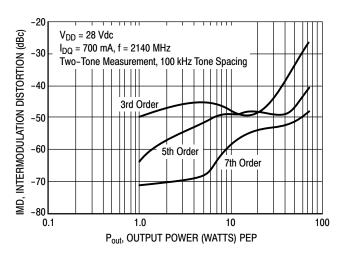


Figure 6. Intermodulation Distortion Products versus Output Power

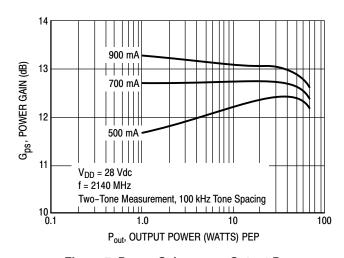


Figure 7. Power Gain versus Output Power

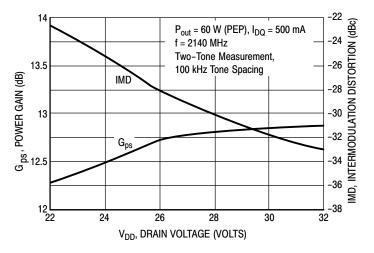
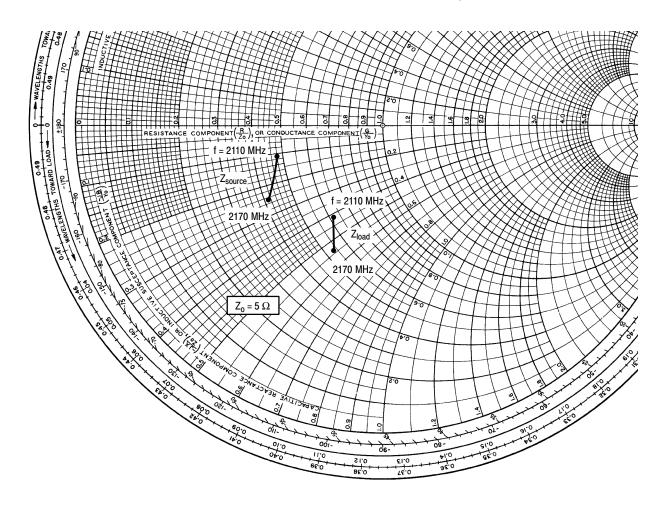


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



 V_{DD} = 28 V, I_{DQ} = 500 mA, P_{out} = 60 W PEP

f MHz	$\mathbf{Z_{source}}_{\Omega}$	$oldsymbol{Z_{load}}{\Omega}$
2110	2.40 - j0.55	3.07 - j2.05
2140	2.26 - j0.87	2.89 - j2.38
2170	2.08 - j1.23	2.66 - j2.71

Z_{source} = Test circuit impedance as measured from gate to ground.

Test circuit impedance as measured Z_{load} from drain to ground.

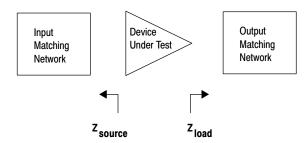
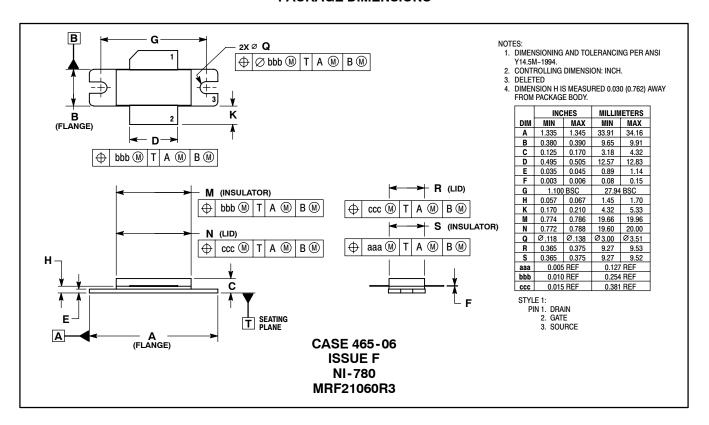
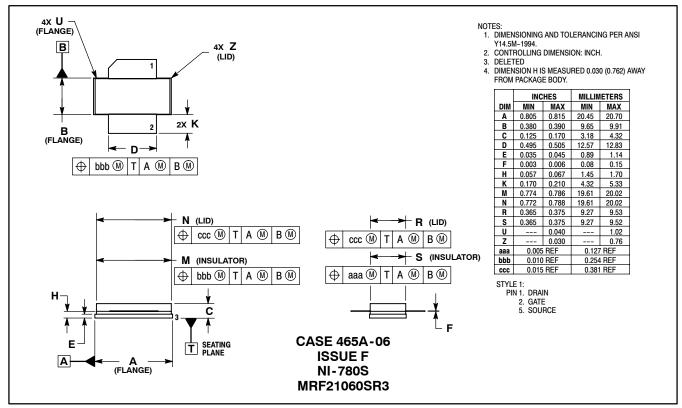


Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS





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