

TBA510

CHROMA PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA510 is a monolithic integrated circuit designed to perform the chrominance amplifier function for television receivers. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. A dc chroma gain control, which can be ganged to the receiver contrast control, is provided. Also incorporated is a variable gain automatic color control (ACC) stage, chroma blanking, burst gating, burst output stage. Two single output transistors provide burst and chroma output.

- DC CHROMA CONTROL
- PAL DELAY LINE DRIVER
- ACC AMPLIFIER
- COLOR KILLER

ABSOLUTE MAXIMUM RATINGS

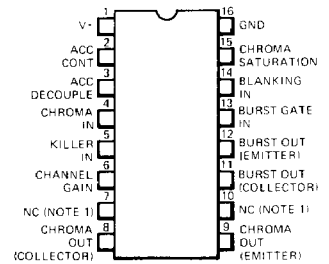
Supply Voltage	13.2 V
Internal Power Dissipation	550 mW
Current into Chroma Delay Line Driver (Collector)	20 mA
Current into Color Burst Output (Collector)	20 mA
Current out of Color Burst Output (Emitter)	20 mA
Current out of Chroma Delay Line Driver (Emitter)	20 mA
Operating Temperature Range	-20°C to +60°C
Storage Temperature Range	-55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

CONNECTION DIAGRAM

16-PIN DIP

(TOP VIEW)

PACKAGE OUTLINE 9B

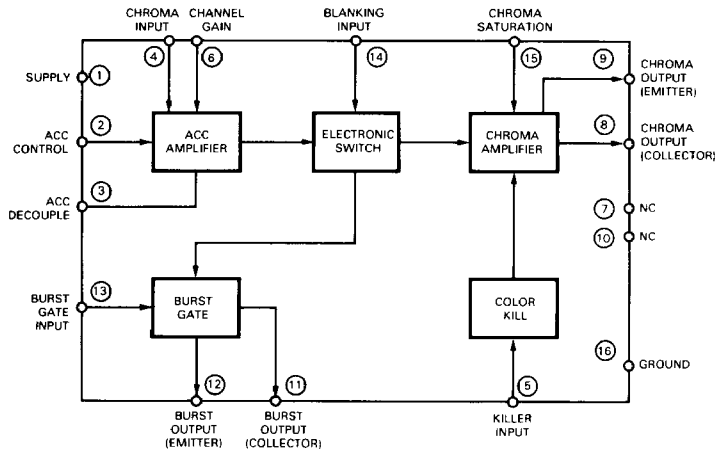


ORDER INFORMATION

TYPE	PART NO.
510	TBA510
(510Q)	(TBA510Q)†

† Not recommended for new designs.

BLOCK DIAGRAM

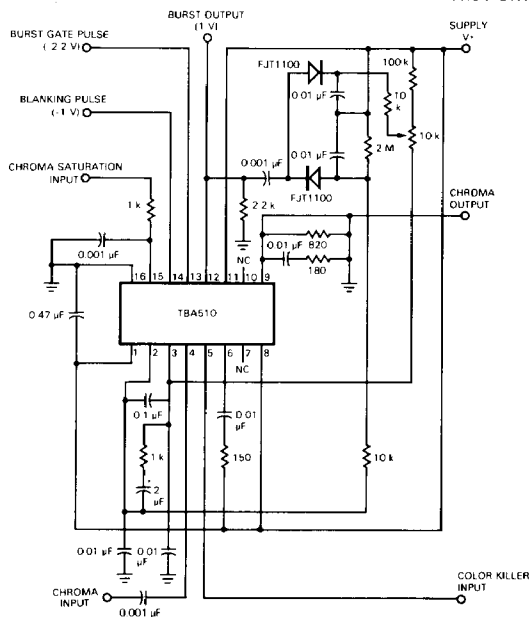


*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_+ = 12\text{V}$, See Test Circuit, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 4) Peak-to-Peak Signal at Chroma Input (V_{4p-p}) Input Impedance of Chroma Signal (Z_4)		15	150 3.0	300	mV_{p-p} $\text{k}\Omega$
Burst Output (pin 11 and 12) DC Voltage at Color Burst Output (V_{12}) Peak-to-Peak Signal at Color Burst Output (V_{12p-p}) Collector Current of Color Burst Output (I_{11})	(Note 2)		8.0 1.0 4.0		V V_{p-p} mA
Chroma Output (pin 8 and 9) DC Voltage at Chroma Output (V_9) Peak-to-Peak Signal at Chroma Output (V_{9p-p}) Range of Contrast and Saturation Control Collector Current at Chroma Output (I_8)	(Note 3)	-30	7.0 1.0 5.0	+6.0	V V_{p-p} dB mA
ACC Input (pin 2) ACC Input Voltage (V_2) for Maximum Gain (Note 4) Input Impedance of ACC Control (Z_2)		50	2.5		V $\text{k}\Omega$
Chroma Saturation Control Input (pin 15) Control Voltage Range (V_{15}) (Note 4) Input Impedance (Z_{15})		1.5 50		4.5	V $\text{k}\Omega$
Chroma Blanking Input (pin 14) Switching Level Range (V_{14}) Input Impedance (Z_{14})		-5.0	2.0	-1.0	V $\text{k}\Omega$
Burst Gate Input (pin 13) Switching Level Range (V_{13}) Input Impedance (Z_{13})		-5.0	4.0	-2.2	V $\text{k}\Omega$
Color Killer Input (pin 5) Input Voltage (V_5) for: Color on Color off Signal Suppression at Color Off Input Impedance (Z_5)		2.5 0 50 100		4.0 1.8	V V dB $\text{k}\Omega$

TEST CIRCUIT



NOTES:

1. NC — no connection (not to be used as a tie point).
2. Color burst output kept constant by ACC circuit.
3. Chroma output (emitter) at nominal saturation and maximum contrast.
4. Gain control characteristic positive.

