TUA6120 'TORNADO'

Gain controlled I/Q Mixer for digital QPSK or 8PSK Sat Signals

Wireless Components

Never stop thinking.

Edition 2004-02-05

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Target Specification V1.1
Confidential
Revision History: 2001-10-22 TUA6120 'TORNADO'

Previous Version:	V1.0 2001-07-06
Page	Subjects (major changes since last revision)
11ff	Pinning
48ff	Defaults added

Preliminary Specification Version 1.2
Confidential
Revision History: 2002-02-25 TUA6120 'TORNADO'

Previous Version:	V1.1 2001-10-22
Page	Subjects (major changes since last revision)
all	Version to preliminary
12ff	Equivalent I/O schematics and DC levels added
29	Application Circuit changed
38	Items # 1, # 10, # 11, # 12, # 13 changed
42	Item # 83 changed
43	Items # 94, # 95, # 98, # 100 changed
50, 53	Footnote added
55, 56	Band 10/11 overlap frequency changed
57	Figure 4-2 changed
58	$t_{SU.ENASDA}$ deleted

Preliminary Specification Version 1.3
Confidential
Revision History: 2002-12-20 TUA6120 'TORNADO'

Previous Version:	V1.1 2001-10-22
Page	Subjects (major changes since last revision)
diverse	Input frequency extended to 2185 MHz
38ff	# 3, # 4, # 6, # 8, # 9, # 10, # 11, # 12, # 22, # 29, # 31, # 32, # 35, # 69, # 79, # 80, # 81, # 63, # 64, # 65, # 66, # 91, # 92, # 93, # 94, # 95 changed, # 14 added
48	Bits 0 to 17, 21, 23 changed
49	Bits 0 to 9 changed, new charge pump currents
50	XTAL I/O new output levels
52	new filter bandwidths
53	ABL: New default
54	Register 80: Footnote changed

Target Specification Version 1.4
Confidential
Revision History: 2003-01-06 TUA6120 'TORNADO'

Previous Version:	V1.3 2002-12-20
Page	Subjects (major changes since last revision)
52	Register 05: Xtal output control bit added
55	VCO band switching table Band **# 9** , **# 10**: GHz-N and GHz-R divider ratio changed

Preliminary Specification Version 1.5
Confidential
Revision History: 2003-07-31 TUA6120 'TORNADO'

Previous Version:	V1.4 2003-01-06
Page	Subjects (major changes since last revision)
11	Function of pins 2, 14 and 23 changed
12	Function of pin 2 changed
15	Function of pin 14 changed
16	Function of pin 23 changed
22	Function of pins 2, 14 and 22 changed
29	Function of pins 2, 14 and 22 changed
29	pin 12, loop filter changed
36	**# 23**; Value changed
38	**# 1**, **# 3**, **# 4**, **# 7**, **# 11**; Values changed
38	**# 13**, **# 14**; Value changed
39	**# 21**, **# 27**-**# 29**; Value changed **# 23**-**# 25**; New added
39	**# 31**, **# 32**; Value changed
41	**# 54**; Value changed
41	**# 61**-**# 66**; Value changed **# 62**; New added
43	**# 100**; Value changed # **101**; New added
49	Bit 15; Definition changed
50	Bit 7,6; Definition changed
52	Bit 5; Value changed
54	Bit 2,3,4,5; Definition changed

Preliminary Specification Version 2.0
Confidential
Revision History: **2003-12-17** TUA6120 'TORNADO'

Previous Version: V1.5 2003-07-31

Page	Subjects (major changes since last revision)
8	Splitting tuning range changed
10	Splitting tuning range changed
16	Pin 20 Equivalent I/O-Schematic, corrected
22	Block diagram corrected
29	Application circuit, Block diagram corrected
35	**# 4** Crystal oscillator divider, new
36	**# 14** AGC timing cap inputs, values changed
36	**# 17** , **# 18** $V_{REF\ -}$, $V_{VCOREF\ -}$ removed
36	**# 17** , **# 18** , **# 19** $V_{REF\ +}$, $V_{VCOREF\ +}$, V_{VREF_BBF} , values changed
36	**# 21** ESD-Protection , value changed
36	**# 23** Ambient temperature, value new
38	**# 1** Stand-by, loop- through on, changed
38	RF input testing range changed
38	**# 3** minimum RF input level test condition, new
38	**# 4** Maximum RF input level min. limit, new
38	**# 6** Gain control range min. limit, new
38	**# 7** Overall voltage gain limit, changed
38	**# 11** Input IP2, value changed
38	**# 12** Input IP2, value changed
38	**# 14** Loop-through gain test condition, new
39	**# 15** RF input DC, new
39	**# 16** RF output DC, new
39	**# 26** Filter stop band, new
40	**# 33** Base-band I / Q inputs, new
40	**# 37** AGCCAP1 voltage, new
40	**# 43** VREF_BBF, new
40	**# 45** VCOREF+, new
40	**# 47** VREF+, new
40	**# 49** GHz PLL Phase detector Charge pump output, new
41	**# 60** PLL tuning step size, new added
41	**# 63** - **# 66** Phase noise test condition, new
41	**# 67** PLL spurious at baseband outputs, new

41	**# 68** Charge pump DC value changed
42	**# 71** - **# 73** Synthesizer PLL active loop filter output, new
42	**# 74** - **# 77** Tuning VCO range added
42	**# 82** - **# 84**, **# 89** Crystal DC moved to reference oscillator I/O, new limits
43	**# 102** ADC clock for AGC, new
43	**Table 4-4** XTALDIV1 XTALDIV2, corrected
47	I^2C short read format, new
49	Note[1)] for GHz R/N-counter, new
50	Bit 8 -12; ADC clock description, added
50	Note[3)] for Preamp = on, new
54	RSSI bit 0 not used, corrected
55	VCO band switching table changed
56	VCO band splitting graph changed
58	**# 1** - **# 2** I^2C bus L, H level changed
59	Electrical Diagrams, new

Specification Version 2.01

Revision History:	**2004-02-05**	TUA6120 'TORNADO'
Previous Version:	V2.0 2003-12-17	
Page	Subjects (major changes since last revision)	
12	Correction of several Average DC voltages	
39	RF output DC, corrected	

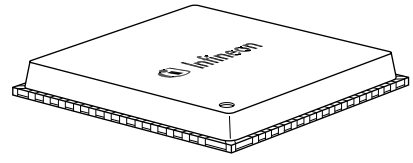
Gain controlled I/Q Mixer for digital QPSK or 8PSK Sat Signals TUA6120 'TORNADO'

Version 2.01

Product Info

General Description

The TUA6120 'TORNADO' is a direct conversion receiver for digital QPSK or 8PSK Sat receiving systems in BICMOS technology.



P-VQFN-48-4

Features

- Few, uncritical external components
- Low impedance unbalanced RF input
- RF loop-through
- Dual matched double balanced mixers
- Digital generation of 0°/90° LO signals
- On-chip oscillators
- On-chip baseband filters
- Balanced I/Q outputs
- Internal AGC for constant output level
- dB-linear RSSI readout
- CMOS PLL-Synthesizer
- 2 high current switch outputs
- Buffered crystal oscillator I/O
- Low noise reference voltage
- 3-wire bus with sub addresses
- I^2C bus with 4 chip addresses and sub addresses
- Splitting of Sat tuning range into 14 bands
- LO frequency above input frequency
- No external tuning voltage required

Application

- DBS, DVB-S, DSS and ISDB-S Set-Top Boxes
- Suitable for dual-NIM applications
- Any I/Q down converter from 915 MHz - 2185 MHz to 0 - 30 MHz

Type	Ordering Code	Package
TUA6120 'TORNADO'	Q 67037-A4	P-VQFN-48-4

1 Product Description

1.1 Overview

The TUA6120 'TORNADO' is a Direct Conversion Receiver for digital QPSK or 8PSK-Sat receiving systems in BICMOS technology.

Compared to the conventional superheterodyne receiver the DCR architecture eliminates expensive RF-filters for image rejection and IF-filters for channel selection. Instead there are on-chip filters with selectable bandwidth integrated. The DCR system is the most promising approach for low-cost digital set-top boxes front ends.

Via a LNA input stage, the RF signal is split into two rails. One is the buffered loop-through RF output and, the other goes through a PGA (Programmable Gain Amplifier) to the I/Q- Mixers.

The signal of the synthesizer VCO is multiplied to 4 x RF input frequency by an internal 3.8-8.6 GHz PLL system. To drive the mixers, this 3.8-8.6 GHz signal is split into quadrature components by a digital divider by 4.

The VCO from which the oscillator signal is derived, never runs at the input frequency.

The mixers are followed by 2 matched base-band PGA's and filters. The filter roll-off is selectable by software. Behind the filters external coupling capacitors eliminate undesired DC-components. Then follow another two base-band amplifiers and output buffers. The gain of the Q base-band amplifier is adjustable for compensation of I/Q gain impairment.

The AGC detector senses the output level and generates the control signals for the PGAs and the RSSI information which is readable via the bus. The AGC system is optimized for best SNR and IM performance.

1.2 Features

- Few, uncritical external components
- Low impedance unbalanced RF input
- RF loop-through
- Dual matched double balanced mixers
- Digital generation of 0°/90° LO signals
- On-chip oscillators
- On-chip baseband filters
- Balanced I/Q outputs
- Internal AGC for constant output level

- dB-linear RSSI readout
- CMOS PLL-Synthesizer
- 2 high current switch outputs
- Buffered crystal oscillator I/O
- Low noise reference voltage
- 3-wire bus with sub addresses
- I^2C bus with 4 chip addresses and sub addresses
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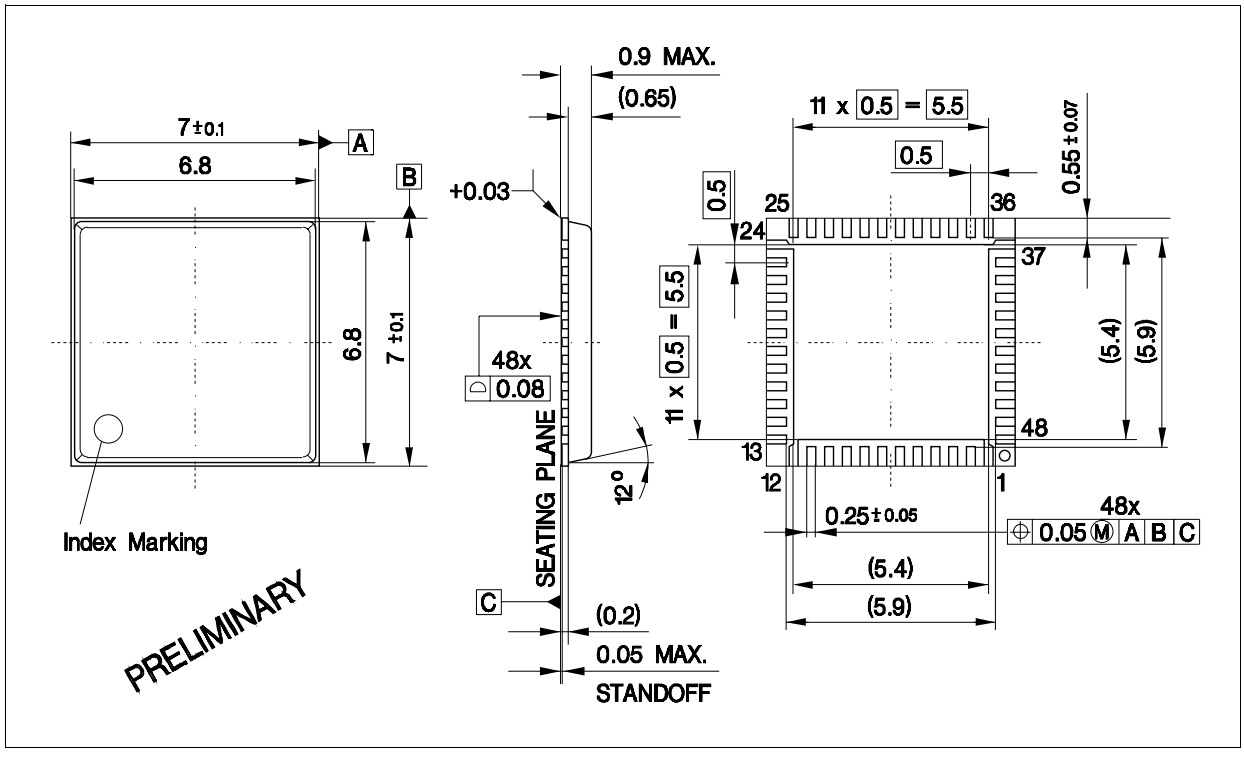
- No external tuning voltage required

1.3 Application

- DBS, DVB-S, DSS and ISDB-S Set-Top Boxes
- Suitable for dual-NIMM applications
- Any I/Q down converter from 915 MHz - 2185 MHz to frequencies 0 - 30 MHz

1.4 Package Outline



P_VQFN_48-4.eps

2 Functional Description

2.1 Pin Configuration

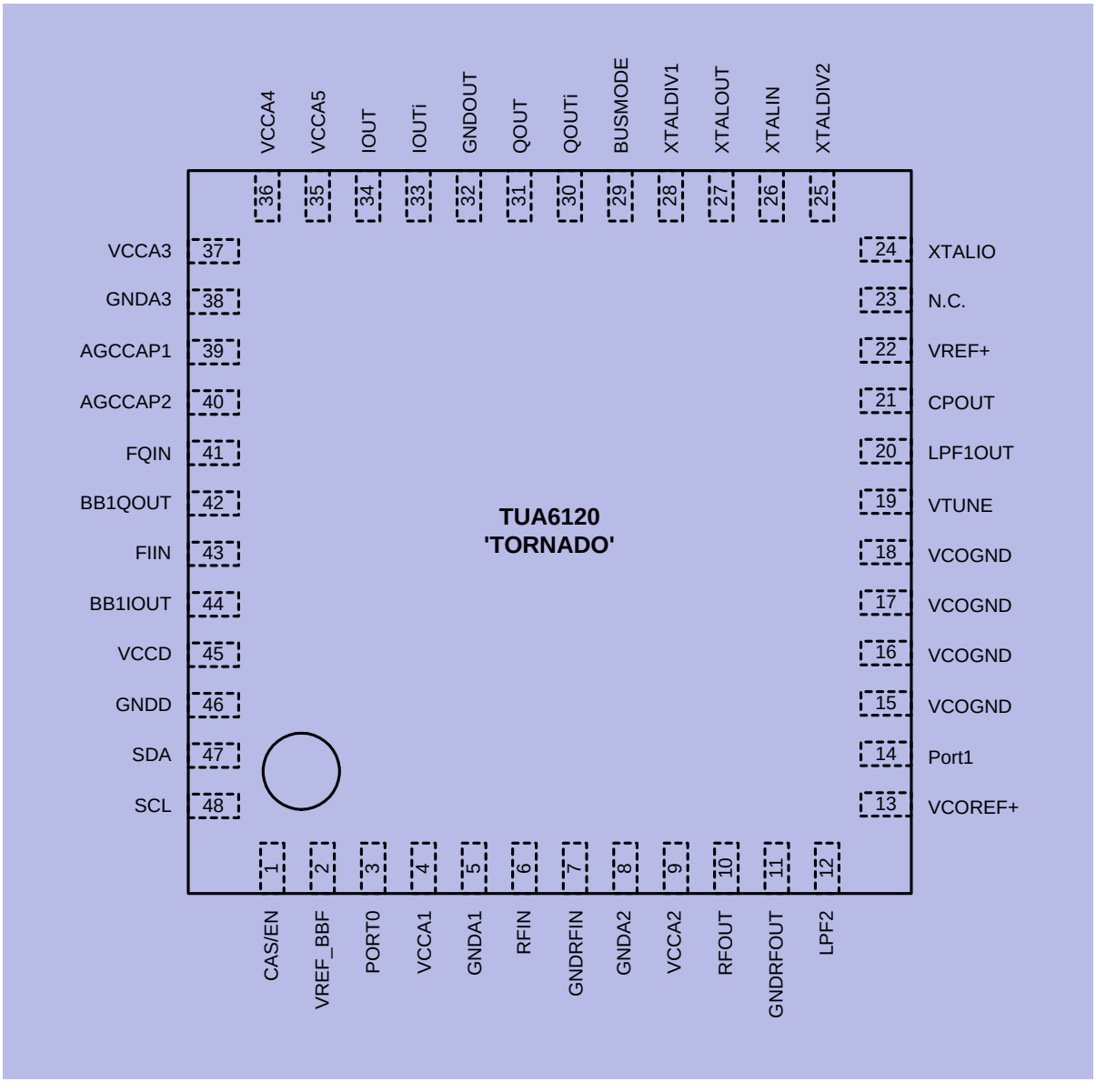


Figure 2-1 Pin Configuration

2.2 Pin Definitions and Function

Table 2-1 Pin Definition and Function

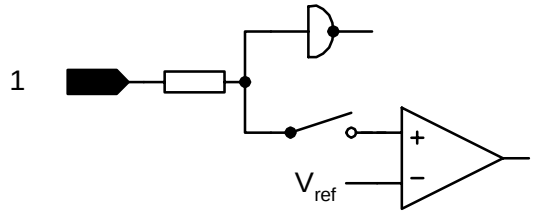
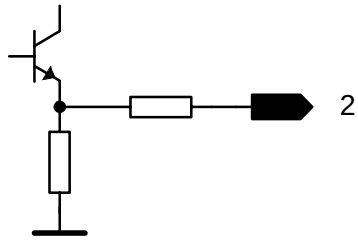
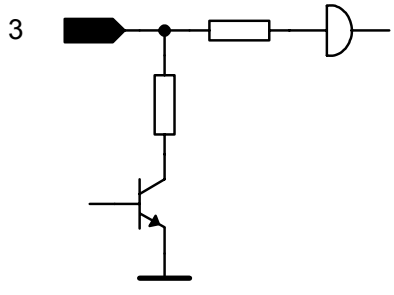
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
1	CAS/EN		n.a.
2	VREF_BBF		2.4 V
3	PORT0		0.0/5.0 V
4	VCCA1	power supply analog	5.0 V
5	GNDA1	ground	0.0 V

Table 2-1 Pin Definition and Function (continued)

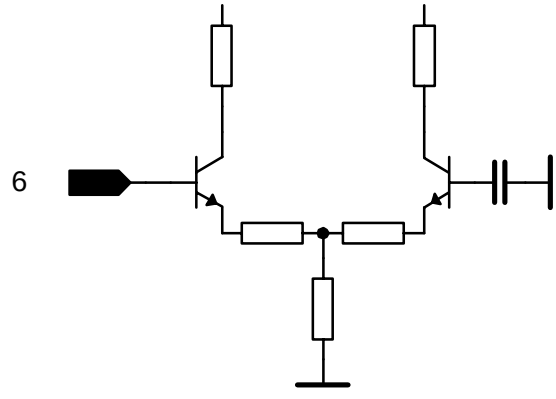
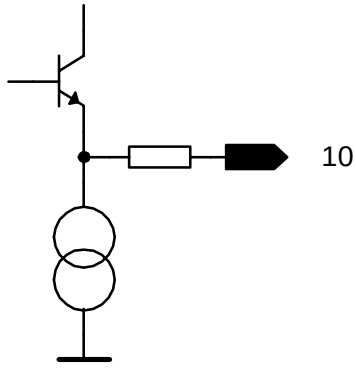
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
6	RFIN		2.0 V
7	GNDRFIN	ground	0.0 V
8	GNDA2	ground	0.0 V
9	VCCA2	power supply analog	5.0 V
10	RFOUT		1.4 V
11	GNDRFOUT	ground	0.0 V

Table 2-1 Pin Definition and Function (continued)

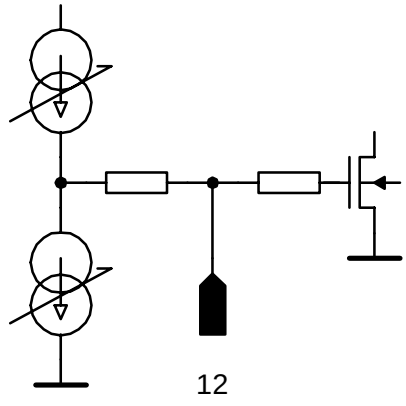
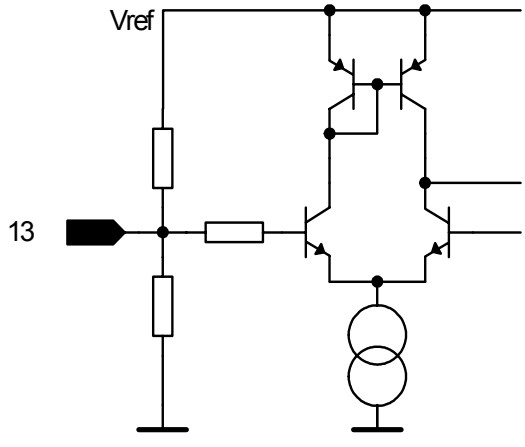
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
12	LPF2		n.a.
13	VCOREF+		1.75 V

Table 2-1 Pin Definition and Function (continued)

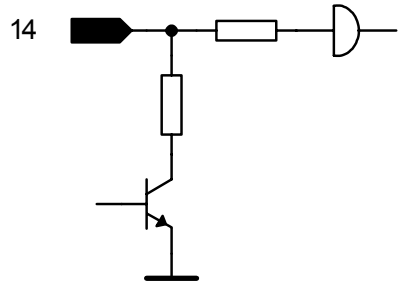
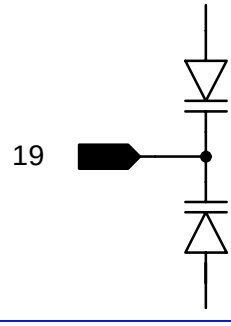
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
14	Port 1		0.0/5.0 V
15	VCOGND	ground	0.0 V
16	VCOGND	ground	0.0 V
17	VCOGND	ground	0.0 V
18	VCOGND	ground	0.0 V
19	VTUNE		n.a.

Table 2-1 Pin Definition and Function (continued)

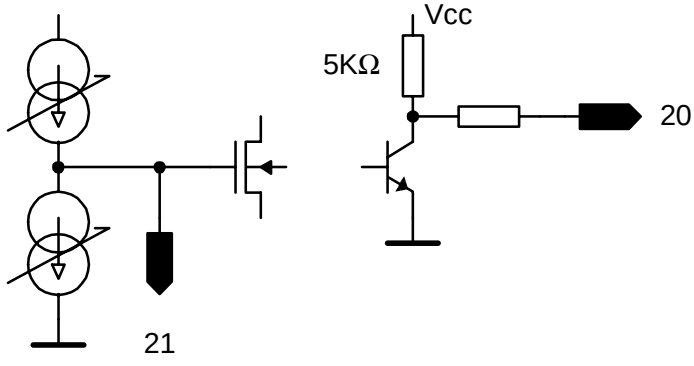
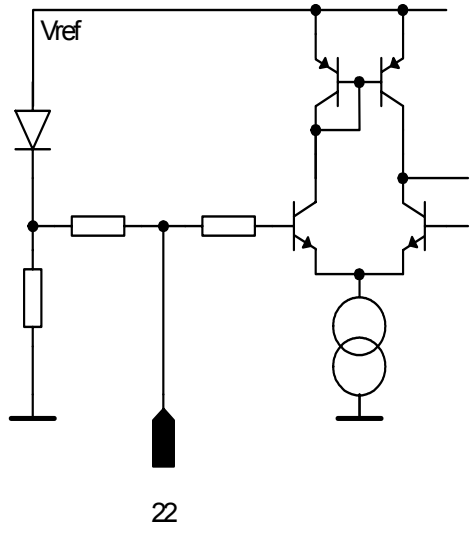
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
20	LPF1OUT		n.a.
21	CPOUT		n.a.
22	VREF+		1.6 V
23	N. C.		n. a.

Table 2-1 Pin Definition and Function (continued)

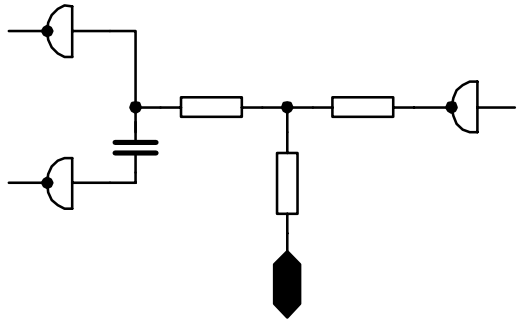
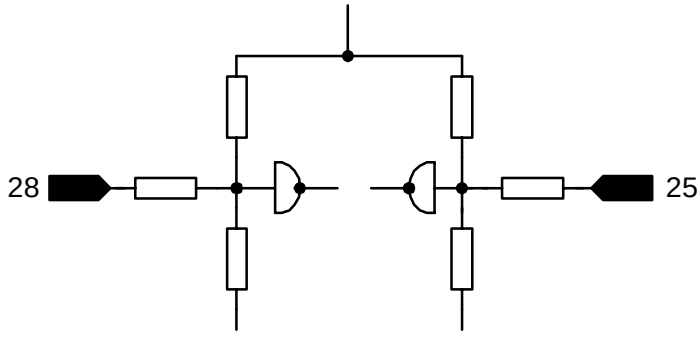
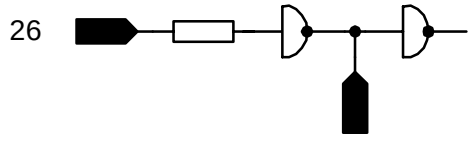
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
24	XTALIO		n.a.
25	XTALDIV2		0.0/3.2 V
26	XTALIN		1.6 V
27	XTALOUT		1.6 V

Table 2-1 Pin Definition and Function (continued)

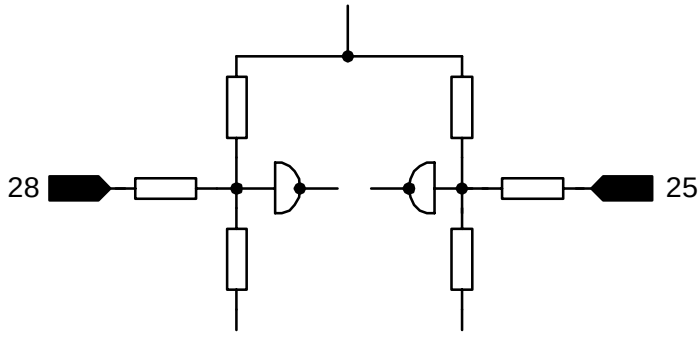
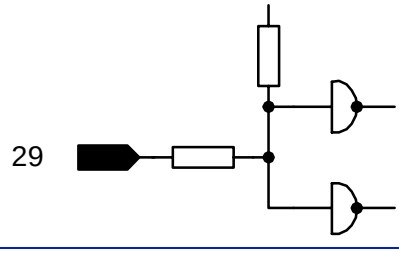
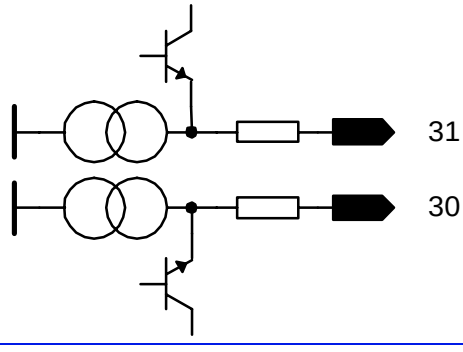
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
28	XTALDIV1		0.0/3.2 V
29	BUSMODE		5.0 V
30	QOUTi		2.4 V
31	QOUT		2.4 V
32	GNDOUT	ground	0.0 V

Table 2-1 Pin Definition and Function (continued)

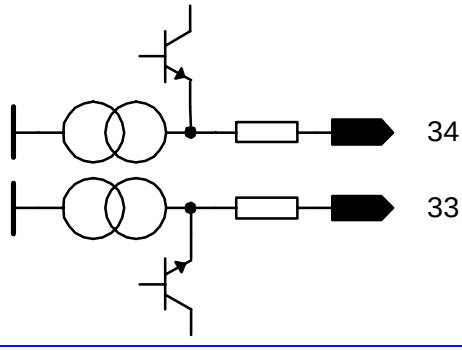
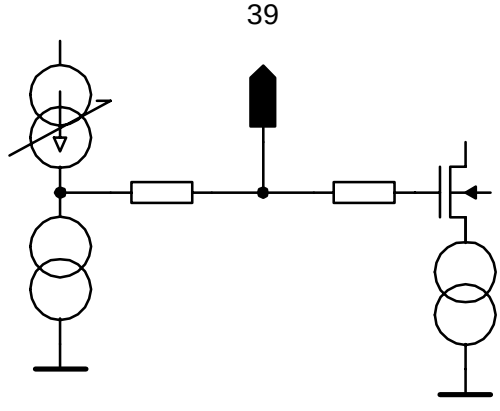
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
33	IOUTi		2.4 V
34	IOUT		2.4 V
35	VCCA5	power supply analog	5.0 V
36	VCCA4	power supply analog	5.0 V
37	VCCA3	power supply analog	5.0 V
38	GNDA3	ground	0.0 V
39	AGCCAP1		3.15 V

Table 2-1 Pin Definition and Function (continued)

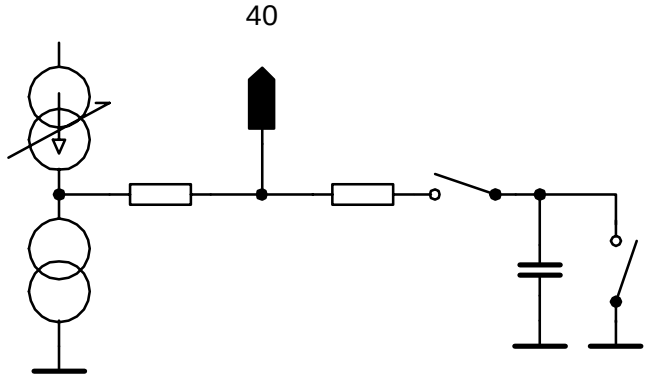
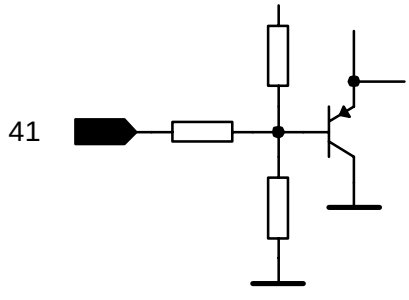
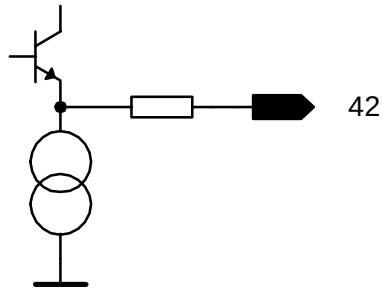
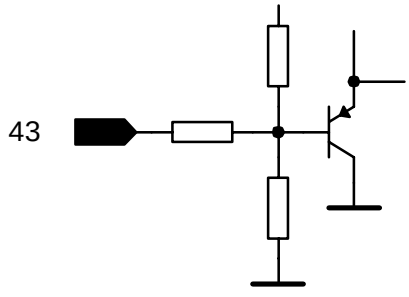
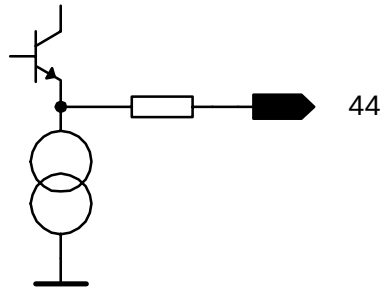
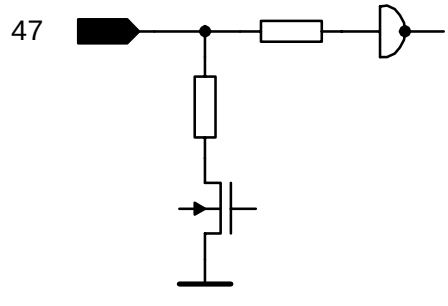
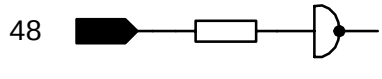
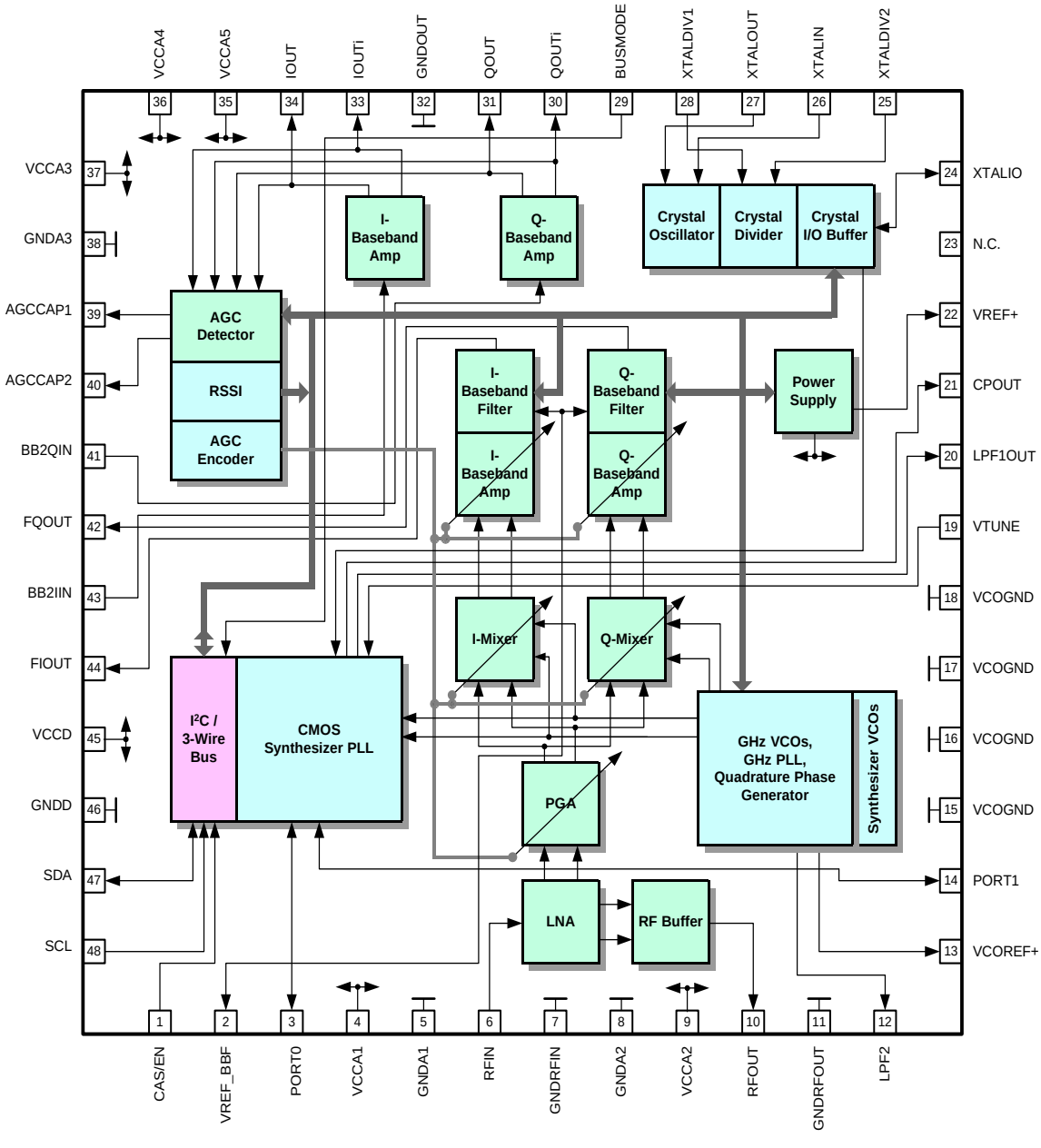
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
40	AGCCAP2 [1)]		n.a.
41	FQIN		2.4 V
42	BB1QOUT		2.4 V

Table 2-1 Pin Definition and Function (continued)

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage
43	FIIN		2.4 V
44	BB1IOUT		2.4 V
45	VCCD	power supply digital	5.0 V
46	GNDD	ground	0.0 V
47	SDA		n.a.
48	SCL		n.a.

[1] If the AGC is in external mode, this pin is used as AGC input, see Register 04 on page 51

2.3 Functional Block Diagram



TUA6120 Blockdiag

Figure 2-2 Block Diagram

2.4 Frequency programming

The tuning frequency of the RF input controlled by the PLL is given below:

$$Fin = [(P \cdot N) + A] \cdot \frac{fref}{R} = \frac{M}{R} \cdot fref \quad \text{with} \quad A \leq N$$

Figure 2-3 Input frequency calculation

rf : frequency of $RF_{input.}$

ri : reference frequency input (crystal oscillator).

P : divide ratio of the prescaler [P/(P+1) = (32/33)] .

A : divide ratio of the A-counter (max. 7 bit).

N : divide ratio of the N-counter (max. 11 bit).

R : divide ratio of the R-counter (max. 10 bit).

M = (P * N) + A : total divide ratio of the PLL (with A < N).

In addition to the above calculation, for each frequency the correct values of the GHz PLL and the VCO settings must be set. See **"VCO band switching table" on Page 55**

$$[(P \cdot N) + A] \geq P \cdot [P - 1]$$

Figure 2-4 Condition for continuous frequency steps

2.5 Functional Block Description

The main functions of the chip are split into a bipolar analog signal processing, a bipolar digital signal generation of 0°/ 90° LO-signals, and a CMOS synthesizer.
Extremely symmetrical layout with matched structures result in best phase and gain balance of the in-phase and quadrature-phase signals.

2.5.1 AGC-System

A complete AGC system is integrated. At the I/Q outputs an AGC detector monitors the output signal. It generates a dB-linear RSSI signal to the input level (Radio Signal Strength Indicator), and control signals to adjust the gain of the PGA's (Programmable Gain Amplifiers). PGA's are used because of their good intermodulation performance during gain control. The smallest AGC step is 0.5 dB, the AGC range is 63.5 dB.
The internal AGC can be disabled.
Then an external AGC voltage can be applied to pin 40.

2.5.2 LNA and RF-Buffer

The LNA is a 75 Ω input amplifier with high linearity and low noise. At its output the RF signal is split. One part goes through the RF-buffer amplifier to a 75 Ω RF-output.

2.5.3 PGA and I/Q-Mixers

The other part goes through a 48 dB control range PGA to the I and Q mixers. Both are of the double balanced mixer (Gilbert cell) type. A second PGA is arranged between the mixer output and the following baseband amplifier.

For best performance the 0°/ 90° LO-signals are fed to the mixers via open collector stages with well defined output impedance and levels.

2.5.4 Baseband Amplifiers and Filters

The 4 base band amplifiers are of wide-band operational type with high overshoot margin.

The amplifiers have a fixed gain of 16 dB and 30 MHz_{-0dB} bandwidth. The distribution of the whole DC-gain into two AC-coupled 16 dB amplifiers ensures that the base band amplifiers are not overloaded by a DC-voltage that may be caused by mixer offset or mixer LO feedback to the input. All 4 outputs can be disabled by bus control. In this state the outputs switch to low voltage and low impedance.

Filters with programmable roll-off are inserted between the baseband amplifiers.

The I and Q output voltages are programmable. The outputs are differential for best interference immunity.

2.5.5 Output Ports

The output ports are designed with open collector transistors for high current pull down and slow switching application.

2.5.6 Reference Voltage

The central reference voltage is a low noise high PSSR bandgap with approx. 2.4 V DC and low temperature drift.

2.5.7 Reference Oscillator

The reference oscillator operates with crystals from 1 - 16 MHz.

2.5.8 Crystal Oscillator Input/Output

This pin accepts an external quartz clock or supplies a quartz clock to the channel decoder. The frequency is controlled by a divider stage.

2.5.9 Synthesizer Loop filter

The synthesizer loop filter can be designed active by using an internal inverting BICMOS amplifier or passive (see Application Circuit on page 29). The loop filter input is internally connected to the phase detector / charge pump output. The BICMOS amplifier output may be disabled (high impedance) by bus.

2.5.10 Synthesizer VCO's

The synthesizer VCO's are symmetrical Colpitts type oscillators with high-Q internal tank circuits. The synthesizer VCO's oscillate at a programmable offset to the input frequency. This guarantees minimum oscillator pulling and self-mixing which results in undesirable DC offset voltage.

2.5.11 Phase Shift 0° / 90°

To get minimum quadrature phase error, a digital generation of the 0°/90° phase shifted local oscillator signal is implemented by a 3.8-8.6 GHz Johnson-counter ÷ 4 .
This counter is designed in high speed stacked ECL bipolar technology.

2.5.12 GHz VCO

This block consists of two on-chip bipolar LC-Oscillators (3.4-6.2 GHz and 6.0-8.6 GHz) controlled via on-chip PLL .
The GHz VCO's oscillate at 4 times the input frequency and are current controlled. The resonant circuit is an on chip symmetrical inductor driven by differential pair amplifier whose current variable parasitic capacitance is used for frequency tuning. The used special multi-tanh gilbert cell makes a wide tuning range possible. The GHz VCO's are under control of a 3.8-8.6 GHz PLL system. The reference frequency of this system is the output of the synthesizer VCO divided by a programmable counter; variation is 200-315 MHz (depending on the selected synthesizer tuning range). At the same time this is the operating frequency range of the phase detector / charge pump.
The high speed charge pump is completely on-chip and designed in BICMOS technology with an external loop filter bandwidth set to 9 MHz.
The GHz VCO frequency is fed to the phase detector via the high speed ECL Johnson counter ÷4 and a lower speed programmable ECL counter.

2.6 GHz PLL

With conventional DCR systems the synthesizer VCO oscillates exactly at the desired receiving frequency.

This is avoided in the **TUA6120 'TORNADO'** by a cascaded double PLL tuning system.

The main benefits of this concept are:

- accurate 0 / 90° generation of the LO signals for the RF input mixers
- no oscillator at input frequency
- programmable frequency offset of the synthesizer VCO referred to the RF input frequency and due to that a
- very low VCO oscillator pulling and self mixing due to crosstalk
- the possibility of splitting the tuning range into several bands.

These advantages are derived from a 2nd GHz PLL system with two VCO's at 4 x Fin.

This 2nd GHz PLL system is located in the broken up feedback of the synthesizer PLL 1 between the VCO1 and the programmable counter input N1.

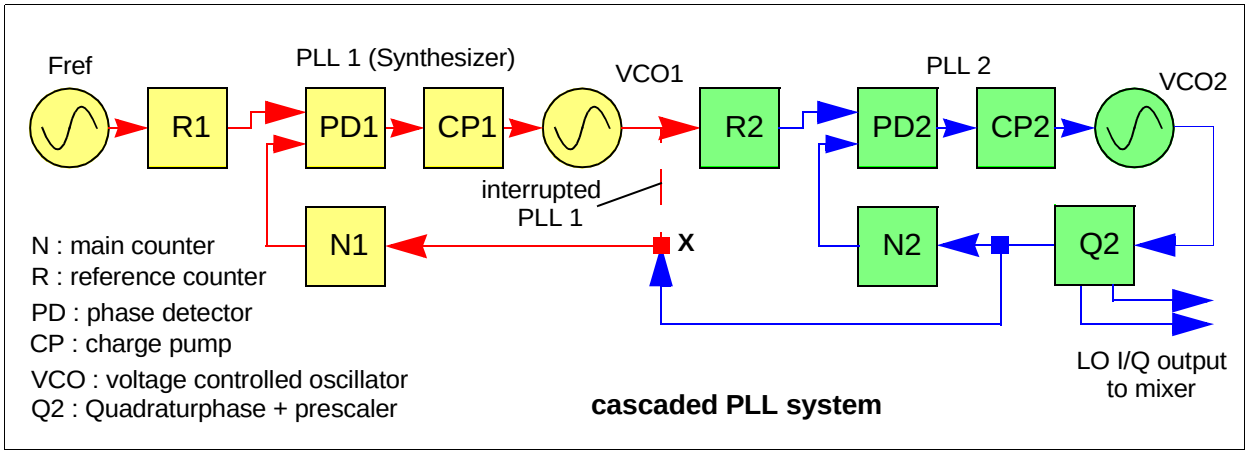


Figure 2-5 Cascaded PLL system

This location enables a shift of the synthesizer VCO1 to other frequencies, independent of the required input LO frequency of the RF mixers. In this case the synthesizer VCO must **not** oscillate at the required LO frequency of the mixer input.

Nevertheless the synthesizer PLL is referred to the LO frequency of the mixer input which makes it easy to program the PLL because it is set exactly to the receiving frequency. Another benefit is the exact mapping of the PLL stepsize to the tuning frequency.

This is not possible in a conventional PLL tuning system with the feedback of the VCO1 directly to the programmable counters N1, if the VCO1 is not running on the RF input

frequency. This may become clear in the above concept, if the interrupted PLL 1 is closed and the LO I/Q output is cut off from node x. In this case step size and tuning frequency have additional terms of calculation. Depending on the system concept. they do not fit to the programmed values of the synthesizer PLL 1, because it is referred to the VCO1 and no longer to the LO I/Q output. (Following dependencies will become valid, $F_{tune} = (N2 / R2) * F_{vco1}$ and $F_{step} = (N2 / R2) * PLL1_{step}$).

The R2 and N2 counters of the GHz PLL enable a programmable frequency offset of the synthesizer VCO to the RF input as well as a splitting of the required RF tuning range.

For the band splitting feature the counters R2 and N2 of the GHz PLL must be used with 2 different values (e.g. 4/2 and 4/3). As a result VCO1 will pass his range twice, while the LO I/Q output to mixer will have a tuning range which is split into 2 bands.

In the feedback of the GHz PLL is located the high speed Johnson-counter $\div 4$ (Q2) which acts as prescaler for the two 3.4 - 8.6 GHz VCO's and accurate 0 / 90° LO generator.

The complete GHz PLL is designed in high speed ECL cascoded technology which enables counter frequencies up to 15 GHz, oscillator frequencies up to 10 GHz and phase detector / charge pump signal slopes of less then 100 ps.

2.6.1 Functional GHz PLL Block Diagram

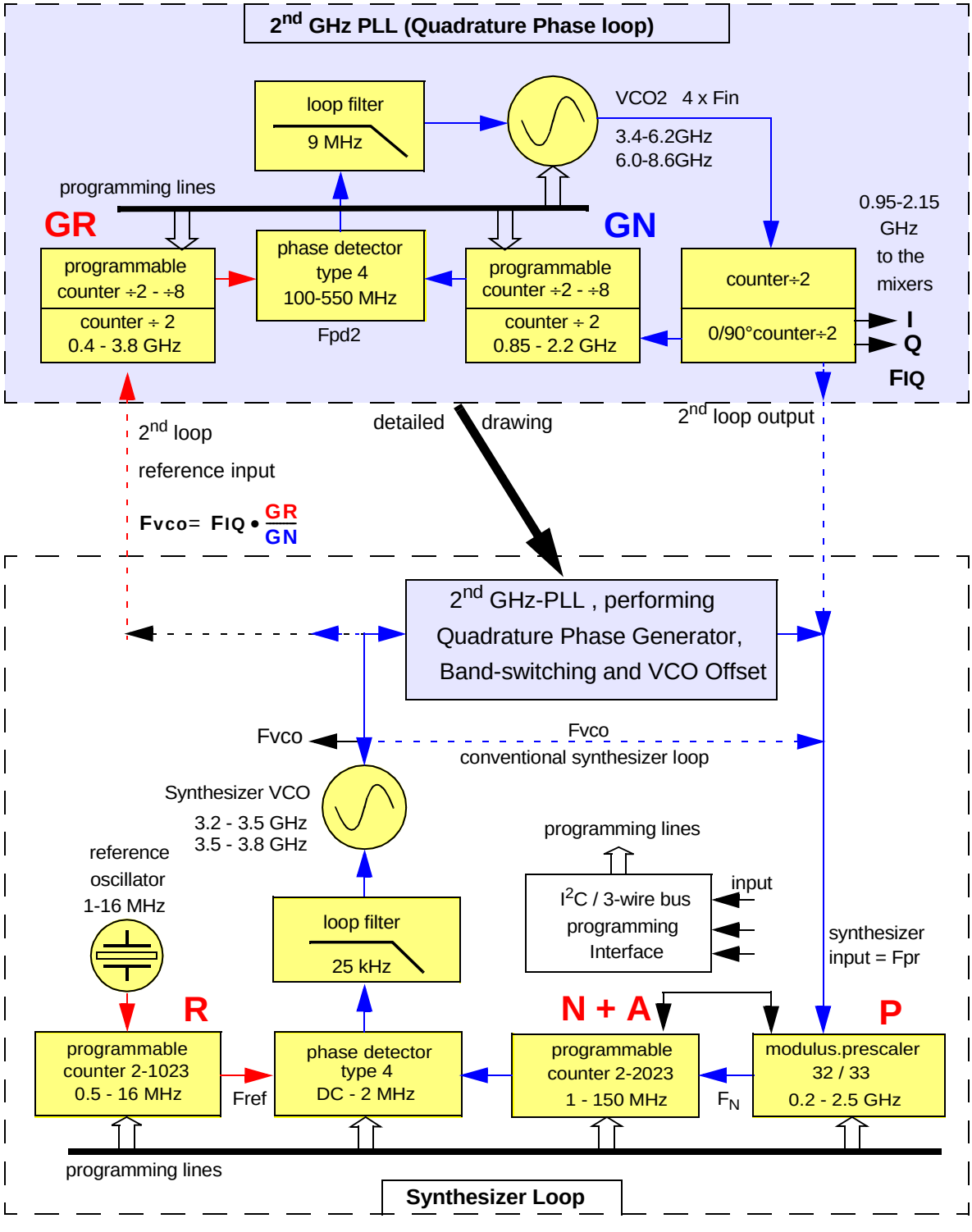
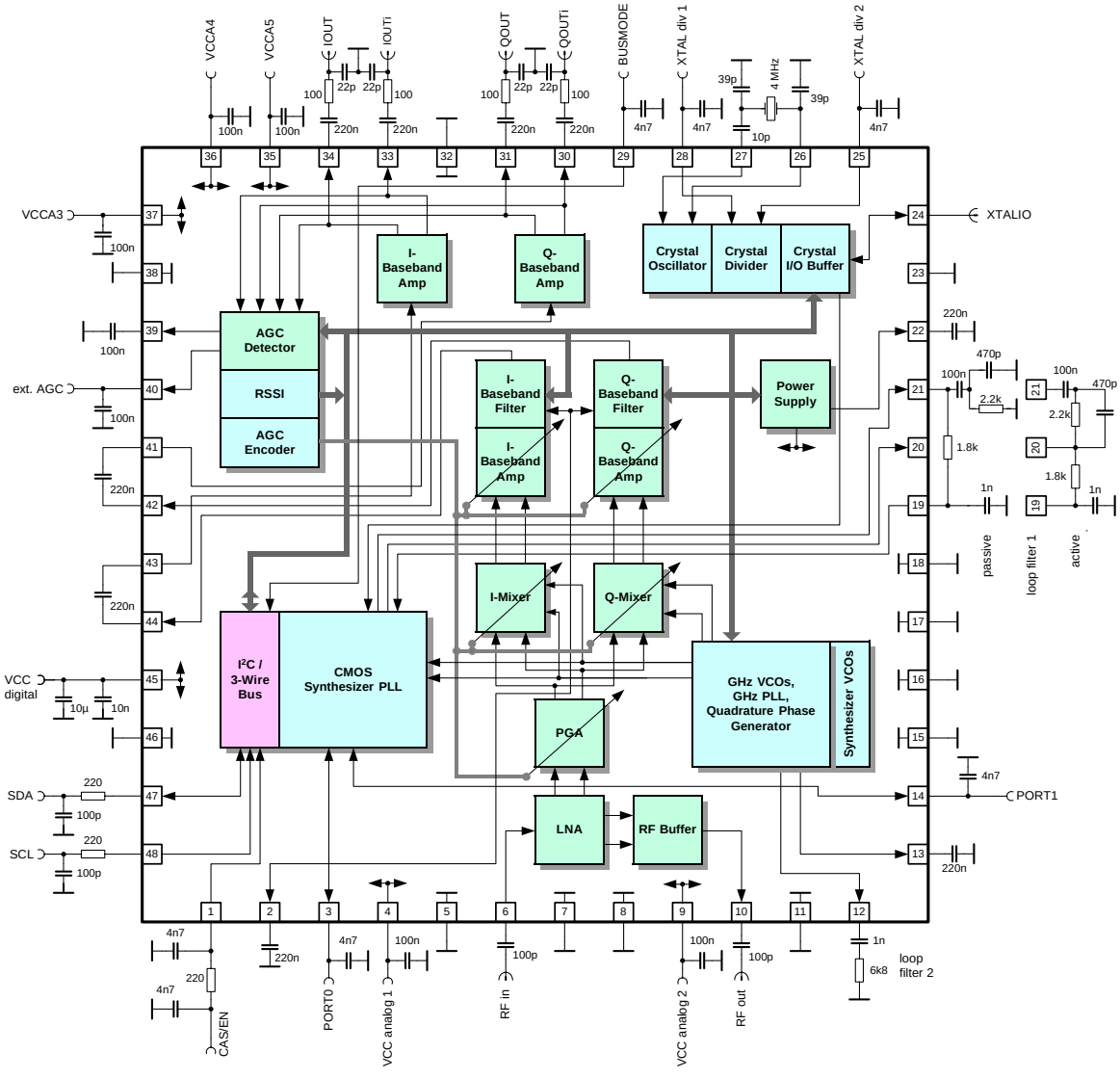


Figure 2-6 GHz PLL block diagram

3 Application

3.1 Application Circuit



TUA6120 Application

Figure 3-1 Application circuit

3.2 Phase noise performance of application

The over all system phase noise at base band of the TUA 6120 is strongly dependent on several parameters :

1.programming of the 2nd PLL (GHz-PLL setting of the R2 and N2 counter)

2.programming of the 1st synthesizer PLL

- receiving frequency (variation of the VCO steepness due to non linearity of the varicap),
- phase detector current,
- crystal frequency,
- step size = Fref,
- loop filter parameter. (bandwidth)

A well balanced phase noise over the whole tuning range requires an optimized parameter programming of the synthesizer PLL for each receiving frequency

– 1st you have to decide for the optimum loop filter bandwidth for your application.

Narrow band loop filter :
achieves better PLL outband phase noise at high frequencies offset but lower PLL inband phase noise at low frequency offset.

Wide band loop filter :
achieves better PLL inband phase noise at low frequencies offset but lower PLL outband phase noise at high frequency offset.

– 2nd you have to decide for the crystal frequency for your application.
Higher crystal frequency achieves better PLL inband phase noise.

– 3rd you have to decide for the main stepsize for your application.
Higher step size achieves better PLL inband phase noise.

– 4th during programming the desired receiving frequency you have to set step size and phase detector output current for each frequency. This is necessary to compensate the non linearity of the varicap.

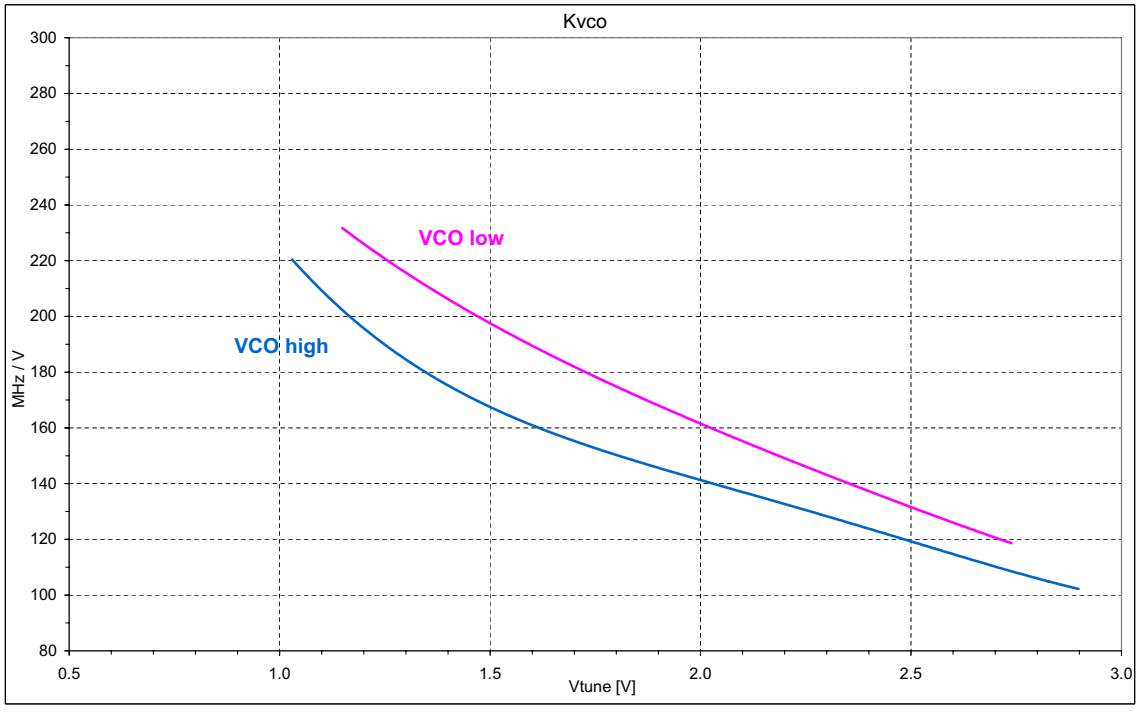
All this is done in the above application circuit which obtains in conjunction with the TUA 6120 programming kit the following worst case phase noise values :

Wide band loop filter 25 kHz, at tuning frequency 2150 MHz

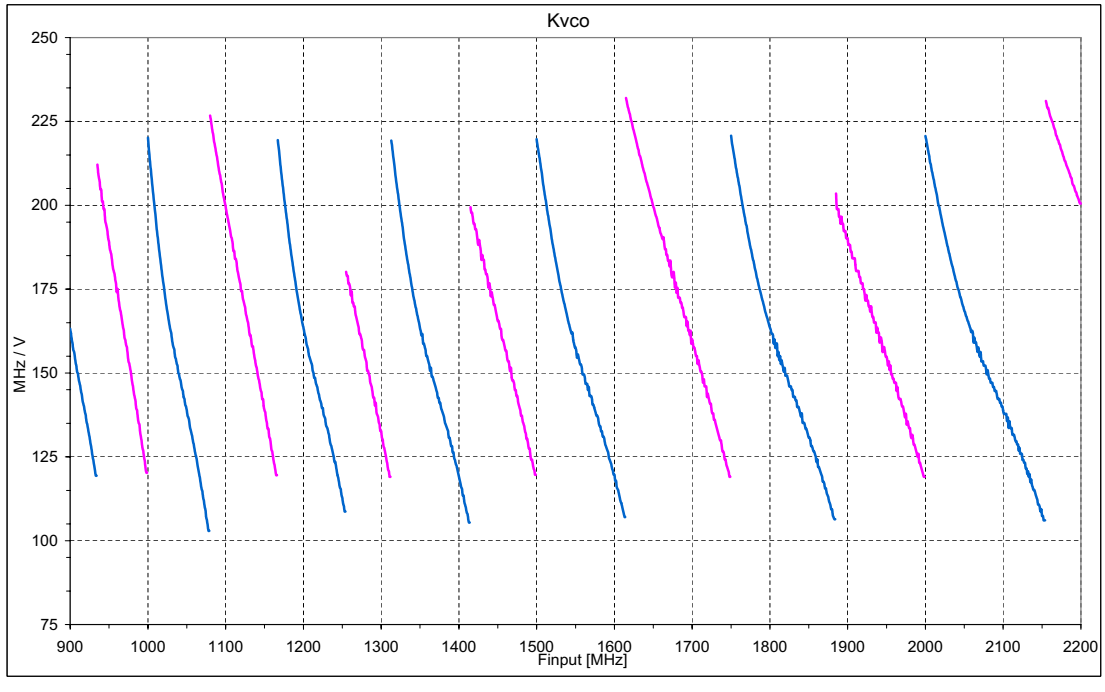
Offset Frequency	1	10	100	1000	kHz
Measured phase noise at base band	- 82	- 83	- 102	- 108	dBc/Hz

For detailed information see our separate evaluation report TUA 6120 C1/C2.

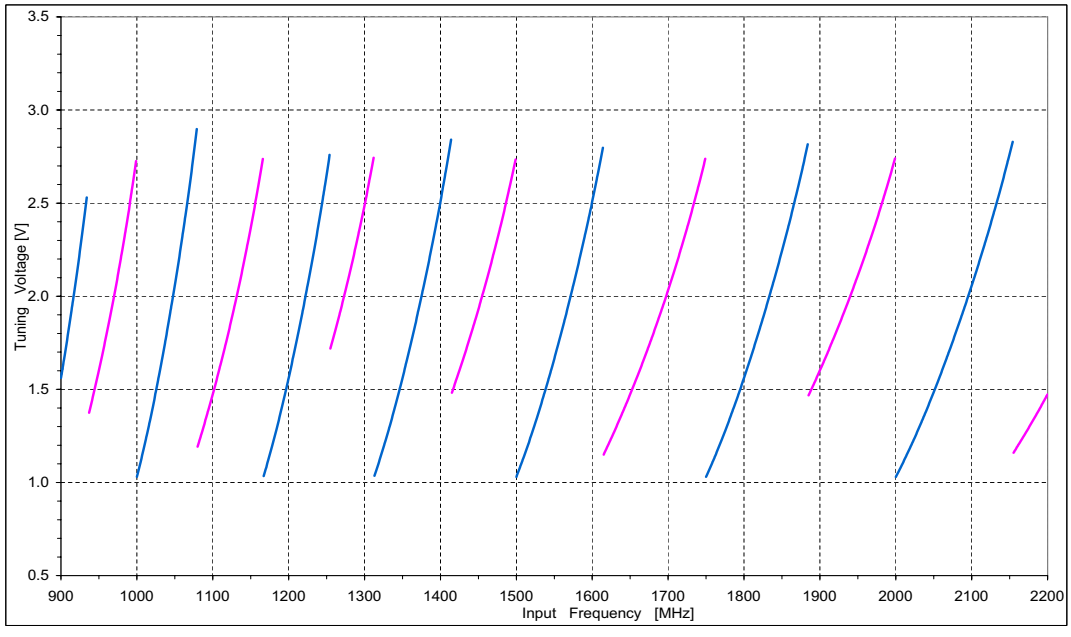
- VCO gain vs. Vtune (typical)
  valid for the application above, band splitting into 14 ranges



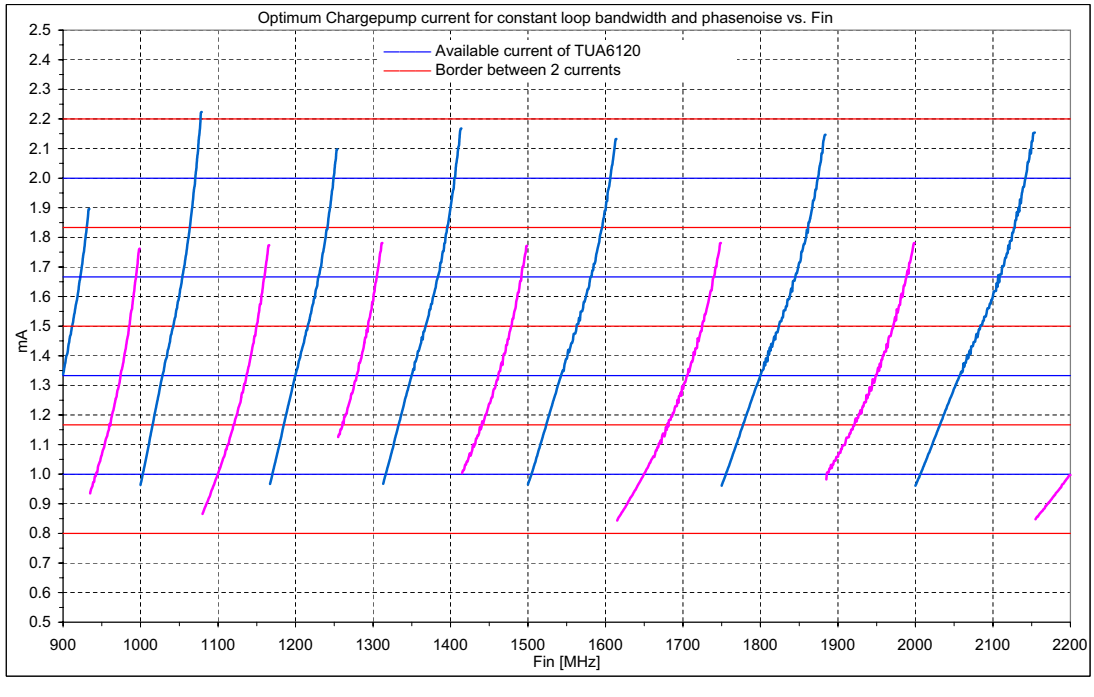
- VCO gain vs. Fin (typical)
  valid for the application above, band splitting into 14 ranges



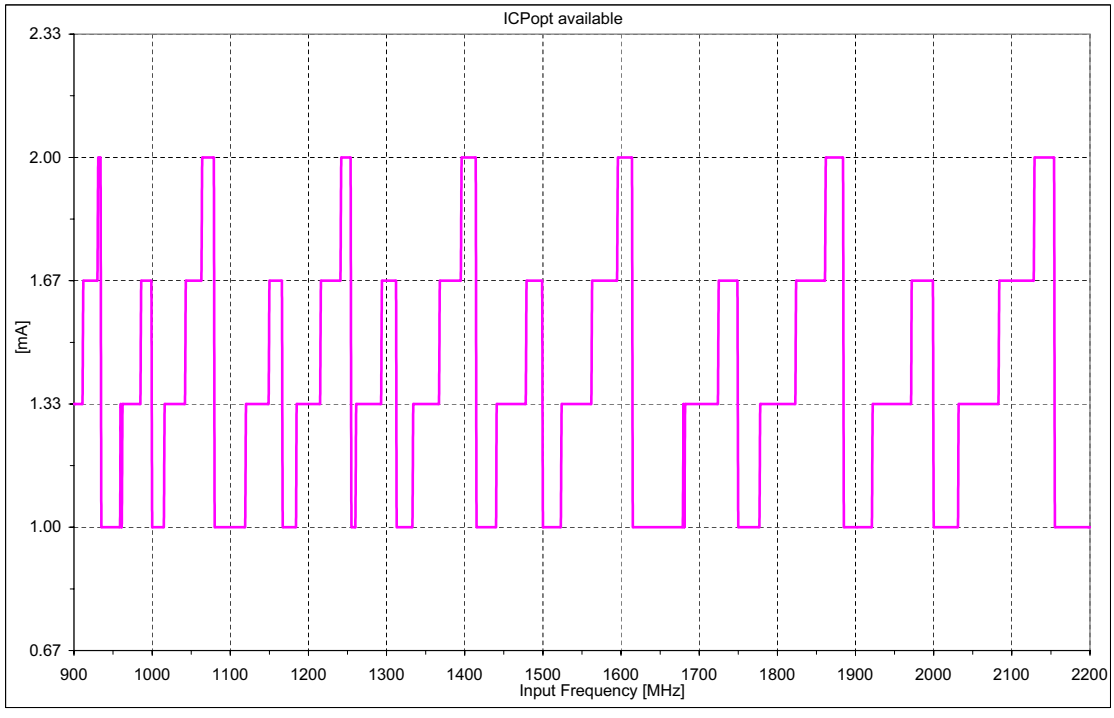
- VCO tuning voltage (typical)
  valid for the application above, band splitting into 14 ranges



- Optimum phase detector current (typical)
  for minimum loop filter bandwidth variation
  valid for the application above, band splitting into 14 ranges



- Optimum available phase detector current (typical)



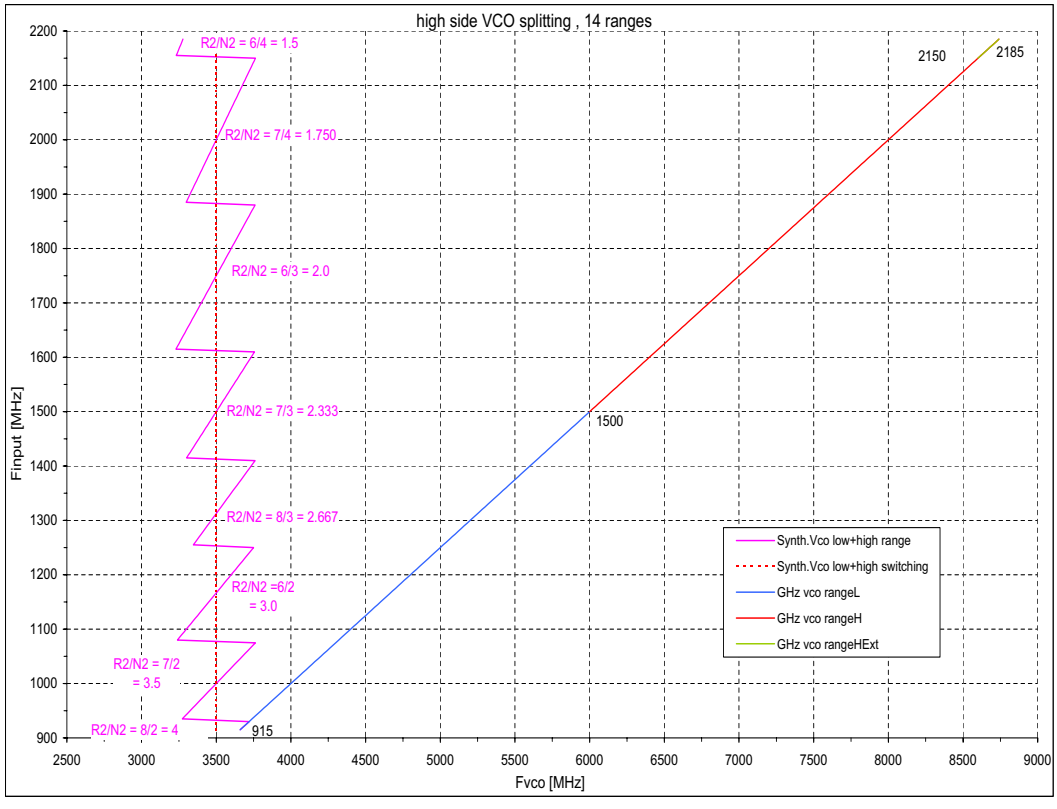
- Phase detector current switching table (typical)
  Result of graphics above

> MHz	mA
900	1.333
912	1.667
931	2.000
935	1.000
960	1.333
986	1.667
1000	1.000
1016	1.333
1043	1.667
1064	2.000
1080	1.000
1120	1.333
1150	1.667
1167	1.000
1185	1.333
1216	1.667

> MHz	mA
1242	2.000
1255	1.000
1261	1.333
1294	1.667
1313	1.000
1334	1.333
1368	1.667
1396	2.000
1415	1.000
1441	1.333
1479	1.667
1500	1.000
1524	1.333
1563	1.667
1596	2.000
1615	1.000

> MHz	mA
1680	1.333
1725	1.667
1750	1.000
1778	1.333
1824	1.667
1862	2.000
1885	1.000
1922	1.333
1972	1.667
2000	1.000
2032	1.333
2084	1.667
2129	2.000
2155	1.000

- Frequency band splitting into 14 ranges
  (no VCO frequency in receiving band)



4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 4-1 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks
1	Supply voltages 1, 2, 3, 4, 5	$V_{VCCA1, 2, 3, 4, 5}$	- 0.3	5.5	V	
2	Supply voltage 6	V_{VCCD}	- 0.3	5.5	V	
3	Crystal oscillator	$V_{XTALout, XTALin}$	- 0.3	3.2	V	
4	Crystal oscillator divider	$V_{XTALDIV1, 2}$	- 0.3	3.2	V	
5	Crystal oscillator buffered I/O	V_{XTALIO}	0	V_{VCCD}	V	
6	Synthesizer charge pump out	V_{CPOUT}	0	V_{VCCD}	V	
7	Synthesizer Loop filter output	$V_{LPF1OUT}$	0	V_{VCCD}	V	
8	Port outputs	$V_{P0, P1}$	0	V_{VCCD}	V	
		$I_{P0, P1}$		15	mA	
		$\Sigma I_{P0, P1}$		30	mA	
9	Port outputs, $V_{P0, P1} = V_{VCCD}$, I = max	t_{Imax}		1	ms	
10	GHz-PLL Charge pump out	V_{LPF2}	0	V_{VCCA2}	V	
11	Baseband outputs	V_{FIOUT}, V_{FQQOUT}	0	V_{VCCA2}	V	
		$I_{BB1IOUT}$, $I_{BB1QOUT}$		4	mA	
12	Baseband filter inputs I/Q	V_{BB2IIN}, V_{BB2QIN}	0	V_{VCCA1}	V	

Table 4-1 Absolute Maximum Ratings (continued)

#	Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks
13	Baseband outputs	$V_{IOUT, IOUTi}$, $V_{QOUT, QOUTi}$	0	V_{VCCA1}	V	
		$I_{IOUT, IOUTi}$, $I_{QOUT, QOUTi}$		4	mA	
14	AGC timing cap inputs	$V_{AGCCAP1}$, $V_{AGCCAP2}$	0	3.2	V	
15	RF input	V_{LNA}	0	3.5	V	
16	RF output	V_{RFOUT}	1.0	2.0	V	
17	Reference voltage filter	V_{REF+}	0	3.2	V	
18	VCO Reference voltage filter	$V_{VCOREF+}$	0	3.2	V	
19	Baseband filter reference	V_{VREF_BBF}	0	3.2	V	
20	I^2C / 3-Wire-Bus	SCL,SDA, CAS/EN BUSMODE	- 0.3	V_{VCCD}+0.3	V	
21	ESD-Protection	V_{ESD}		2	kV	1)
22	Total power dissipation	P_{tot}		1300	mW	
23	Ambient temperature	T_A	-20	70	°C	2)
24	Junction temperature	T_j		125	°C	
25	Storage temperature	T_{stg}		150	°C	
26	Thermal resistance junction case	R_{th}		2	K/W	3)

1) all ESD tests done according to EIA/JESD22-A114-B (HBM in circuit test), as a single device in circuit contact discharge test.

2) The maximum ambient temperature depends on the mounting conditions of the package. Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C.

3) Referred to top center of package.

Notes:

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

4.1.2 Operating Range

Table 4-2 Operating Range

#	Parameter	Symbol	Limit Values min	Limit Values max	Unit	Test Conditions	■	Item
1	Supply voltages 1,2,3,4,5	$V_{VCCA1, 2, 3, 4, 5}$	4.75	5.25	V			
2	Supply voltage 6	V_{VCCD}	4.75	5.25	V			
3	Difference between VCCA1, VCCA2, VCCA3, VCCA4, VCCA5, VCCD and between all GND pins	Δ V	-0.3	0.3	V			
4	Input frequency range	f_{RFIN}	915	2185	MHz			
5	Ambient temperature	T_A	-20	70	°C			1)

■ This value is not subject to production test - verified by design/characterization.

1) The maximum ambient temperature depends on the mounting conditions of the package.
Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C.

4.1.3 AC/DC Characteristics

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1},V_{CCA2}, V_{CCD} = 5 V

#	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions	■	Item
Power supply									
1	Total current consumption	I_{VCCA1}+	155	189	225	mA	normal operation		pin 4,9, 35, 36, 37, 45
		I_{VCCA2}+ I_{VCCA3}+ I_{VCCA4}+		183		mA	loop-through off		
				9		mA	Total stand by		
		I_{VCCA5}+ I_{VCCD}		50		mA	Stand-by, loop-through on		
RF input (950-2150MHz) RF source impedance 75 Ω, RF input, pin 6, test circuit									
2	Input frequency	f_{RFIN}	915		2185	MHz			pin 6
3	minimum RF input level	V_{RFIN}		-79.5		dBm	f = 1000 MHz		
			-82		-77	dBm	output level = $1V_{pp}$ differential		
4	maximum RF input level	V_{RFIN}	-19.5	-17.0		dBm	f = 1000 MHz, in AGC range		
				-8		dBm	out of AGC range	■	
5	Input impedance	R_{RFIN}		75		Ω	f = 0.9 - 2.2 GHz	■	
		C_{RFIN}		1.2		pF		■	
6	Gain control range	ΔG_V	61	63.5		dB			
7	Overall voltage gain	G_V	81	83,5		dB	output level = $1V_{pp}$ differential		
8	VCO power present at RF input	P_{VCO}	-60	- 50	-40	dBm	f = R_2 / N_2 x f_{in}	■	
9	LO power present at RF input	P_{LO}		- 90	-80	dBm	f = f_{in}	■	
10	input compression point -1 dB	ICP	-5	-3		dBm	minimum gain	■	
11	Input IP2	IIP2	35	40		dBm	input level = -25 dBm output level = 600 mVpp differential 22MHz BBfilter on	■	
12	Input IP3	IIP3	5	10		dBm		■	
13	Noise Figure	NF		10	11.5	dB	maximum gain, DSB	■	
14	Loop-through gain	Gp		-1		dB	75 Ω, load		pin 10

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1}, V_{CCA2}, V_{CCD} = 5 V (cont'd)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
RF input DC									
15	DC voltage	V_{RFin}	1.8	2.0	2.2	V			pin 6
RF output DC									
16	DC voltage	V_{RFout}	1.2	1.4	1.6	V			pin 10
Base-band I / Q outputs, IOUT, IOUTi, QOUT, QOUTi, BB1IOUT, BB1QOUT, pins 34-33, 31-30, 44, 42									
17	DC voltage	$V_{Iout,Qout}$		2.4		V	R_L>1MΩ		also pins 42, 44
18	DC quiescent current	$I_{Iout,Qout}$		2.4		mA	R_L>1MΩ		
19	Baseband I/Q output voltage see Register 05 on page 52	V_{IOUT} V_{QOUT}	500	1000	2000	mV_{pp}	R_L>1MΩ, C_L < 10p, differential		
20	Baseband I/Q output bandwidth	$BW_{-0.5\ dB}$	20	22		MHz	no filter reference=1MHz 1V_{pp} differential		
21		$BW_{-1\ dB}$	30	35		MHz			
22		$BW_{-3\ dB}$	50	60		MHz			
23	Baseband filter 1 bandwidth	$BW_{-1\ dB}$	9.8	11	12.2	MHz	reference=1MHz 1V_{pp} differential Table "Register 05" on Page 52		
24	Baseband filter 2 bandwidth	$BW_{-1\ dB}$	19.5	22	24.5	MHz			
25	Baseband filter 3 bandwidth	$BW_{-1\ dB}$	29	33	37	MHz			
26	Filter stop band	ATT	-45	-50		dBc	f > 3 x $f_{roll-off}$		
27	Baseband I/Q output flatness	ΔG		0.5		dB	up to 10 MHz, no filter	■	
28	Quadrature error, phase	ΔΦ		2	4	deg	950 MHz, 1600 MHz, 2150 MHz, RFin = -35 dBm, test circuit		
29	Quadrature error, gain	ΔG		0	0.5	dB			
30	Baseband I/Q output impedance	R_{IOUT}, R_{QOUT}			50	Ω	dynamic resistance	■	also pins 42, 44
31	SNR @ 45 Mbaud, 1Vpp differential	IFOUT, QFOUT	5	7		dB	maximum gain	■	
32		IFOUT, QFOUT	28	33		dB	minimum gain	■	

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1}, V_{CCA2}, V_{CCD} = 5 V (cont'd)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	■	Item
			min	typ	max				
Base-band I / Q inputs FIin, FQin, pins 41, 43									
33	DC voltage	$V_{FIin,FQin}$		2.4		V	R_L>1MΩ		
34	Input resistance	$R_{FIin,FQin}$		18		kΩ	internal	■	
AGCCAP2 voltage input									
35	Gain control range	ΔV_{GAIN}	0.35		1.65	V	typical values		pin 40
36	Gain control input impedance	R_{GAIN}	1			MΩ		■	pin 40
AGCCAP1 voltage (AGC = internal)									
37	Agc rectifier voltage	$V_{Agccap1}$		3.15		V	within AGC range	■	pin 39
Port outputs, P0, P1									
38	Supply voltage	V_P	0		5.5	V	max. Vcc		pins 3,14
39	LOW output voltage	V_P	0		0.5	V	I_P = 15 mA		
40	LOW output current	I_P			15	mA			
41	HIGH output current	I_P	0		10	µA	V_P = 5 V		
42	Port outputs,I = max	t_{Imax}			1	ms	$V_{P0, P1} = V_{VCC}$		
VREF_BBF									
43	Reference voltage	V_{ref}	2.2	2.4	2.6	V			pin 2
44	Vref output current	I_{ref}			2	mA		■	
VCOREF+									
45	Reference voltage	V_{ref}	1.6	1.75	1.9	V			pin 13
46	Vref output current	I_{ref}			2	mA		■	
VREF+									
47	Reference voltage	V_{ref}	1.45	1.6	1.75	V			pin 22
48	Vref output current	I_{ref}			2	mA		■	
GHz PLL Phase detector Charge pump output / Loop filter input									
49	DC voltage	V_{LPF2}	0.4		4.5	V	loop locked		pin 12
50	DC current	I_{LPF2}	-100		100	µA		■	

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1}, V_{CCA2}, V_{CCD} = 5 V (cont'd)

#	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions	■	Item
Synthesizer PLL									
51	N-counter divider	N	2		2047		11-Bit, CMOS	■	
52	A-counter divider	A	0		127		7- Bit, CMOS	■	
53	R-counter divider	R	2		1023		10-Bit, CMOS	■	
54	Prescaler divider	P		32/33			Bipolar		
55	Equivalent phase noise at phase detector input, @ 1 kHz offset, within loop band width, 6 kHz loop BW, SSB	Φ_{PLL}		-164		$^{dBc}/_{Hz}$	f_{ref} = 30 kHz	■	
56		Φ_{PLL}		-159		$^{dBc}/_{Hz}$	f_{ref} = 100 kHz	■	
57		Φ_{PLL}		-158		$^{dBc}/_{Hz}$	f_{ref} = 125 kHz	■	
58		Φ_{PLL}		-155		$^{dBc}/_{Hz}$	f_{ref} = 250 kHz	■	
		Φ_{PLL}		-149		$^{dBc}/_{Hz}$	f_{ref} = 1000 kHz	■	
59	Quadrature phase mismatch	$\Delta\Phi$		2	4	deg			
60	PLL tuning step size	f_{ref}	1		2000	kHz		■	
61	Total divider ratio [1]	M	992		65631		P = 32/33	■	
62	Input frequency	f_{RFIN}	794 992 1984			MHz	f_{ref} = 800 kHz f_{ref} = 1 MHz f_{ref} = 2 MHz		

[1] The minimum total divider ratio is only important for continuous frequency step size, if lower divider ratios are used not all frequencies are possible. To find out the missing frequencies our control program for I^2C / 3-wire bus may be used.

Overall phase noise, fref = 800 kHz, loop filter bandwidth = 25 kHz (Figure 3.1)

63	Phase noise SSB output level = +10dBm, 2 MHz	Φ_{tot}	80	84		$^{dBc}/_{Hz}$	1 kHz offset	■	
64		Φ_{tot}	82	86		$^{dBc}/_{Hz}$	10 kHz offset	■	
65		Φ_{tot}	100	105		$^{dBc}/_{Hz}$	100 kHz offset	■	
66		Φ_{tot}	105	110		$^{dBc}/_{Hz}$	1 MHz offset	■	

PLL spurious at baseband outputs IOUT, IOUTi, QOUT, QOUTi

67	PLL spurious	ATT	-40			dBc	f_{out}=1MHz, $1V_{pp}$ diff.		

Synthesizer Phase detector Charge pump output / Vtune input

68	DC voltage	V_{CPOUT}	0.4		4.5	V	loop locked		pin 19
69	DC current	I_{CPOUT}	1		2	mA			
70	Tristate output current	I_{CPOUT}		0.1	1	nA	V_{CPOUT} = 2 V		pin 21

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1}, V_{CCA2}, V_{CCD} = 5 V (cont'd)

#	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions	■	Item
	Synthesizer PLL active loop filter output								
71	DC voltage	$V_{LPF1out}$	0.4		V_{VCC}	V	internal Pull-up		pin 20
72	DC current	$I_{LPF1out}$	10		5000	µA			
73	internal pull-up	$R_{LPF1out}$		5		kΩ	connect to V_{CCD}	■	
	Tuning VCO's								
74	Synthesizer VCO 1	f	3230		3500	MHz			
75	Synthesizer VCO 2	f	3500		3770	MHz			
76	GHz VCO 1	f	3600		6200	MHz			
77	GHz VCO 2	f	5900		8800	MHz			
	Crystal oscillator								
78	Crystal frequency	f	1	4	16	MHz	parallel resonance	■	pins 26, 27
79	Crystal resistance	R		30	100	Ω	series resonance	■	
80	negative input impedance	Z_{XTALIN}		420		Ω	f = 4 MHz	■	
81	Drive current	I_{QOSZ}		900		$µA_{rms}$	f = 4 MHz	■	
	Reference oscillator input/output								
82	DC voltage XTALIN see Register 02 on page 50	V_{XTALIN}	-0.2	0	3.0	V	preamp enabled	■	pin 24
			0	0.9	3.0	V	preamp disabled	■	
83	XTALIO input voltage, see Register 02 on page 50	V_{XtalIO}	150	200	1000	mV_{pp}	preamp = on	■	
84			1.5	1.8	3.0	V_{pp}	preamp = off	■	
85	XTALIO input impedance	R_{XtalIO}		400		kΩ		■	
86	XTALIO output voltage see Register 02 on page 50	V_{XtalIO}		1.6		V_{pp}	R_L > 1MΩ,	■	
87				2.4		V_{pp}	Vcc = 5 V,	■	
88				3.2		V_{pp}	C_L = 10 pF	■	
89	XTALOUT V_{DC}	$V_{XTALOUT}$	0		3.2	V	see Register 02 on page 50		
90	XTALIO output current	I_{XtalIO}			0.1	mA		■	
91	XTALIO output impedance	R_{XtalIO}		1.4		kΩ	V_{XtalIO} = 1.8 V_{pp}	■	
92		R_{XtalIO}		1.2		kΩ	V_{XtalIO} = 2.6 V_{pp}	■	
93		R_{XtalIO}		1.2		kΩ	V_{XtalIO} = 3.3 V_{pp}	■	

Table 4-3 AC/DC Characteristics, T_A = 25 °C, V_{VCCA1}, V_{CCA2}, V_{CCD} = 5 V (cont'd)

#	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions	■	Item
	I^2C and 3-Wire-bus Clock, Data, Enable, pins 1, 47, 48								
94	HIGH level input voltage	V_{IH}	1.30		V_{VCC}	V	V_{VCC} of µP in the range 1.8 to 5 V		
95	LOW level input voltage	V_{IL}	-0.5		0.71	V			
96	LOW level output voltage (DATA), only I2C-bus	V_{OL}	0		0.4 0.6	V	3 mA sink current 6 mA sink current		
97	Hysteresis of Schmitt trigger inputs	V_{hys}	0.2			V		■	
98	H-input current	I_H			10	µA	$V_I = V_{VCC}$		
99	L-input current	I_L	-10			µA	V_I = GND		
	BUSMODE								
100	H-input current H-input voltage L-input current	I_H V_H I_L	 V_{VCC}-1 -60	 V_{VCC}	10	µA V µA	$V_I = V_{VCC}$ V_I = open V_I = GND		pin 29
	XTALDIV1, XTALDIV2								
101	H-input voltage L-input current	V_H I_L	2.8 -60	3.2		V µA	V_I = open V_I = GND		pins 25, 28
	ADC clock for AGC = Crystal frequency / ADC clock divider						see Register 02 on page 50		
102	ADC clock freq.	f_{in}		0.5	1	MHz			

1) V_{VCC} of µP in the range 1.8 to 5 V.

Table 4-4 XTAL divider ratio

XTALDIV2 1)	XTALDIV1 1)	XTAL divider ratio
0	0	1
0	1	2
1	0	4
1	1	8

1) 0: Pin is connected to ground. 1: Pin is open (internal pull up current).

4.2 Bus Interface

4.2.1 Addressing

Table 4-5 Pin Function

Pin Designation	BUSMODE	SDA	SCL	CAS / EN
Function	**bus mode select**	**serial data**	**clock**	**I²C: chip address select,3-W: enable**
I²C mode	0	data in/out	clock in	four chip addresses [1]
3-wire mode	1 or open			0: chip is addressed

[1] see Table 4-6 Chip Address Organization in I2C Mode on page 44,
see Table 4-7 Address selection in I2C Mode on page 44.

Table 4-6 Chip Address Organization in I²C Mode

Name	Byte	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
Write Mode									
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=0
Read Mode									
Address Byte	ADB	1	1	0	0	0	MA1	MA0	R/W=1

Table 4-7 Address selection in I²C Mode

			Chip Address (Hex)	
Voltage at CAS/EN	**MA1**	**MA0**	**Write Mode**	**Read Mode**
(0 to 0.1) x V_{CC}	0	0	C0	C1
open circuit or (0.2 to 0.3) x V_{CC}	0	1	C2	C3
(0.4 to 0.6) x V_{CC}	1	0	C4	C5
(0.9 to 1) x V_{CC}	1	1	C6	C7

4.2.2 Sub Addressing

Table 4-8 Sub Addresses of Write Data Registers

Function	Hex	MSB	S6	S5	S4	S3	S2	S1	LSB
A/N Divider	00	0	0	0	0	0	0	0	0
Reference Divider	01	0	0	0	0	0	0	0	1
Control Bytes	02	0	0	0	0	0	0	1	0
Port Byte	03	0	0	0	0	0	0	1	1
AGC Mode	04	0	0	0	0	0	1	0	0
Baseband Control	05	0	0	0	0	0	1	0	1
Test Modes	06	0	0	0	0	0	1	1	0

Table 4-9 Sub Addresses of Read Data Registers

Function	Hex	MSB	S6	S5	S4	S3	S2	S1	LSB
Status	80	1	0	0	0	0	0	0	0
not used	81	1	0	0	0	0	0	0	1
RSSI	82	1	0	0	0	0	0	1	0

4.3 Bus Data Format

Table 4-10 Bus Data Format

I^2C-bus Write Mode

Bit	Function
STA	
1	MSB
1	chip address (Write)
0	
0	
0	
MA0	
MA1	
0	LSB
ACK	
S7	MSB
S6	sub address (Write) 00H...06H
S5	
S4	
S3	
S2	
S1	
S0	LSB
ACK	
DX	MSB
...	data in X...0 (X=7,15 or 23)
D5	
D4	
D3	
D2	
D1	
D0	LSB
ACK	
STO	

I^2C-bus Read Mode

Bit	Function
STA	
1	MSB
1	chip address (Write)
0	
0	
0	
MA0	
MA1	
0	LSB
ACK	
S7	MSB
S6	sub address (Read) 80H...82H
S5	
S4	
S3	
S2	
S1	
S0	LSB
ACK	
STA	restart
1	MSB
1	chip address (Read)
0	
0	
MA0	
MA1	
1	LSB
ACK	
DX	MSB
...	data out X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB
1	
STO	

3W-bus Write Mode

Bit	Function
S7	MSB
S6	sub address (Write) 00H...06H
S5	
S4	
S3	
S2	
S1	
S0	LSB
DX	MSB
...	data in X...0 (X=7,15 or 23)
D5	
D4	
D3	
D2	
D1	
D0	LSB

3W-bus Read Mode

Bit	Function
S7	MSB
S6	sub address (Read) 80H...82H
S5	
S4	
S3	
S2	
S1	
S0	LSB
DX	MSB
...	data out X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB

[1] after each byte an acknowledge is generated.

STA: Start condition, STO: Stop condition, ACK: Acknowledge.

Table 4-11 I²C Short Read Bus Data Format

I²C-bus Read Mode

first read

Bit	Function
STA	
1	MSB
1	chip address (Write)
0	
0	
0	
MA0	
MA1	
0	LSB
ACK	
S7	MSB
S6	sub address (Read) 80H...82H
S5	
S4	
S3	
S2	
S1	
S0	LSB
ACK	
STA	restart
1	MSB
1	chip address (Read)
0	
0	
0	
MA0	
MA1	
1	LSB
ACK	
DX	MSB
...	data out X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB
1	
STO	

The first read must have the same format as a single read :

- *Write chip address* (write)
- *Sub address* (write)
- *Read chip address* (write)
- *Data* (read)

all following read calls to the same register may have the following short read format :

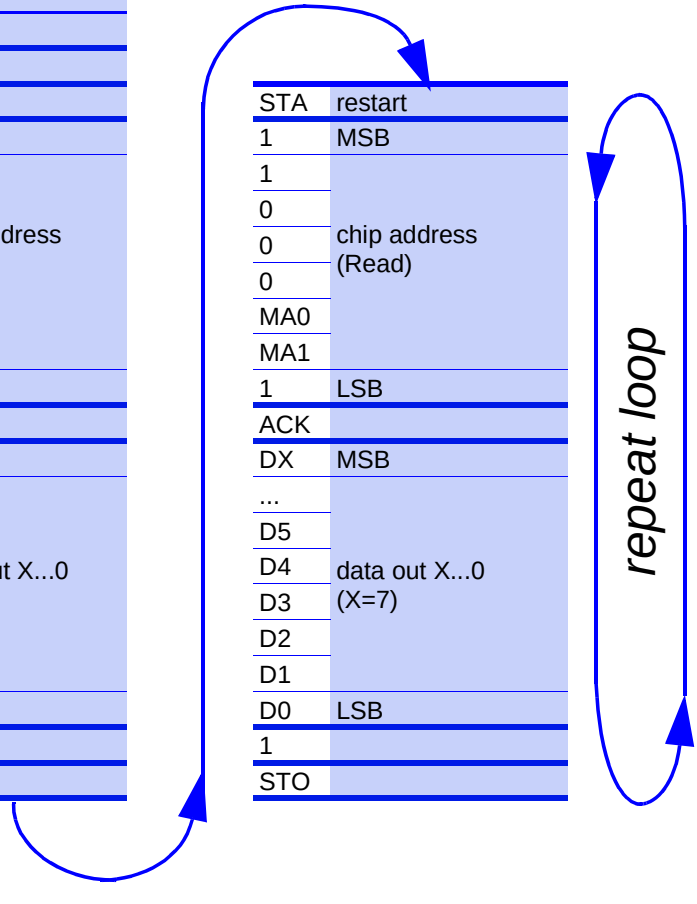
- *Read chip address* (write)
- *Data* (read)

This mode will only be terminated by a new write operation with
- *Write chip address* (write)

repeated short read

to the same register as first read

STA	restart
1	MSB
1	chip address (Read)
0	
0	
0	
MA0	
MA1	
1	LSB
ACK	
DX	MSB
...	data out X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB
1	
STO	



4.4 Write Registers, Data Byte Specification

Table 4-12 Data Byte Specification of Write Data Registers

Register 00
Subaddress 00H
A/N Divider

Bit	Symbol	Bits	V	Function	Description	Defaults
23		1		reserved	must be set to 1	1
22	GV	0		GHz VCO switch	GHz VCO1 is on	0
		1			GHz VCO2 is on	
21	SV	0		Synthesizer VCO switch	Syth. VCO1 is on	
		1			Syth. VCO2 is on	1
20	GN2	GN2 GN1 GN0		GHz PLL N-counter programmable divider bits N = 2 ... 8	Divider ratio	GN2 GN1 GN0
		0 0 0			4	
		0 0 1			2	0 0 1
19	GN1	0 1 0			3	
		0 1 1			4	
		1 0 0			5	
18	GN0	1 0 1			6	
		1 1 0			7	
		1 1 1			8	
17	D17		2^{10}	Synthesizer N-counter programmable divider bits: $N = 2^{10} \times D17 + ... + 2^2 \times D9 + 2^1 \times D8 + D7$ N = 2 ... 2047		0
16	D16		2^9			0
15	D15		2^8			0
14	D14		2^7			0
13	D13		2^6			0
12	D12		2^5			1
11	D11		2^4			0
10	D10		2^3			0
9	D9		2^2			1
8	D8		2^1			1
7	D7		2^0			1
6	D6		2^6	Synthesizer A-counter programmable divider bits: $A = 2^6 \times D6 + ... + 2^2 \times D2 + 2^1 \times D1 + D0$ A = 0 ... 127		0
5	D5		2^5			0
4	D4		2^4			0
3	D3		2^3			0
2	D2		2^2			0
1	D1		2^1			1
0	D0		2^0			0

Default divider ratio N = 39

Default divider ratio A =2

Table 4-12 Data Byte Specification, Write Registers (continued)

Register 01

Subaddress 01H

Reference Divider

Bit	Symbol	Bits			V	Function	Description	Defaults		
15	MOD	0				Prescaler divider ratio	forbidden			
		1					Div. ratio = 32/33	1		
14	CP1	CP1	CP0			Charge-pump current		CP1	CP0	
		0	0				1 mA	0	0	
13	CP0	0	1				1.33 mA			
		1	0				1.66 mA			
		1	1				2 mA			
12	GR2	GR2	GR1	GR0		GHz PLL R-counter programmable divider bits R = 2 ... 8	Divider ratio [1.]	GR2	GR1	GR0
		0	0	0			4			
		0	0	1			2			
11	GR1	0	1	0			3			
		0	1	1			4			
		1	0	0			5			
10	GR0	1	0	1			6			
		1	1	0			7	1	1	0
		1	1	1			8			
9	R9				2^9	Synthesizer R-counter programmable divider bits: $R = 2^9 \times R\,9 + \ldots + 2^2 \times R2 + 2^1 \times R1 + R0$ R = 2 ... 1023		0	Default divider ratio R = 5 [2.]	
8	R8				2^8			0		
7	R7				2^7			0		
6	R6				2^6			0		
5	R5				2^5			0		
4	R4				2^4			0		
3	R3				2^3			0		
2	R2				2^2			1		
1	R1				2^1			0		
0	R0				2^0			1		

[1.] The GHz R/N-counter (register 00 bits 18,19,20; register 01 bits 10,11,12) are Johnson counters which may hang up if they start from a forbidden state. For a 2-3-4-5-6-7-8 counter chain forbidden states can appear at non binary divider values of 3, 5, 6, 7. Whereas the forbidden states in odd counter values correct themselves this will not happen with even counter values. Therefore the remaining counter value of 6 may come into an forbidden state if the programming is switched from a higher value (7 or 8) to 6, because the higher divider values include the forbidden states for counter value of 6.
Therefore **it is an absolute must to program the counter chain to e.g. 5** (which does not include forbidden states for 6) **before it is set from higher values to 6**. If this is not done a proper operation of the TUA6120 cannot be guaranteed.

[2.] Reference frequency is 800 kHz with a 4 MHz crystal.

Table 4-12 Data Byte Specification of Write Data Registers (continued)

Register 02

Subaddress 02H

Control Bytes

Bit	Symbol	Bits	V	Function	Description	Defaults
15	FL1	0		Lock Flag control if FL0 = 1[1]	Lock Flag at P0	0
		1			Lock Flag at P1	
14	FL0	0		Lock detect output as selected by FL1[1]	Lock Flag not at port	0
		1			Lock Flag at port	
13	AGCP	0		AGC polarity [2]	positive AGC slope	0
		1			negative AGC slope	
12	AC4		2^4	AGC ADC clock control divider ratio AC = 2^4 * AC4+...+ 2^1 *AC1+ AC0, AC = 1 ... 31	ADC clock for AGC = Crystal frequency / ADC clock divider ratio AGC,ADC cycle time = 1/9 of ADC clock	0 1 0 0 0
11	AC3		2^3			
10	AC2		2^2			
9	AC1		2^1			
8	AC0		2^0			Default divider ratio AC = 8
7	ST1	ST1 ST0		Stand-by and Loop-thru control		ST1 ST0
		0 0			Normal mode	0 0
		0 1			Normal mode, but loop thru off	
6	ST0	1 0			Stand-by but LNA and loop-thru on	
		1 1			Total stand-by	
5	QB1	QB1 QB0		XTAL I/O control		QB1 QB0
		0 0			XTAL is input	0 1
		0 1			Output level = 1.8 V_{pp}	
4	QB0	1 0			Output level = 2.6 V_{pp}	
		1 1			Output level = 3.3 V_{pp}	
3	QIL	0		Quartz I/O input level	Preamp = off	0
		1			Preamp = on [3]	
2	PDP	0		Phase-detector polarity control	Polarity = negative	1
		1			Polarity = positive	
1	CPT	0		Charge-pump control [4]	Charge-pump = on	0
		1			Charge-pump = off	
0	OS	0		LPF1OUT on/off	LPF1OUT = off	0
		1			LPF1OUT = on	

[1] Port is switched to tristate if used as lock flag output. The port sinks current if the flag is set.

[2] Only valid if AGC is external, otherwise **Table "Register 04" on Page 51**

[3] Preamp = on is only allowed if XTAL I/O control is input (register 02, bits 4,5 = 0)
more **Table "XTALIO input" on Page 42**

[4] If not in test mode, otherwise **Table "Register 06" on Page 53**.

Table 4-12 Data Byte Specification of Write Data Registers (continued)

Register 03
Subaddress 03H
Port Byte

Bit	Symbol	Bits	V	Function	Description	Defaults
7	P7			not used		0
6	P6					0
5	P5					0
4	P4					0
3	P3					0
2	P2					0
1	P1	0		Port control	Port 1 current is off	0
		1			Port 1 current is on	
0	P0	0			Port 0 current is off	0
		1			Port 0 current is on	

Register 04
Subaddress 04H
AGC Mode

Bit	Symbol	Bits		V	Function	Description	Defaults	
7	AI1	AI1	AI0		AGC current	I_{source} = 20 µA = constant	AI1	AI0
6	AI0	0	0			I_{sink} = 150 nA	0	0
		0	1			I_{sink} = 300 nA		
		1	0			I_{sink} = 450 nA		
		1	1			I_{sink} = 600 nA		
5	AL3				AGC control	if AL3 = 1, AL2 = 1, AL1 = 1, AL0 = 0: AGC is external, otherwise AGC is internal	0	
4	AL2						0	
3	AL1						0	
2	AL0						0	
1	not used						0	
0							0	

Table 4-12 Data Byte Specification of Write Data Registers (continued)

Register 05

Subaddress 05H

Baseband Control

Bit	Symbol	Bits			V	Function	Description	Defaults		
7						not used		0		
6	F1	F1	F0			Base-band filter roll-off		F1	F0	
		0	0				Full bandwidth	0	0	
		0	1				11 MHz			
5	F0	1	0				33 MHz			
		1	1				22 MHz			
4	ED	0				Base-band amplifier control	BB amps = on	0		
		1					BB amps = off			
3	GA2	GA2	GA1	GA0		I/Q output level, differential		GA2	GA1	GA0
		0	0	0			0.5 V_{pp}			
		0	0	1			0.75 V_{pp}			
2	GA1	0	1	0			1.0 V_{pp}	0	1	0
		0	1	1			1.25 V_{pp}			
		1	0	0			1.5 V_{pp}			
1	GA0	1	0	1			1.75 V_{pp}			
		1	1	0			2.0 V_{pp}			
		1	1	1			not used			
0	XO	0				Xtal output control	Xtal output = on	0		
		1					Xtal output = off			

Table 4-12 Data Byte Specification of Write Data Registers (continued)

Register 06

Subaddress 06H

Test Modes

Bit	Symbol	Bits		V	Function	Description	Defaults		
7	not used						0		
6	ABL2	ABL 2	ABL 1		ABL pulse for phase detector [1]		ABL 2	ABL 1	
		0	0			1.7 ns			
5	ABL1	0	1			2.5 ns	0	1	
		1	0			3.8 ns			
		1	1			5.8 ns			
4	CPM	0			Charge-pump control	Charge-pump = bipolar			0
		1				Charge-pump = monopolar			
3	CPP	0				Charge-pump = sinking current, if CPM = 1			0
		1				Charge-pump = sourcing current if CPM = 1			
2	CPT	0				Charge-pump = on			0
		1				Charge-pump = off (tristate)			
1	PIO	0			Test frequency control	P0, P1 are input for f_{ref}, f_{div} [2]			
		1				P0, P1 are output for f_{ref}, f_{div}			1
0	TED	0			Testmode control	Testmode disabled			0
		1				Testmode enabled			

[1] ABL bits are independent of testmode control bit TED.

[2] I/O for f_{ref} is P0, I/O for f_{div} is P1. f_{ref} is the output frequency of the R-counter and f_{div} the output frequency of theN-counter.

4.5 Read Registers, Data Byte Specification

Table 4-13 Data Byte Specification of Read Data Registers

Register 80
Subaddress 80H
Status

Bit	Symbol	Bits		Function	Description	Defaults
7	POR			power-on flag[1)]	POR = 1 if power-on reset	
6	FL			lock-in flag	FL = 1 if loop is locked	
5	STBY3			stand-by flag 3	STBY3 = 0 if loop through is on. Default is loop through on	
4	STBY2			stand-by flag 2	STBY2 = 0 if LNA is on. Default is LNA on	
3	STBY1			stand-by flag 1	STBY1=0 if direct converter is on. Default is direct converter on	
2	AGC			AGC flag	AGC = 1 if AGC is external. As default AGC is in internal mode	
1				not used		1
0						1

[1)] The power-on flag is reset after a read operation.

Register 82
Subaddress 82H
RSSI

Bit	Symbol	Bits		Function	Description	Defaults	
7	RS7		2^7	RSSI (Field-strength indicator) RSSI = 0 ... 127	RSSI = 2^7x RS7+ 2^6x RS6+...+ 2^1x RS1	0	without input signal
6	RS6		2^6			0	
5	RS5		2^5			0	
4	RS4		2^4			0	
3	RS3		2^3			0	
2	RS2		2^2			0	
1	RS1		2^1			0	
0	RS0		2^0	not used		0	

4.6 VCO band switching table

Table 4-14 VCO band switching

Band	f_{RFIN} [MHz]	Synth. VCO[1)]	SV bit 1)	GHz VCO 1)	GV bit 1)	GHz N-divider ratio 1)	GHz R-divider ratio 2)	GHz N-counter 1)			GHz R-counter 2)		
								GN2	GN1	GN0	GR2	GR1	GR0
1	915	2	1	1	0	2	8	0	0	1	1	1	1
	935												
2	935	1	0				7				1	1	0
	1000												
3	1000	2	1										
	1080												
4	1080	1	0				6				1	0	1
	1167												
5	1167	2	1										
	1255												
6	1255	1	0			3	8	0	1	0	1	1	1
	1313												
7	1313	2	1										
	1415												
8	1415	1	0				7				1	1	0
	1500												
9	***1500***	2	1	2	1		6				1	0	1
	1615												
10	1615	1	0										
	1750												
11	1750	2	1				7	0	1	1	1	1	0
	1885												
12	1885	1	0			4							
	2000												
13	2000	2	1										
	2155												
14	2155	1	0				6				1	0	1
	2185												

1) see Register 00 on page 48.

2) see Register 01 on page 49.

Remark: The total input frequency range is divided into 14 bands. The crossover frequency of the GHz VCO's, 1500 MHz, is in ***bold italic*** letters. After power-on the band 3 is selected as default.

4.7 VCO band splitting

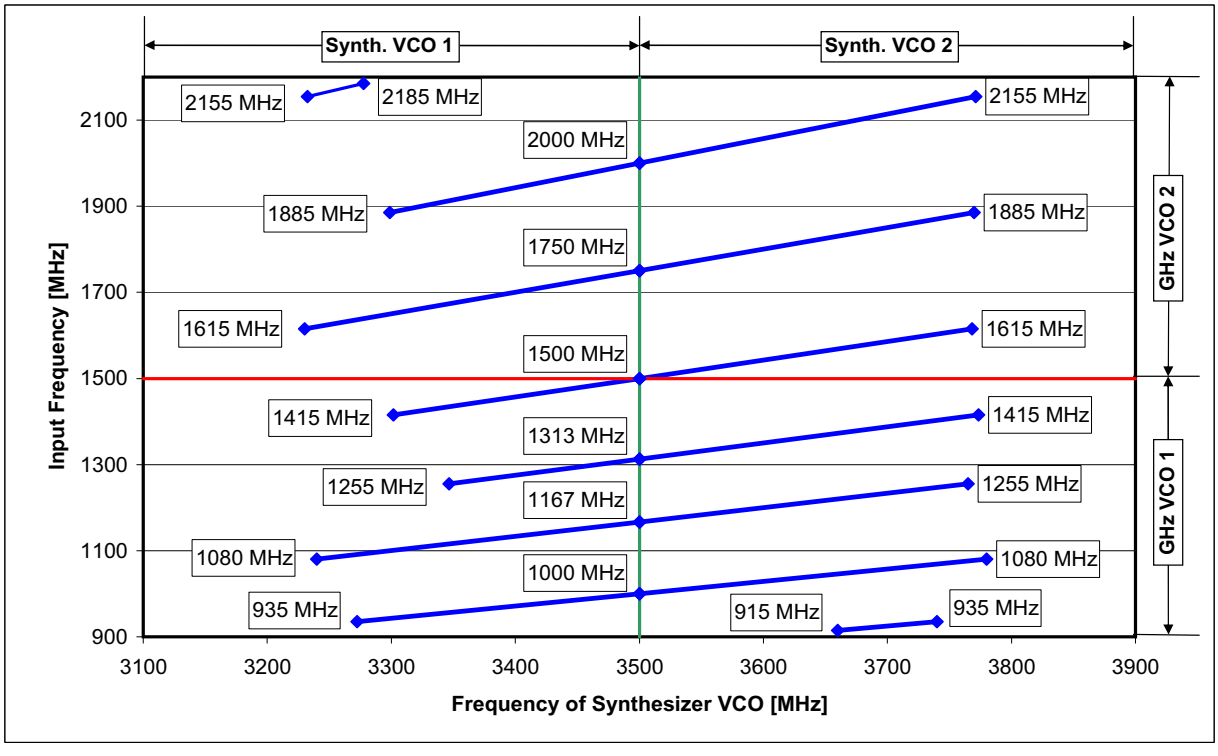


Figure 4-1 VCO band splitting

4.8 Bus Timing

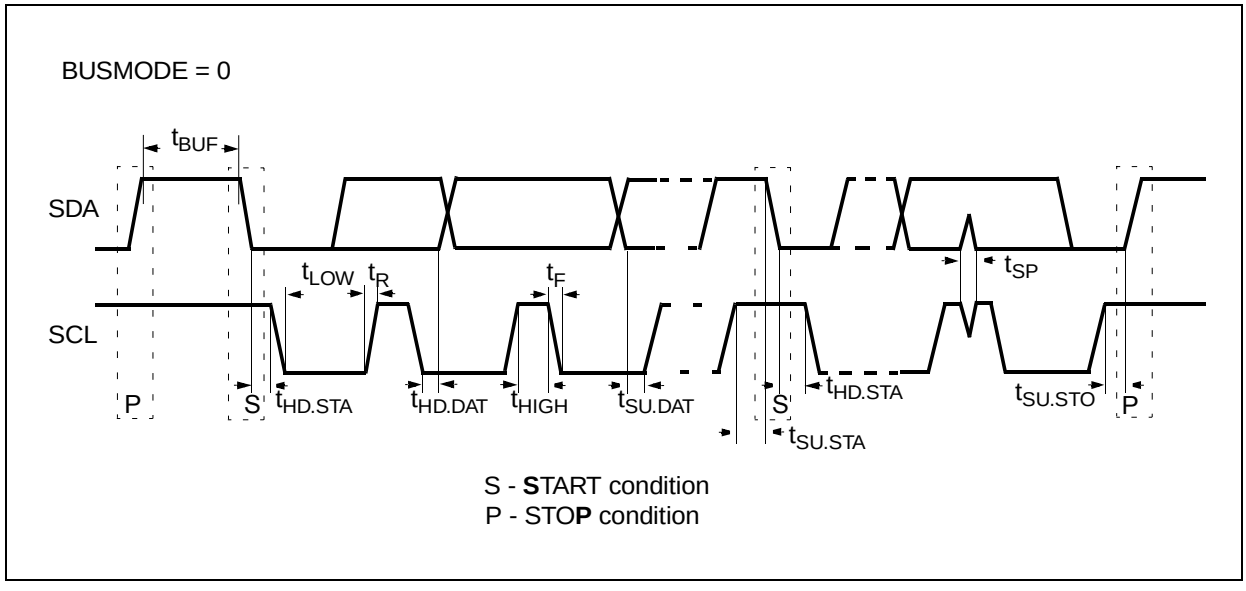


Figure 4-2 I²C Bus

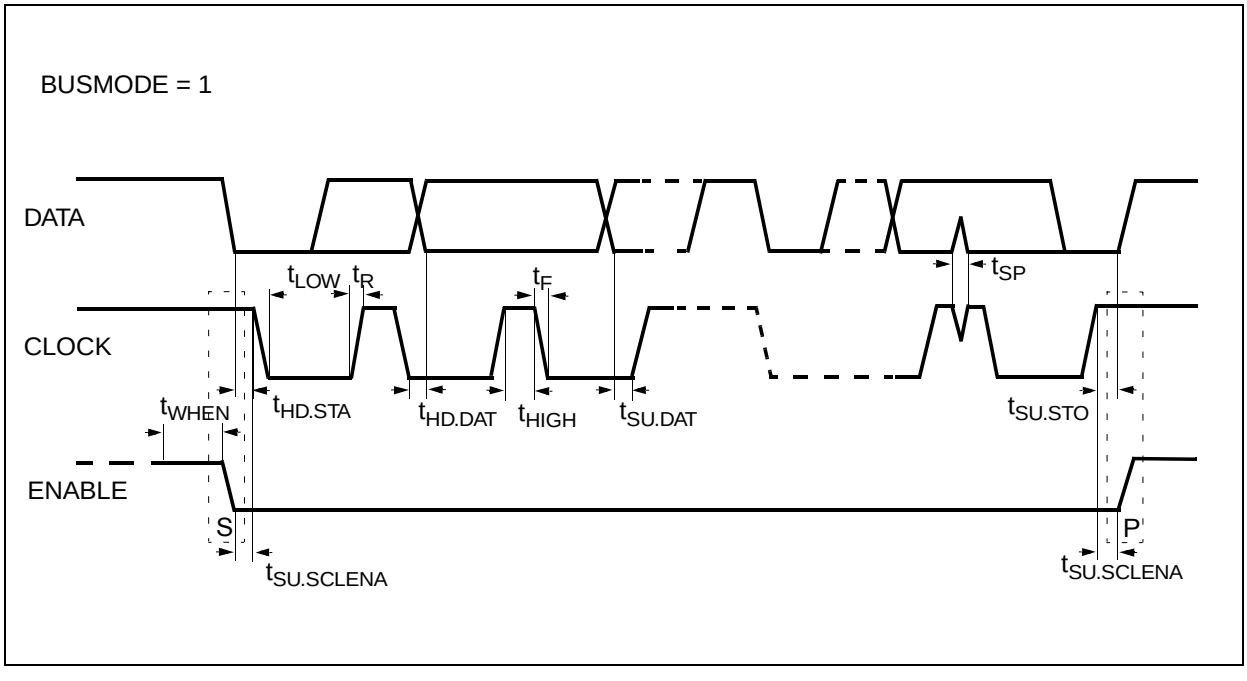


Figure 4-3 3-Wire Bus

Table 4-15 Bus Timing

No	Parameter	Symbol	Limit Values min	Limit Values max	Unit
1	LOW level input voltage (SDA, SCL, CAS/EN, BUSMODE)	V_{IL}	-0.5	0.71	V
2	HIGH level input voltage (SDA, SCL, CAS/EN, BUSMODE)	V_{IH}	1.3	5.5	V
3	Hysteresis of Schmitt trigger inputs	V_{Hys}	0.2		V
4	Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
5	LOW level output voltage (SDA), only I2C-bus at 3mA sink current at 6mA sink current	V_{OL}	0	0.4 0.6	V V
6	Output fall time from $V_{IH\ min}$ to $V_{IL\ max}$ with a bus capacitance from 10pF to 400pF with up to 3mA sink current at V_{OL}	t_{OF}	$20+0.1C_b$ [1)]	250	ns
7	SCL clock frequency	f_{SCL}	0	400	kHz
8	Bus free time between a STOP and START condition [2)]	t_{BUF}	1.3	-	µs
9	Hold time (repeated) START/ENABLE ON condition. After this period, the first clock pulse is generated.	$t_{HD.STA}$	0.6	-	µs
10	LOW period of the SCL clock pulse	t_{LOW}	1.3	-	µs
11	HIGH period of the SCL clock pulse	t_{HIGH}	0.6	-	µs
12	Set-up time for a repeated START condition 2)	$t_{SU.STA}$	0.6	-	µs
13	Data hold time	$t_{HD.DAT}$	0		ns
14	Data set-up time	$t_{SU.DAT}$	100	-	ns
15	Rise time, fall time of SDA and SCL signals	t_R, t_F	$20+0.1C_b$1)	300	ns
16	Set-up time for STOP/ENABLE OFF condition	$t_{SU.STO}$	0.6	-	µs
17	Setup time SCL to CAS/EN	$t_{SU.SCLENA}$	0.6	-	µs
18	H-pulse width (CAS/EN) for new data protocol [3)]	t_{WHEN}	0.6	-	µs
19	Capacitive load for each bus line	C_b	--	400	pF

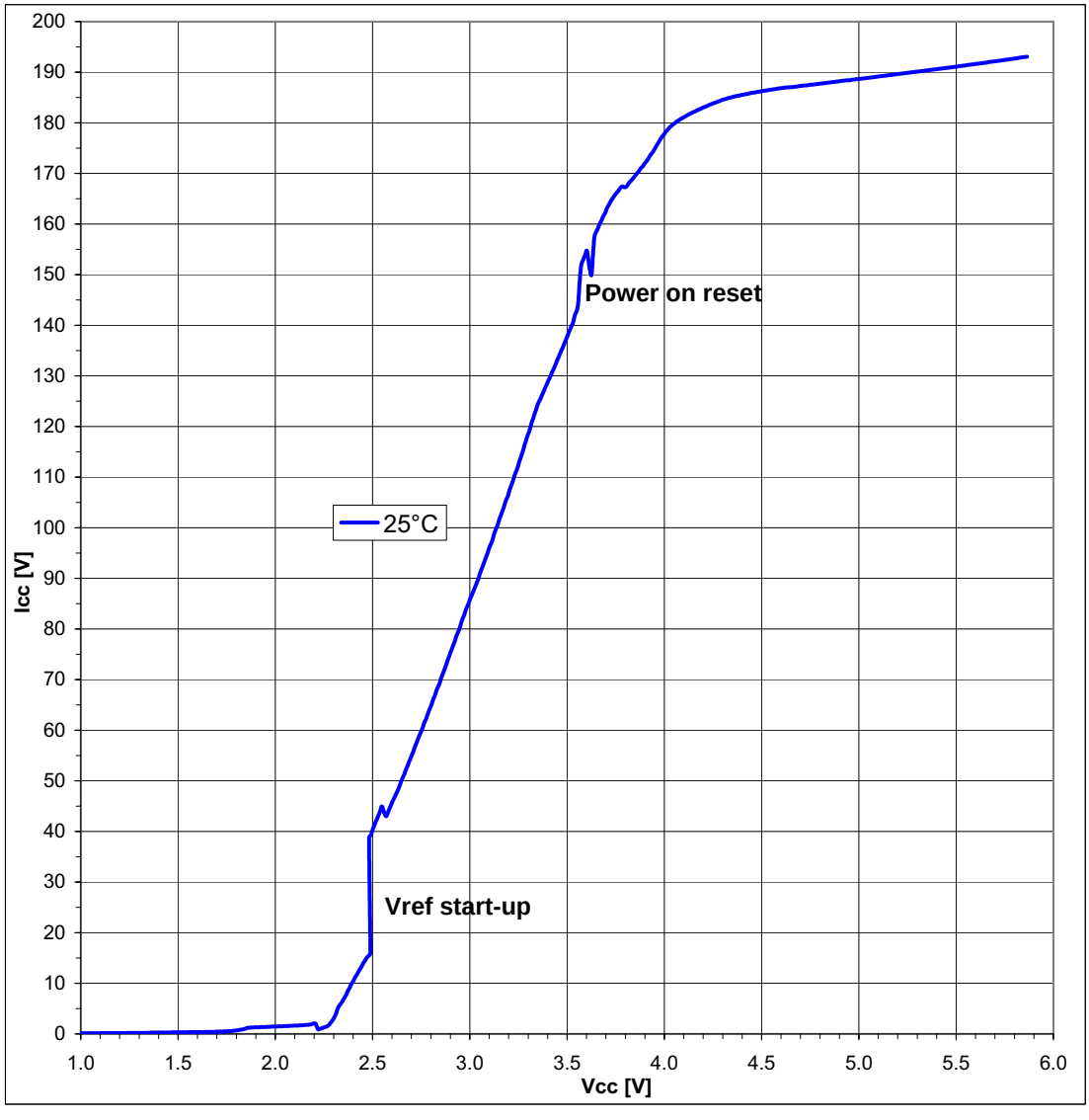
1) C_b = capacitance of one bus line in pF.
Note that the maximum t_F for the SDA and SCL bus lines quoted in table above (300ns) is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

2) only for I^2C bus mode.

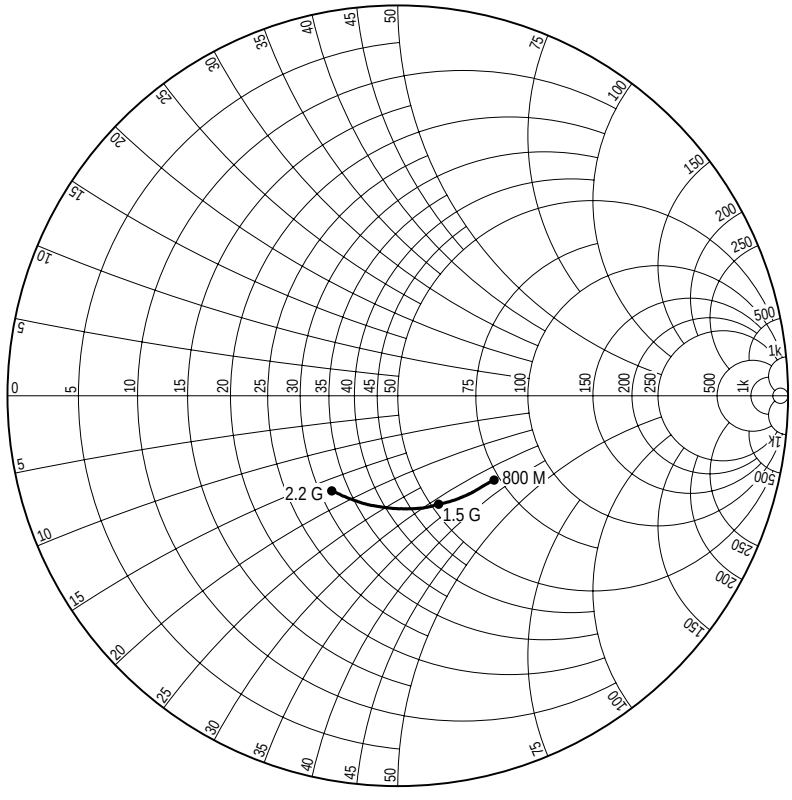
4.9 Electrical Diagrams

4.9.1 Current consumption vs. Vcc

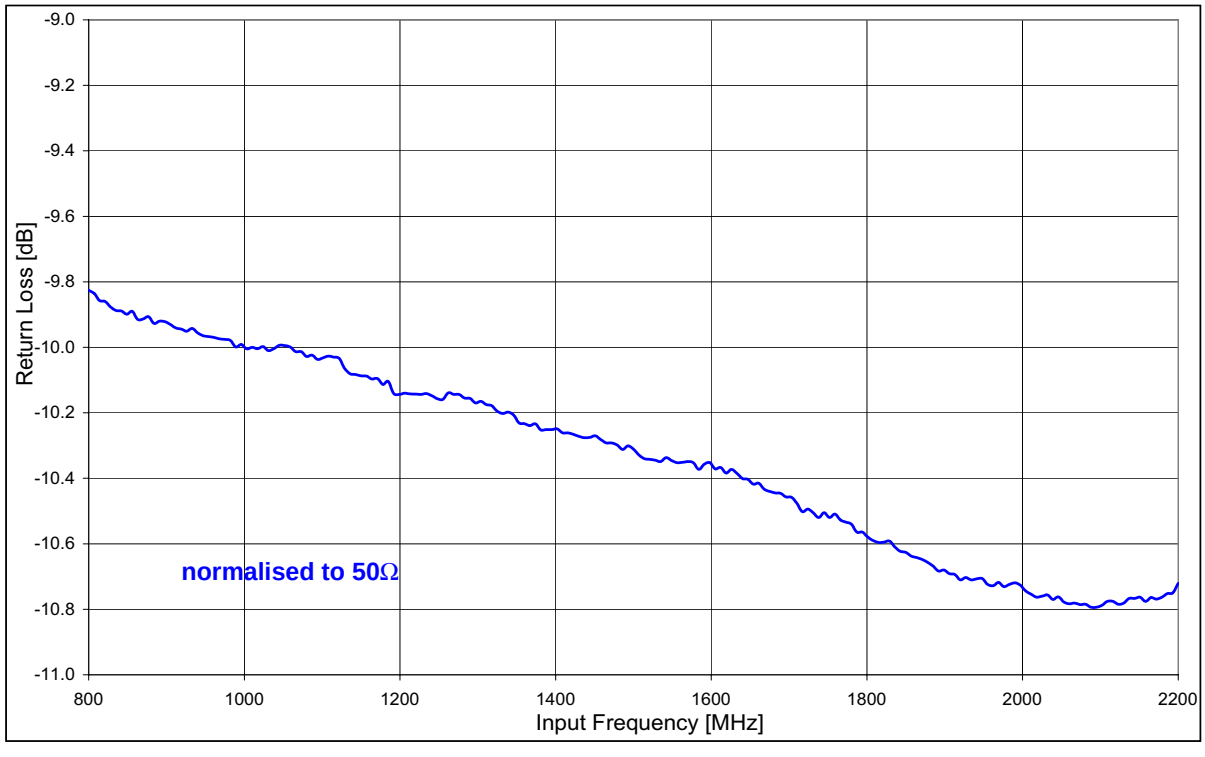
In this measurement the TUA6120 starts with the power on reset settings.
PLL tuned to 1000 MHz (Crystal = 4MHz, Fref = 800kHz), Baseband filter off,
other settings see 4.4 Write Registers, Data Byte Specification on page 48.



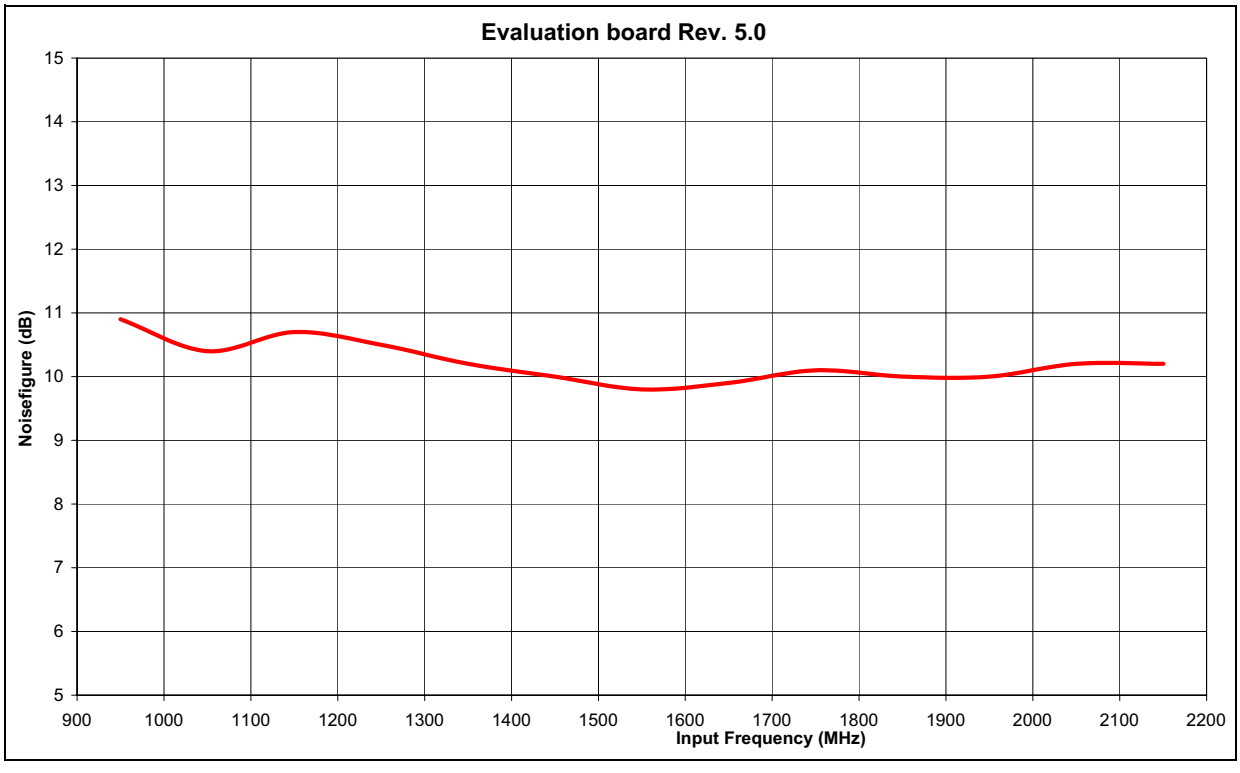
4.9.2 RF input impedance, Smith diagram



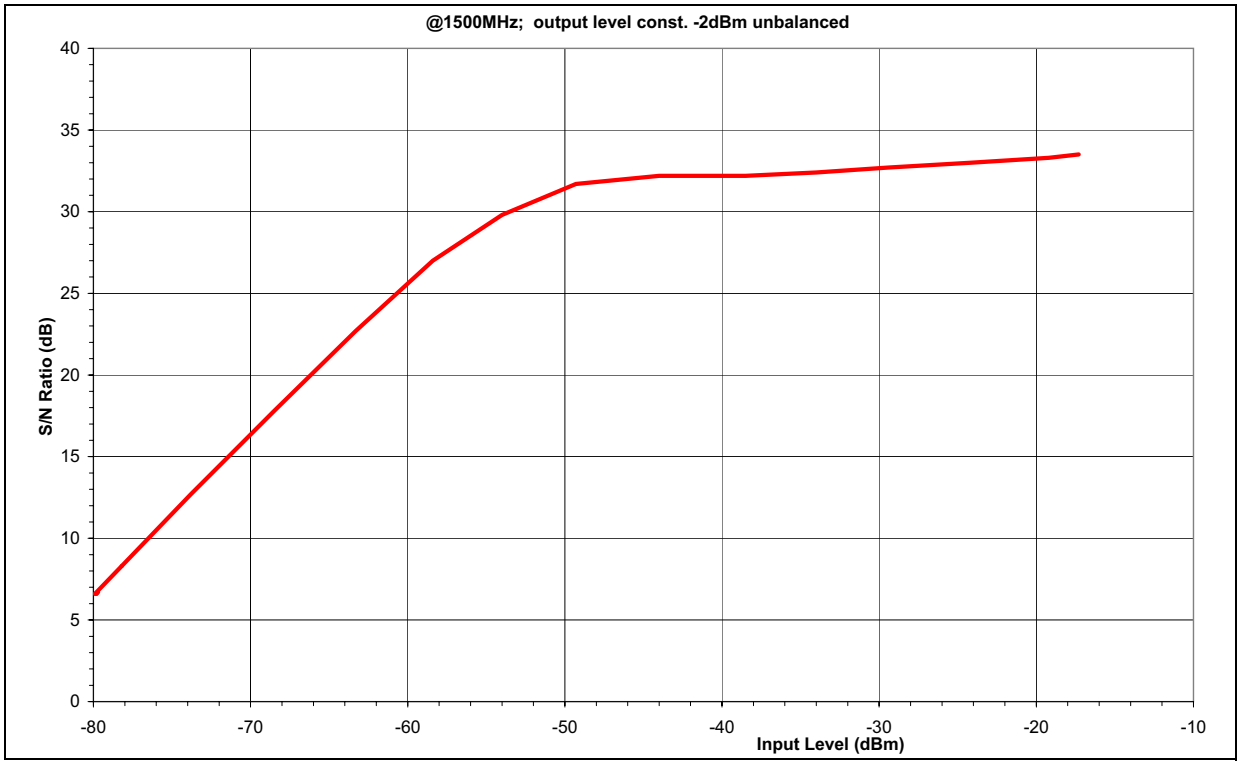
4.9.3 RF input return loss vs. input frequency



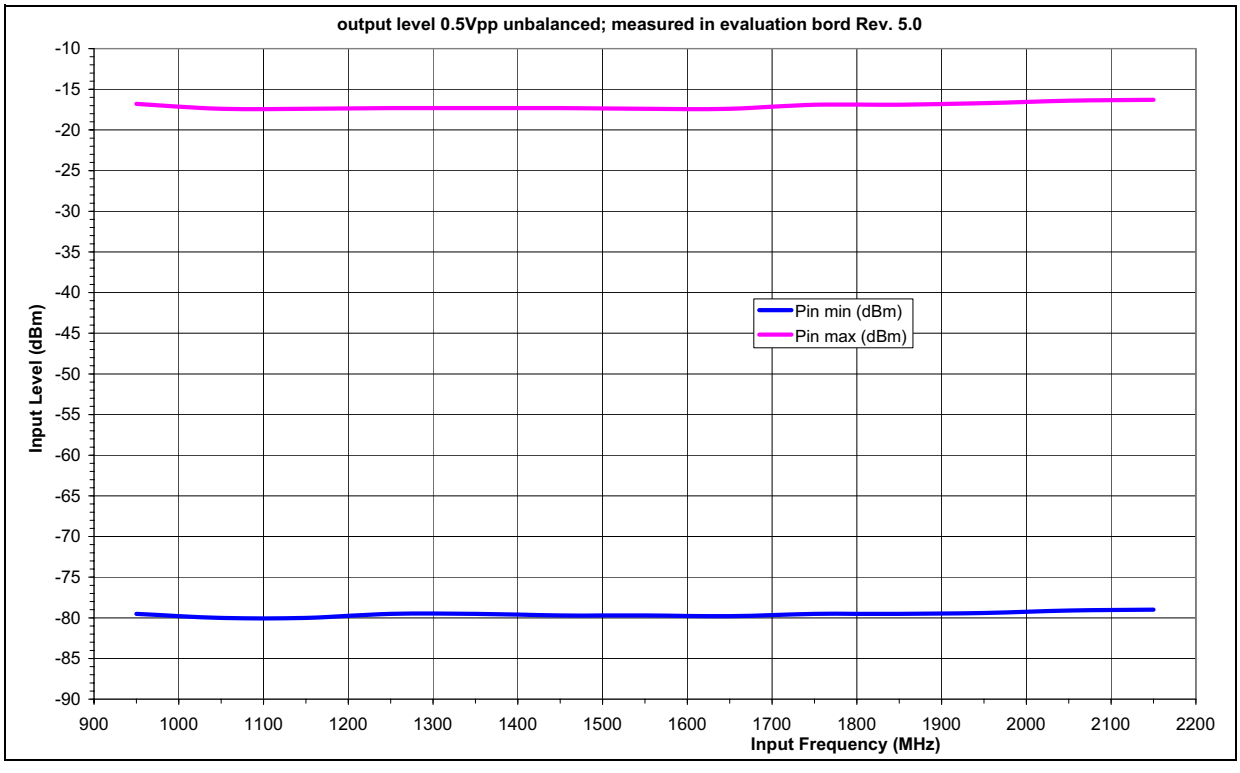
4.9.4 Noise figure vs. input frequency



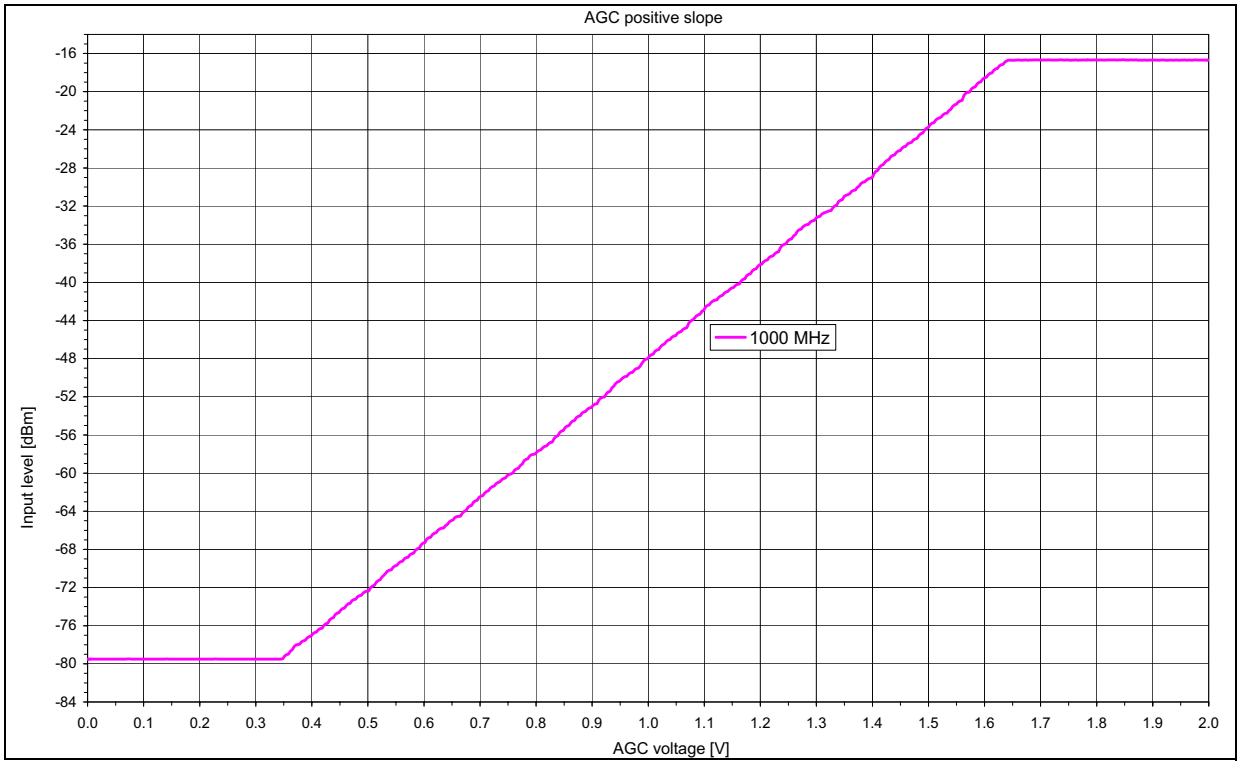
4.9.5 S/N vs. input level



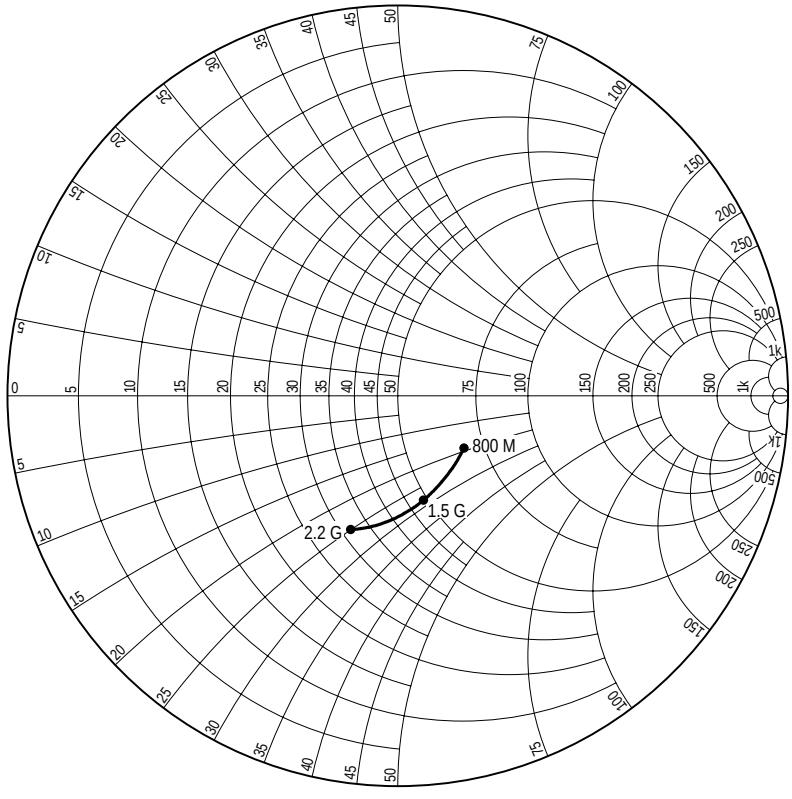
4.9.6 RF input range



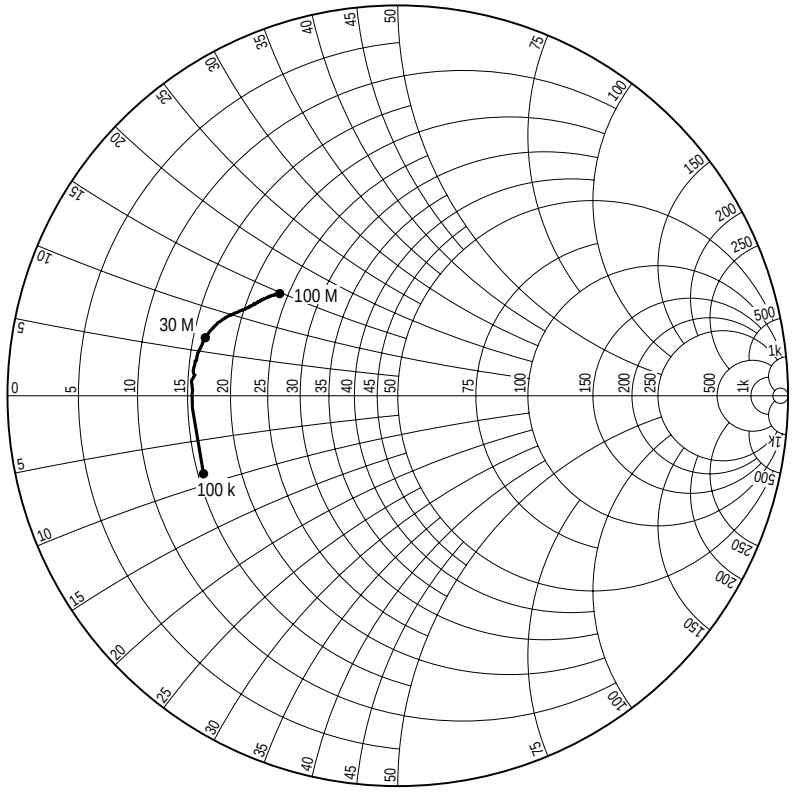
4.9.7 Input level vs. AGC voltage



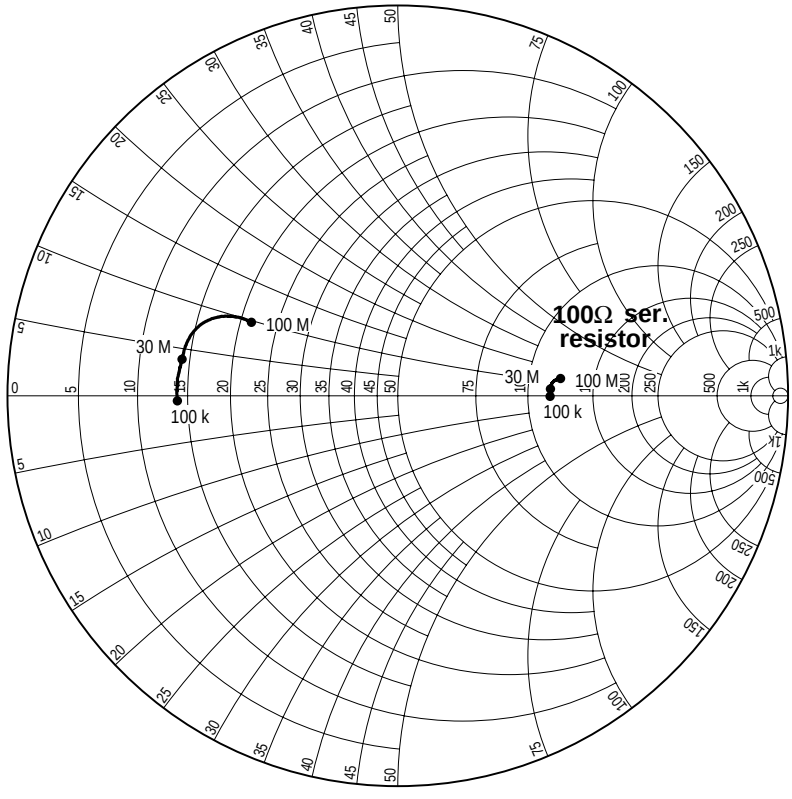
4.9.8 RF output impedance, Smith diagram



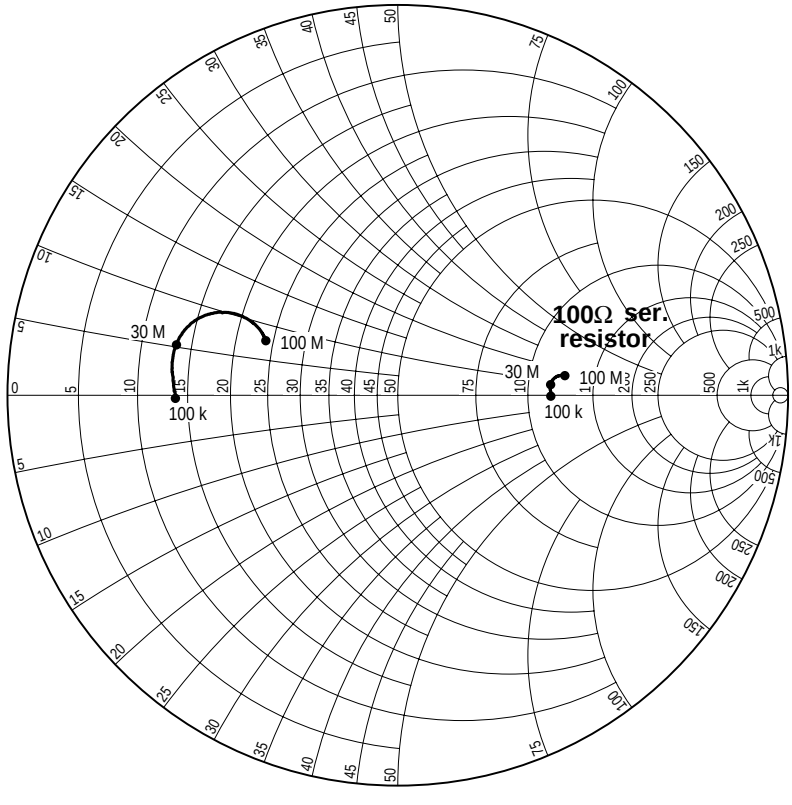
4.9.9 1. Baseband output impedance, Smith diagram



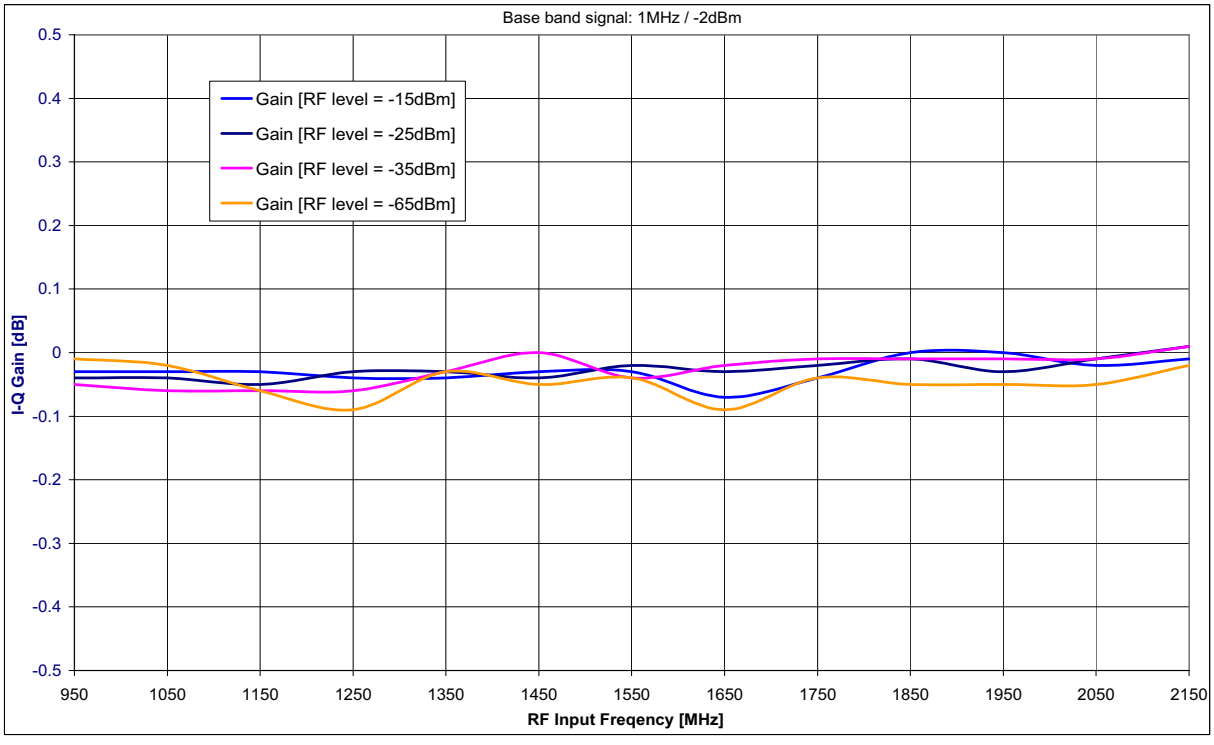
4.9.10 2. Baseband output impedance, Smith diagram

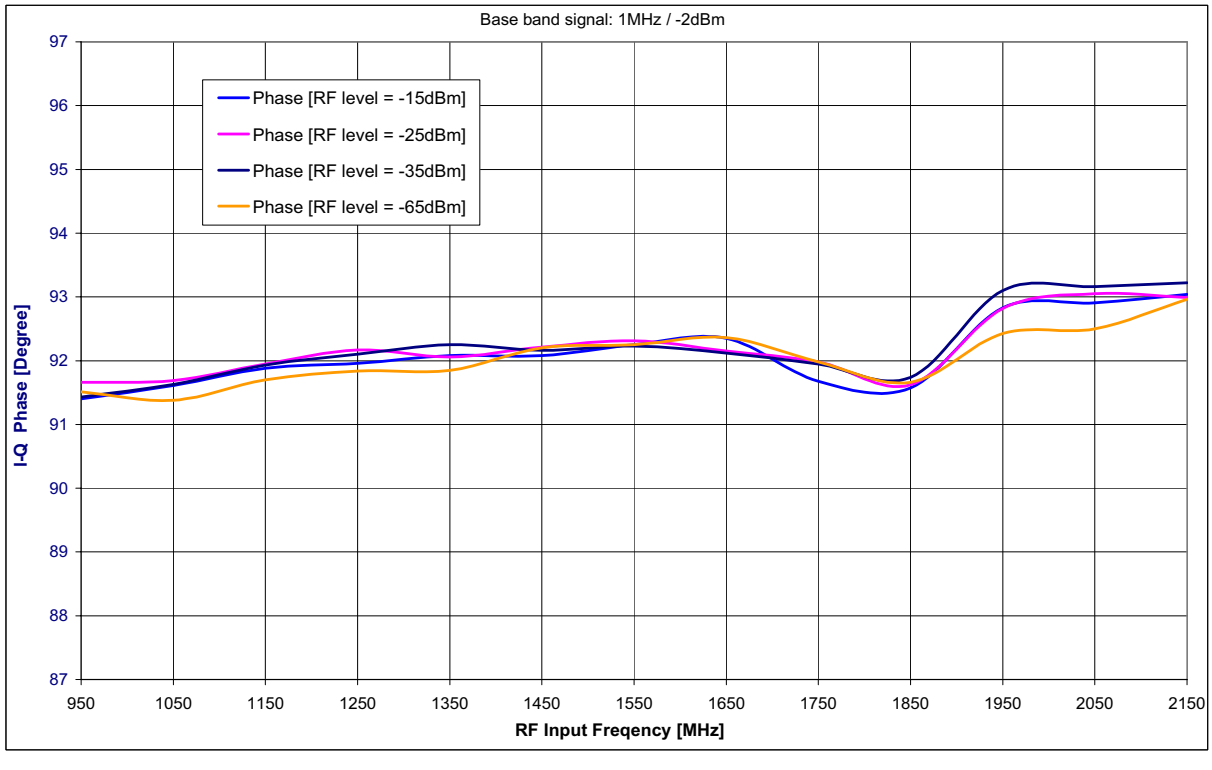


4.9.11 2. Baseband output-inverted impedance, Smith diagram

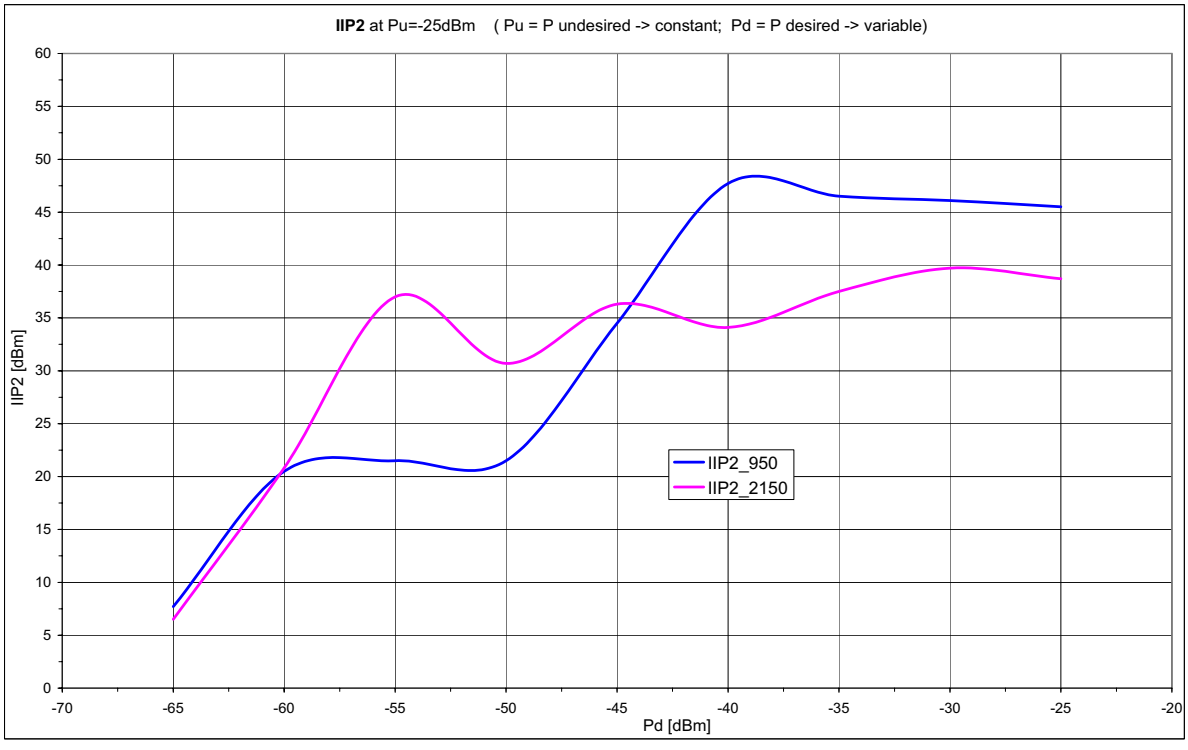


4.9.12 I-Q Impairments

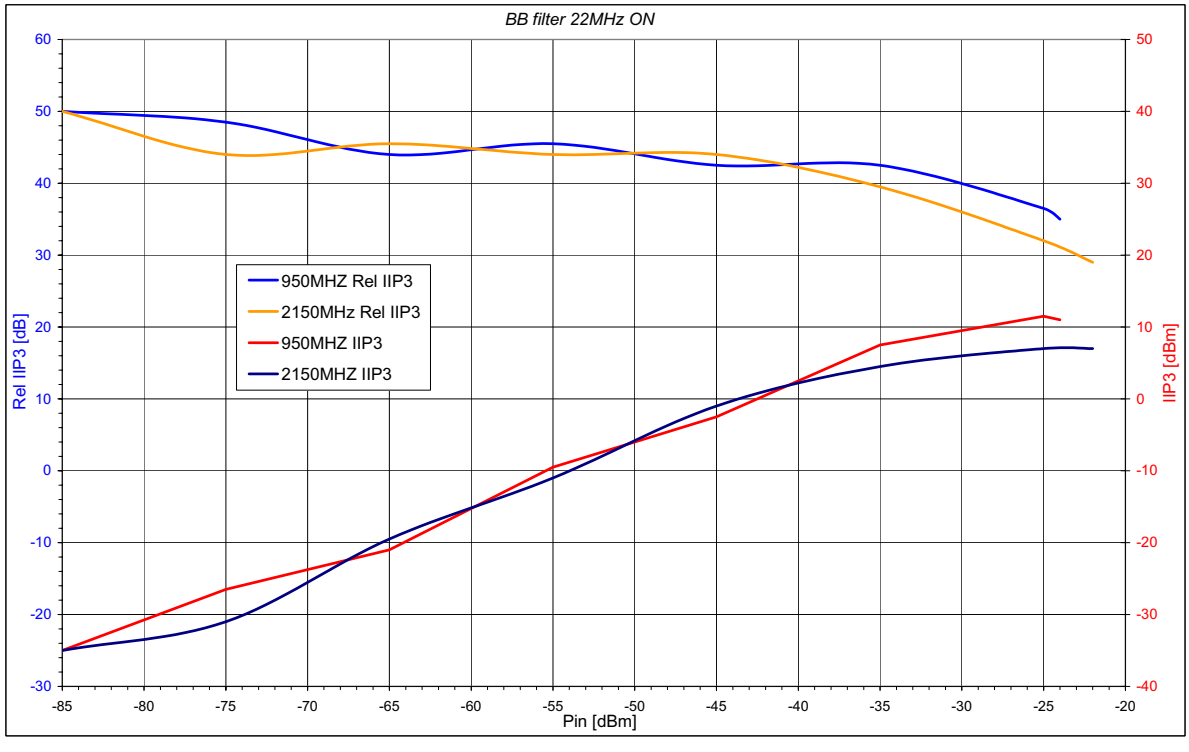




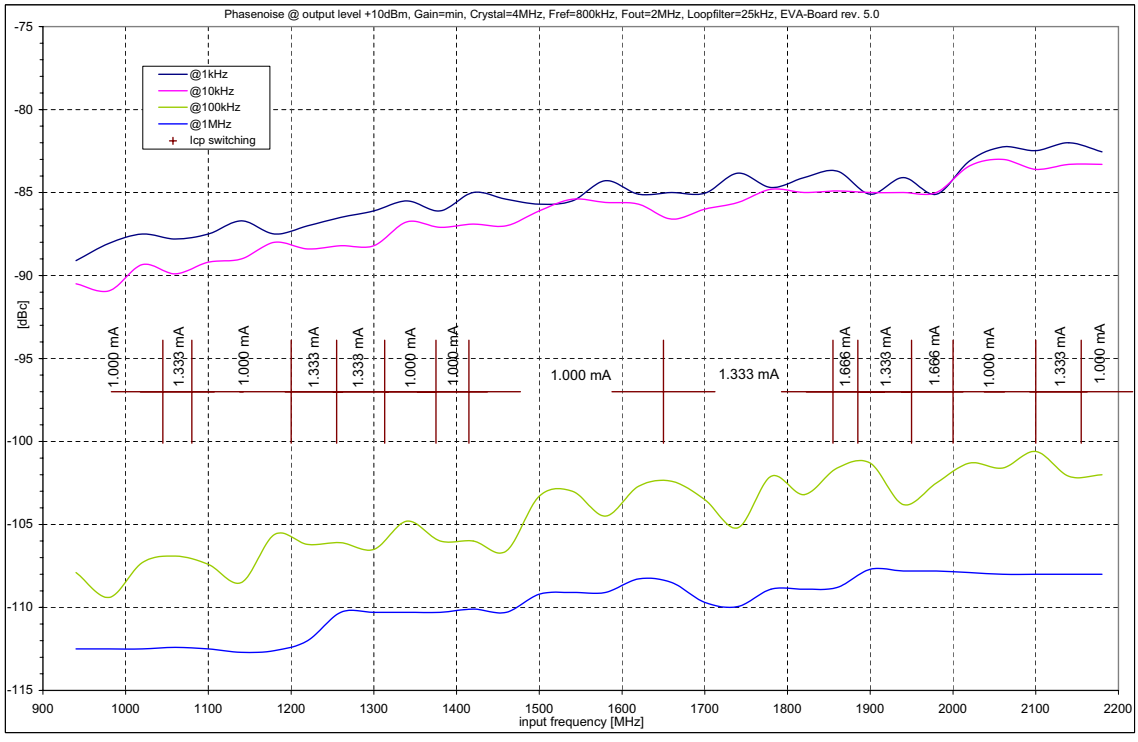
4.9.13 Second order intermodulation input related (IIP2)



4.9.14 Third order intermodulation input related (IIP3)

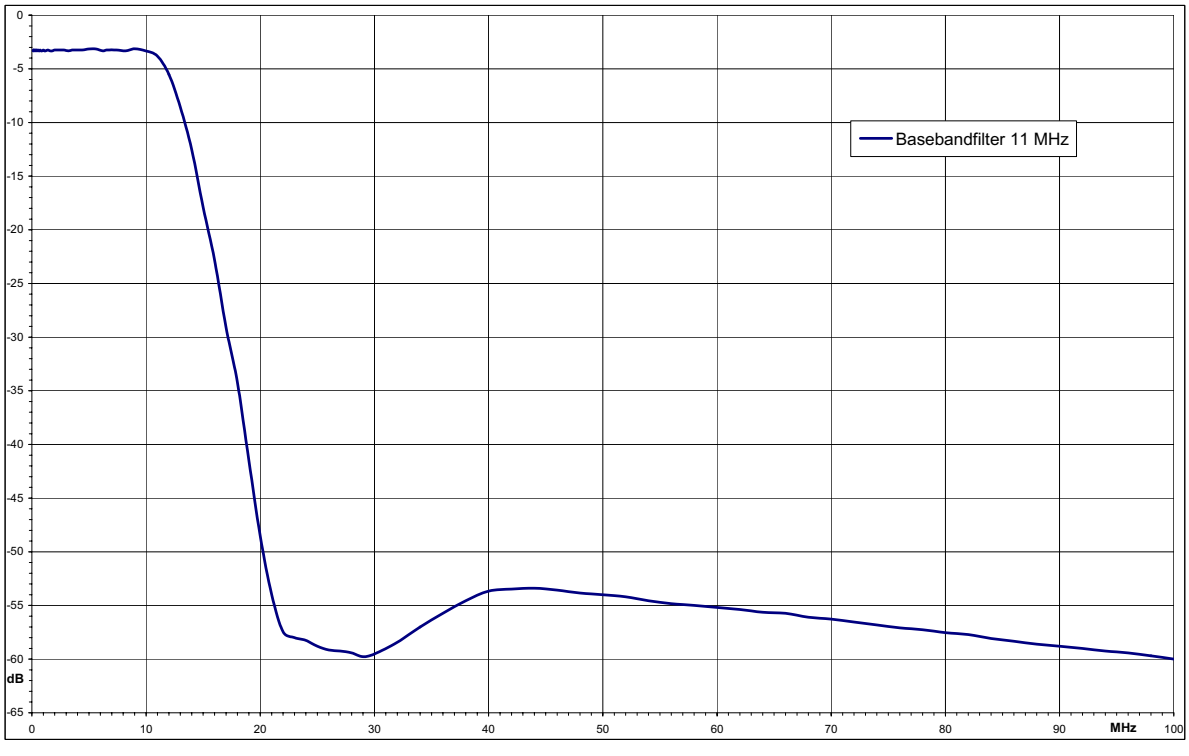


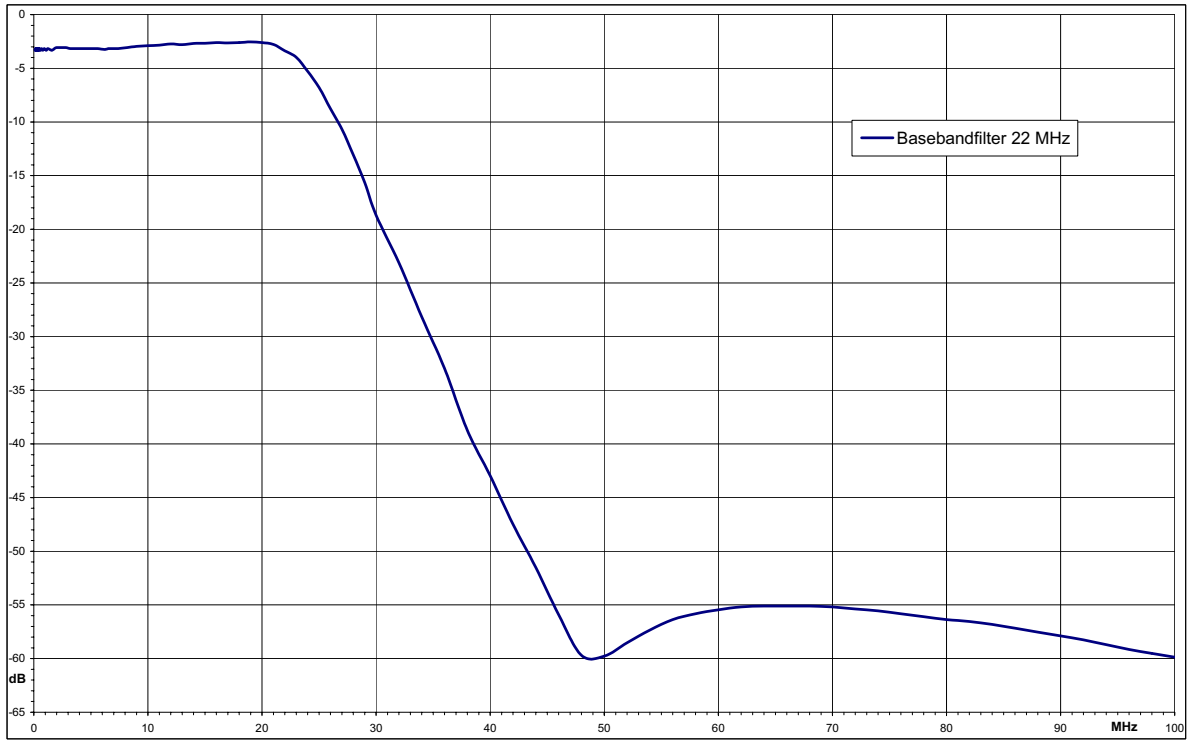
4.9.15 Phasenoise

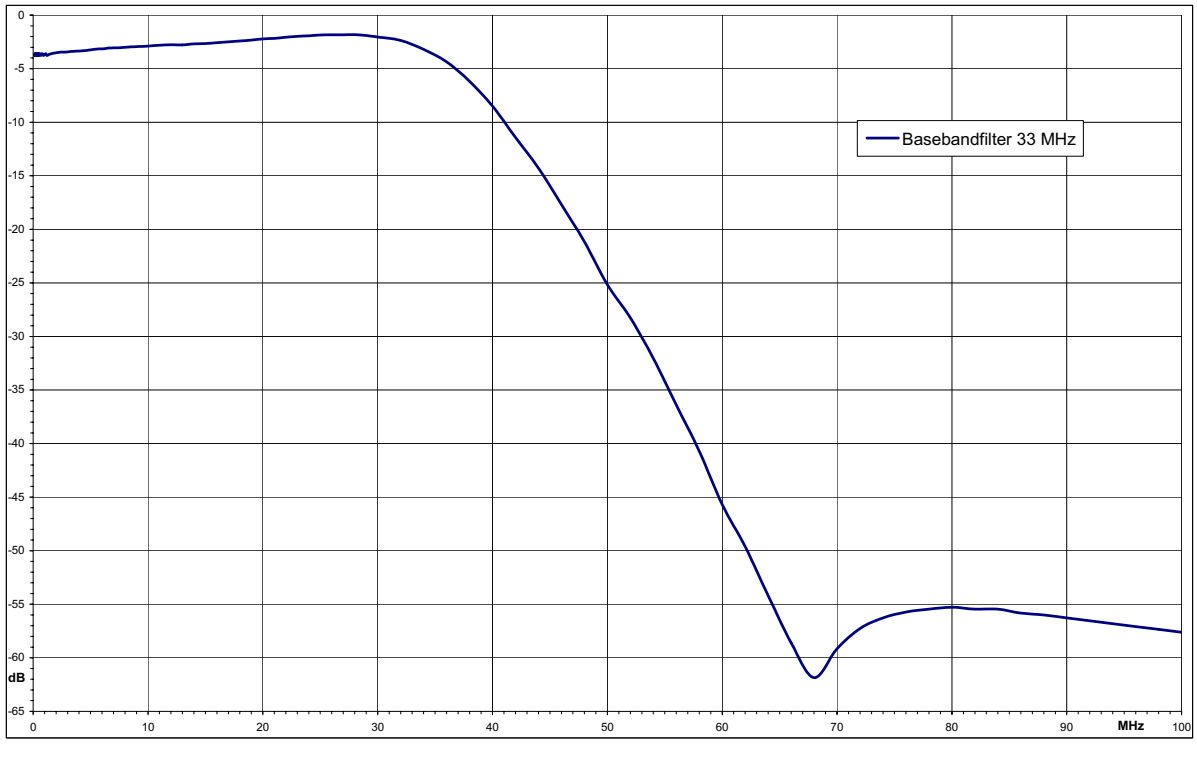


4.9.16 Frequency response of base band filter

both base band amplifiers in series, coupling capacitor 220 nF




Basebandfilter 22 MHz
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
dB
0
10
20
30
40
50
60
70
80
90
100
MHz


Basebandfilter 33 MHz
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
dB
0
10
20
30
40
50
60
70
80
90
100
MHz

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