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ML6411

Programmable Video Digitizer with Selectable Gain and Clamps
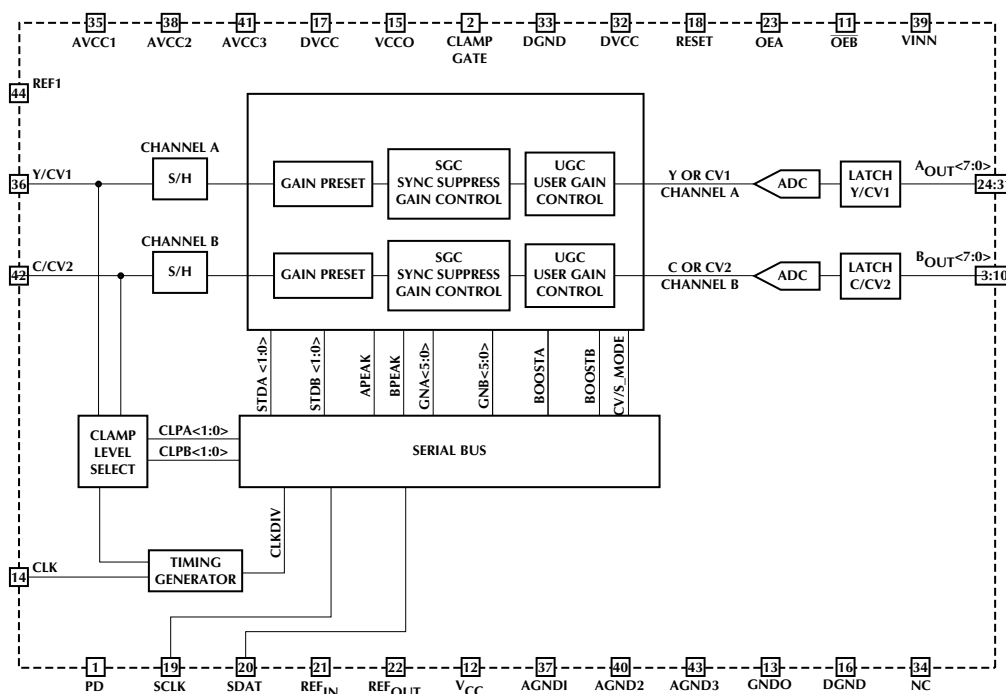
GENERAL DESCRIPTION

The ML6411 is a Dual Video A/D converter, incorporating two input sample and holds, two high speed 8-Bit A/D converters, programmable gain control, selectable clamps, multi-phase clocking, and reference voltage generation. The ML6411 can be used to convert the following analog signals to digital signals: two composite channels or S-video channel.

All inputs are provided with appropriate input selectable clamps to establish DC level. The clamps are full DC restore circuits with the A-to-D converters in each respective correction loop. The clamps are selectable to 16, 24, 64, and 128. The programmable gain control provides various possibilities to select and adjust the gain via two separate mechanisms: Sync-Suppressed Gain Control (SGC) for sync suppressed video such as RGB, and User Gain Control (UGC) for video formats that require scalable gain settings. Each of these can be programmed through a serial bus.
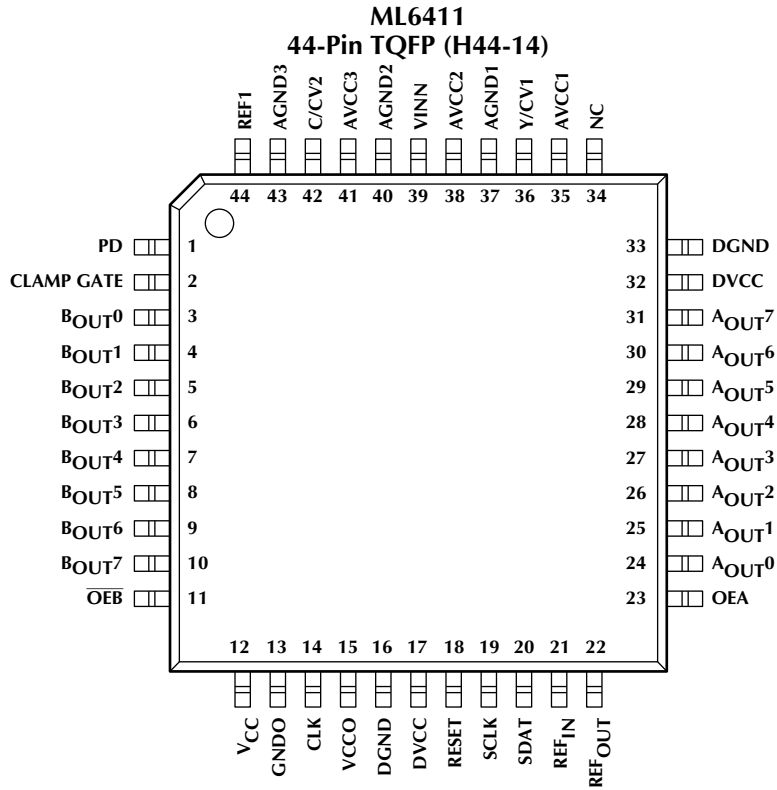
FEATURES

■ Complete video digitizer for Y/C and CV video

■ Contains A/D's with scalable gain, selectable clamps, and clock generation (programmable via serial bus)

■ Two 8-Bit +/- ½ LSB Differential Non-Linearity with 30MHz guaranteed conversion

■ Two Gain Control Mechanisms for programmable or sync-suppressed video gain control

■ Selectable Video Clamping: 16, 24, 64, 128

■ Selectable Video Gain: 3dB to –6dB

■ Operating total power dissipation less than 425mW

■ Power down mode and Tri-state output control

■ Applications: Video Capture, Video Editing, Video Cameras, Y/C and CV analog to digital conversion

■ 44-pin TQFP

BLOCK DIAGRAM

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PIN CONFIGURATION

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44-Pin TQFP (H44-14)

Top pins (left to right, 44–34): REF1, AGND3, C/CV2, AVCC3, AGND2, VINN, AVCC2, AGND1, Y/CV1, AVCC1, NC

Left side pins (top to bottom):
Pin	Signal
1	PD
2	CLAMP GATE
3	$B_{OUT}0$
4	$B_{OUT}1$
5	$B_{OUT}2$
6	$B_{OUT}3$
7	$B_{OUT}4$
8	$B_{OUT}5$
9	$B_{OUT}6$
10	$B_{OUT}7$
11	$\overline{OEB}$

Right side pins (top to bottom):
Pin	Signal
33	DGND
32	DVCC
31	$A_{OUT}7$
30	$A_{OUT}6$
29	$A_{OUT}5$
28	$A_{OUT}4$
27	$A_{OUT}3$
26	$A_{OUT}2$
25	$A_{OUT}1$
24	$A_{OUT}0$
23	OEA

Bottom pins (left to right, 12–22): V_{CC}, GNDO, CLK, VCCO, DGND, DVCC, RESET, SCLK, SDAT, REF_{IN}, REF_{OUT}

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PIN DESCRIPTION

PIN	NAME	FUNCTION
1	PD	When high, power downs the chip. TTL compatible
2	Clamp Gate	Luma clamp gate input. Clamps to selected level when high. TTL compatible
3-10	B_{OUT}<7:0>	Either chroma bits 7 (B_{OUT}7MSB) to 0 (B_{OUT}0 LSB) or composite bits 7 (MSB) to 0 (LSB). TTL compatible
11	$\overline{OEB}$	Output enable for the BOUT channel. Active low. TTL compatible
12	VCC	Reference voltage. Tie to Digital V_{CC}
13	GNDO	Output ground pin
14	CLK	Clock input pin. TTL compatible
15	VCCO	Output supply pin
16	DGND	Digital ground pin
17	DVCC	Digital supply pin
18	RESET	Resets the control registers to nominal values. Active HIGH. TTL compatible input
19	SCLK	Control Bus Clock. Address latched on rising edge, data on falling edge
20	SDAT	Control data
21	REF_{IN}	Internal reference tied to REF_{OUT}
22	REF_{OUT}	Internal reference tied to REF_{IN}
23	OEA	Output enable for the AOUT channel. Active high. TTL compatible
24-31	A_{OUT}<7:0>	Luma bit 7 (A_{OUT}7 MSB) thru Luma bit 0 (A_{OUT}0 LSB) outputs or Composite bit 7 (MSB) thru Composite bit 0 (LSB) outputs. TTL compatible
32	DVCC	Digital supply pin
33	DGND	Digital ground pin
34	NC	No connection
35	AVCC1	Analog supply pin
36	Y/CV1	Y or CV (primary composite) input pin
37	AGND1	Analog ground pin
38	AVCC2	Analog supply pin
39	VINN	Internal common mode bias of the A/D
40	AGND2	Analog ground pin
41	AVCC3	Analog supply pin
42	C/CV2	C (modulated chroma) or CV (2nd composite for dual channel mode) input pin
43	AGND3	Analog ground pin
44	REF1	Internal reference. Tie this pin thru 0.1uF capacitor to analog ground for proper operation

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ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC Supply Voltage (AVCC, DVCC, VCCO) .... -0.3V to 7V
Analog & Digital Inputs/Outputs .... -0.3 to AVCC+0.3V
Input Current Per Pin .... -25mA to 25mA
Storage Temperature Range...................... −65°C to 150°C
Junction Temperature .... 125°C

OPERATING CONDITIONS

Temperature Range .... 0°C to 70°C
Supply Range (AVCC, DVCC, VCCO) .... 4.5V to 5.5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, AVCC, DVCC, VCCO = 4.5V to 5.5V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION						
P_{diss}	Max power dissipation	Cload = 0pF		425	600	mW
SUPPLY						
AVCC	Analog supply voltage		4.5		5.5	V
DVCC	Digital supply voltage		4.5		5.5	V
VCCO	Output supply voltage		4.5		5.5	V
IDD	Digital supply current	FCLK = 30MHz		17	30	mA
I_O	Output supply current	FCLK=30MHz, V_{IN}=NTSC, 40IRE modulated rate, Cload=0pF		7		mA
I_{shut}	Shutdown current			5		mA
INPUT SIGNALS (CLK, CLAMP GATE, OEA, $\overline{OEB}$)						
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2.4		DV_{CC}	V
I_{IL}	High level Input Current	DV_{CC} - 0.1V	-5		5	μA
C_{IN1}	Input Capacitance			3		pF
INPUT SIGNALS (Y / CV1, C / CV2)						
V_{IN}	Input Voltage	Peak-to-peak for 2V	1.0	2.0	3.0	V
		Peak-to-peak for 1V	0.5	1.0	1.5	V
C_{IN2}Input	Capacitance			3		pF
I_{charge}	Clamp Charge Current	Clamp Gate = High, Digital Output < Clamp level		700		μA
I_{disch}	Clamp Discharge Current	Clamp Gate = High, Digital Output > Clamp level		−700		μA
A TO D CONVERTER OUTPUTS (A_{OUT}<7:0>, B_{OUT}<7:0>)						
	Low level output voltage	Io = 2mA	0		0.6	V
	High level output voltage		2.4		VCCO	
	Leakage current	Tri-state mode	-20		20	μA

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ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
FCLK	Clock input max frequency			30		MHz
T_{cph}	Clock input min high time	See Figure 2	15			ns
T_{cpl}	Clock input min low time	See Figure 2	15			ns
	Clamp Gate Width	V_{IN} magnitude 2V max	1.5			µs
	Clamp Gate Width	V_{IN} magnitude > 2V	3.5			µs
ANALOG SIGNAL PROCESSING						
	Y/C Gain Match	CGAIN1 = CGAIN2 = 0		1.01		V/V
	Chroma Crosstalk	Y_{IN} = 5MHz and C_{IN} = at DC; or Y_{IN} = at DC and C_{IN} = 5MHz		−60		dB
	Differential Gain	V_{IN} = NTSC 40 IRE modulated ramp FCLK = 27 MHz		2		%
	Differential Phase	V_{IN} = NTSC 40 IRE modulated ramp FCLK = 27 MHz		1		degree
	Signal to Noise Ratio	V_{IN} = 2V, 10MHz sinewave, FCLK = 20MHz		48		dB
		V_{IN} = 2V, 10MHz sinewave, FCLK = 30MHz		45		dB
	Distortion	V_{IN} = 2V, 10MHz, FCLK = 20MHz		0.3		%
	SFDR	V_{IN} = 2V, 10MHz, FCLK = 20MHz		54		dB
TRANSFER FUNCTION						
	DC integral linearity	@ 27MHz		±0.8		LSB
	DC differential linearity	@ 27MHz		±0.5		LSB
GAIN CONTROL						
G_{RES}	Gain accuracy of UGC for a given gain level	Input = $1V_{P-P}$ or $2V_{P-P}$ (See Note 2)	-30mV		30mV	%
	Absolute gain error			5		%
	Gain accuracy for standard preset gain, G_{PRESET}			1		%
OUTPUT TIMING						
t_{ds}	Sampling delay	See Figure 2		8		ns
t_{ho}	Output hold time	See Figure 2		10		ns
t_{do}	Output delay time	See Figure 2		12		ns
t_{oe}	Output enable time	See Figure 2		5		ns
t_{od}	Output disable time	See Figure 2		5		ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: Volt Peak-to-Peak = V_{P-P}

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SERIAL BUS

Unless otherwise specified, AVCC, DVCC, VCCO = 4.5V to 5.5V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT (SDAT)						
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{IH}	High Level Input Voltage		$V_{CC} - 0.8$		V_{CC}	V
I_{IL}	Low Level Input Current	V_{IN} = 0V			1.0	µA
I_{IH}	High Level Input Current	V_{IN} = DV_{CC}			1.0	µA
Z_{IN}	Input Impedance	f_{CLK} = 100kHz		1		MΩ
C_{IN}	Input Capacitance			2		pF
SYSTEM TIMING (SCLK)						
f_{CLOCK}	S_{CLK} Frequency				100	kHz
V_{HYS}	Input Hysteresis		0.2			V
t_{SPIKE}	Spike Suppression	Max Length for Zero Response		50		ns
t_{WAIT}	Wait Time From STOP to START On S_{DATA}			1.3		µs
$t_{HD/START}$	Hold Time for START On S_{DATA}			0.6		µs
$t_{SU/START}$	Setup Time for START On S_{DATA}			0.6		µs
t_{LOW}	Min LOW Time On S_{CLK}		1.3			µs
t_{HI}	Min HIGH Time On S_{CLK}		0.6			µs
$t_{HD/DATA}$	Hold Time On S_{DATA}			5.0		µs
$t_{SU/DATA}$	Setup Time On	Fast mode	100			ns
		Slow mode	250			ns
t_{LH}	Rise Time for S_{CLK} & S_{DATA}			30	300	ns
t_{HL}	Fall Time for S_{CLK} & S_{DATA}			30	300	ns
$t_{SU/STOP}$	Setup Time for STOP On S_{DATA}			0.6		µs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: All specifications include reconstruction filter and line driver.

Note 3: Normalized to burst.

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FUNCTIONAL DESCRIPTION

GENERAL

The Universal Video Digitizer is a single-chip Video A/D converter with an analog front end which is intended for analog to digital conversion of 2V peak-to-peak (V_{P-P}) or $1V_{P-P}$ signals at rates up to 30 MSPS through a high performance A/D with ±½ DNL performance. It forms a complete solution for data conversion of dual CV and Y/C signals including gain settings and clamp settings by incorporating clamps, user selectable gain controls (UGC and SGC), bias and clock generation.

The ML6411 consist of two video clamps, two sample and hold amplifiers, two three-stage pipeline A/D converters, digital error correction circuitry, selectable clamps, programmable gain control, bias voltage generation and clock generation. The operating power dissipation is 425mW typical.

INPUT FOR VARIOUS VIDEO MODES

The ML6411 can digitize various analog video inputs: S-Video (Y/C), or composite video (CV). Again, for each video channel, the gain and clamps can be selected. A description of each of these modes is described below. The Table 1 below provides a summary of the various modes.

Dual Channel Composite Video (CV1 and CV2) Mode

The composite input channels are provided through the Y/CV1 (A channel) and C/CV2 (B channel) pins. To activate this mode, the CV/S_Mode Bit (Register D, Bit D3) must set HIGH (D3=1). This mode is selectable via serial bus. In this mode, the two S&H circuits for each channel can be clocked up to 30MHz. Each CV channel can be then scaled for a desired gain setting using the User Gain Control (UGC). Standard gain selection can also be chosen using the preset gain modes for $2V_{P-P}$ signals only. For $1V_{P-P}$ signals, the preset gain selection mode is not available; however the UGC functions can be used to select gain values. The preset gain modes are for typical NTSC or PAL composite video and are selectable via serial bus through the STDA<1:0> and STDB<1:0> (Register B, Bits B4, B3, B2, and B1) bits. When using the preset gain mode, the output signals are enhanced by amplifying the input signal by the value of G_{PRESET} (see Table 2). In addition, the clamp levels can be selected for either channel for 16, 24, 64, and 128 binary levels (depending on the channel) via the serial bus through the CLPA<1:0> and CLPB<1:0> bits (see Table 3).

S-Video (Y / C) Mode

The input channels are provided through the Y/CV1 (A channel) and C/CV2 (B channel) pins. To activate this mode, the CV/S_Mode Bit (Register D, Bit D3) must be set LOW (D3=0). This mode is selectable via serial bus. In this mode, the two S&H circuits for each channel can be clocked up to 30MHz. Each channel (Y and C) can be then scaled for a desired gain setting using the User Gain

Control (UGC). Standard gain selection can also be chosen using the preset gain modes for $2V_{P-P}$ signals only. For $1V_{P-P}$ signals, the preset gain selection mode is not available; however the UGC functions can be used to select gain values. The preset gain modes are for typical NTSC or PAL S-Video and are selectable via serial bus through the STDA<1:0> and STDB<1:0> (Register B, Bits B4, B3, B2, and B1) bits. When using the preset gain mode, the output signals are enhanced by amplifying the input signal by the value of G_{PRESET} (see Table 2). In addition, the clamp levels can be selected for either channel for 16, 24, 64, and 128 binary levels (depending on the channel 24 not available for C-channel) via the serial bus through the CLPA<1:0> and CLPB<1:0> bits (see Table 3).

Input Voltage Selection

The ML6411 can support $1V_{P-P}$ and $2V_{P-P}$ input video. Selection for the voltage input is programmed via control register on the APEAK and BPEAK bits, A channel and B channel, respectively (see Table 7).

GAIN SELECTION CONTROL (UGC AND SGC)

There are two separate control mechanisms that can be used to scale gain settings for the incoming video format: User Gain Control (UGC) and Sync-suppressed Gain Control (SGC).

User Gain Control (UGC)

The user gain control function is achieved through a variation of the full scale range of the A/D converters. This will provide the user with approximately +/-3dB gain variation as needed. Y reference and C reference are supplied by two independent DACs. The user can adjust the gain of each ADC independently providing the 6-Bit code for the gain control through serial interface for each A/D. Each step change can increment or decrement the gain by 3% and allows for up to 64 different gain setting levels per channel. The UGC can be used for both 1V and $2V_{P-P}$ inputs. When using the UGC mode, the output signals are enhanced by amplifying the input signal by the value of G_{UGC}. Table 4 provides a summary of the possible incremental ranges. The gain accuracy of the UGC for each of the 64 levels is +/-1.5%. The UGC gain settings are selected via serial bus by programming Registers C, D, and E on the GNA<5:0> bits for the A-channel and GNB<5:0> bits for the B-channel.

Unity gain is set at default for GNA<5:0> = 100,000 and GNB<5:0> = 100,000. For values of GNA<5:0> and GNB<5:0> from 100,000 to 111,111, the gain increases monotonically from 0dB (unity gain) to almost 3dB (actually 1.48x), while from 100,000 to 000,000 the gain decreases monotonically from 0dB (unity gain) to –3dB (0.5x). Note that Table 4 provides only approximation of gain values: actual gain values can vary from device to device.

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FUNCTIONAL DESCRIPTION (Continued)

Sync-suppress Gain Control (SGC)

This control function is used for video where the sync signal is suppressed (i.e., chroma signal). In which case, the SGC can be activated to provide a 25% gain boost to each channel (Y and C). The SGC is activated via serial bus (Register D, Bits D1 and D2), also called the BOOSTA and BOOSTB programming bits. In the SGC mode, the output signals are enhanced by amplifying the input signal by the value of G_{SGC} (see Table 5).

Using The Gain Control Blocks Together

The UGC combined provides digital gain control data to a variable gain control circuit while the SGC is directly in the A/D processing path. Hence the UGC sets variable gain control of the A/D.

When the UGC and the SGC are enabled. In this mode, the output gain is the combination of the different gain setting mechanisms:

For $1V_{P-P}$ signals,

Equation 1: Output Gain = [<Input Signal> x G_{UGC} x G_{SGC}] + Clamp Level

For $2V_{P-P}$ signals,

Equation 2: Output Gain = [<Input Signal> x G_{UGC} x G_{SGC} x G_{PRESET}] + Clamp Level

Note that separate G_{UGC}, G_{SGC}, and G_{PRESET} values are available for both channels A and B. There are up to 640 combinations of gain settings possible.

WARNING

Note that it is possible to exceed the output voltage ranges for standard video using the combination of the gain setting mechanisms on the input signal. The user should take precaution in understanding the gain limits necessary and make the proper selection for each of the gain mechanism.

A/D CONVERTER

The A/D conversion is performed via a three stage pipeline architecture. The first two stages quantize their input signal to the three bits, then subtract the result from the input and amplify by a factor of four. This creates a residue signal which spans the full scale range of the following converter. The subtraction and amplification is performed via a bottom plate sampling capacitor feedback amplifier, similar to the input sample and hold. The third stage quantizes the signal to four bits. One bit from each of the last two stages is used for error correction.

The first stage A/D performs the conversion at the end of the sample and holds period, approximately one-half

cycle later, after the subtraction/amplification of the first stage has settled. The third stage A/D performs the conversion after another one-half cycle delay, when the second stage has settled. Error correction is then performed and, one clock cycle later, data is transferred to the output latch. This creates a 3 clock latency.

INPUT SAMPLE AND HOLD

The input sample and hold consist of a bottom plate sampling capacitor feedback amplifier. The input capacitance is 0.4pF, plus transmission gate. The input to the sample and hold is driven differentially. The sample and hold samples the input signal during the positive half cycle of the input clock, and holds the last value of the input during the negative half cycle of the input clock. The settling time of the amplifier is less than 10nS.

INPUT COUPLING AND DC CLAMP PROGRAM SELECTION

All inputs are AC coupled into the positive sampling capacitor of the sample and hold. Each input capacitor becomes the integrating component for the DC restore clamps. The direction of clamp current depends on the data at the A/D output during the clamp gating pulse. For the color channel (i.e. C in Y/C mode) the clamp level is 128. If the code is above this number during the gate pulse, the current source will sink current from the input capacitor in order to drive the input voltage lower. Otherwise, the current source will source current to raise the input voltage. Clamp currents are shown in Table 6.

The clamp values of 16, 24, 64, 128 can be select via register program (Register A and B) through the serial bus. Note that there is no Level 24 in the B channel. The CLPA<1:0> controls the clamp settings for the A-channel, while the CLPB<1:0> controls the clamp settings for the B-channel. For example, clamp values can be selected independently for the chroma channel in Y/C mode (CLPB<1:0>). Once the clamp settings are selected, the clamps are active when the ClampGate is asserted HIGH. The ClampGate signal is an external signal provided by a genlock/sync clock device that is genlocked to the horizontal sync of the video input. The ML6431 can be used to generate the ClampGate signal (see Application Section).

SERIAL PROGRAM

The ML6411 can be register programmed through the serial bus. Clamping and gain setting can be selected for various video formats. This serial bus is a standard three-pin interface with data, clock, and ground. See Timing Control information. Table 7 provides a description the Register information. Please see section "Input Coupling and DC Clamp Program Selection" and "Gain Select Control".

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FUNCTIONAL DESCRIPTION (Continued)

RESET DEFAULT MODE

The ML6411 provides a RESET pin that programs the Control Registers as described in Table 8. The RESET pin is active HIGH. Basically, the ML6411 on RESET defaults to:

■ S-Video mode. Ideally, for PAL S-Video since Preset Mode (STDA and STDB bits) is set to unity gain boost ($G_{PRESET} = 1$) for both Y and C (see Table 2)

■ Y is clamped to 16. C is clamped to 128 (see Table 3) and CLPA and CLPB bits)

■ UGC is set to unity gain ($G_{UGCA} = 1$ and $G_{UGCB} = 1$) to either Y or C channels (see Table 4 and GNA and GNB bits)

■ Input pin are set for $2V_{P-P}$ inputs on both Y and C

MODE	REGISTER/BIT VALUES	CHANNEL	SIGNAL	INPUT	OUPUT	OPTIONS
Dual CV	Register D, Bit D3= CV/S_Mode =1	A	CV1	Y/CV1 pin	$A_{OUT}^{<7:0>}$	Gain Control Selection (UGC, SGC) and Clamp Selection. $1V_{P-P}$ or $2V_{P-P}$ inputs. Serial Bus Programable.
		B	CV2	C/CV2 pin	$B_{OUT}^{<7:0>}$	
S-Video	Register D, Bit D3= CV/S_Mode =0	A	Y	Y/CV1 pin	$A_{OUT}^{<7:0>}$	Gain Control Selection (UGC, SGC) and Clamp Selection. $1V_{P-P}$ or $2V_{P-P}$ inputs. Serial Bus Programable.
		B	C	C/CV2 pin	$B_{OUT}^{<7:0>}$	

Note: Volt Peak-to-Peak = V_{P-P}

Table 1. Various Video Modes Using the ML6411 and Key Features

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DUAL COMPOSITE VIDEO MODE

STANDARD	TYPICAL INPUTS		GAIN SELECTION OF AMPLIFIERS		GAIN FACTOR OF AMPLIFIERS (nominal)	
	Channel A	Channel B	Channel A	Channel B	Channel A	Channel B
	CV1 Input (mV)	CV2 Input (mV)	STDA<1:0>	STDB<1:0>	$G_{PRESETA}$	$G_{PRESETB}$
Composite Video NTSC	1320	1320	01	01	1.061	1.061
Composite Video PAL	1400	1400	00	00	1	1
Preset Mode 1	1320	1320	01	11	1.061	0.7495
Preset Mode 2	1428	1428	11	00	1.02	1
Preset Mode 3	1400	1400	00	11	1	0.7495
Preset Mode 4	1294	1294	10	10	1.082	1.082

S-VIDEO MODE

STANDARD	TYPICAL INPUTS		GAIN SELECTION OF AMPLIFIERS		GAIN FACTOR OF AMPLIFIERS (nominal)	
	Channel A	Channel B	Channel A	Channel B	Channel A	Channel B
	Y Input (mV)	C Input (mV)	STDA<1:0>	STDB<1:0>	$G_{PRESETA}$	$G_{PRESETB}$
S-Video NTSC	1320	1320	01	01	1.061	1.061
S- Video PAL	1400	1400	00	00	1	1
Preset Mode 1	1320	1320	01	11	1.061	0.7495
Preset Mode 2	1428	1428	11	00	1.02	1
Preset Mode 3	1400	1400	00	11	1	0.7495
Preset Mode 4	1294	1294	10	10	1.082	1.082

Table 2. Video Standard Preset Gain Selection Modes

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DUAL COMPOSITE MODE

CLAMP LEVEL		CLPA1 BIT	CLPA0 BIT	NOTES
Channel A (CV1)	16	0	0	Typical CV Clamp. Defaults to this value on RESET
	24	1	0	
	64	0	1	
	128	1	1	

CLAMP LEVEL		CLPB1 BIT	CLPB0 BIT	NOTES
Channel B (CV2)	16	1	0	Typical CV clamp.
	64	1	1	
	128	0	X	Defaults to this value on RESET

S-VIDEO MODE

CLAMP LEVEL		CLPA1 BIT	CLPA0 BIT	NOTES
Channel A (Y)	16	0	0	Typical Y clamp. Defaults to this value on RESET
	24	1	0	
	64	0	1	
	128	1	1	

CLAMP LEVEL		CLPB1 BIT	CLPB0 BIT	NOTES
Channel B (C)	16	1	0	
	64	1	1	
	128	0	X	Typical C clamp. Defaults to this value on RESET

Note: X = Don't Care

Table 3. Programmable Clamp Level Selection

A-CHANNEL

	GNA5	GNA4	GNA3	GNA2	GNA1	GNA0	GAIN FACTOR G_{UGCA} (NOMINAL)
1	1	0	0	0	0	0	0.50
2	1	0	0	0	0	1	0.52
3	1	0	0	0	1	0	0.53
4	1	0	0	0	1	1	0.55
5	1	0	0	1	0	0	0.56
6	1	0	0	1	0	1	0.58
7	1	0	0	1	1	0	0.59
8	1	0	0	1	1	1	0.61
9	1	0	1	0	0	0	0.63
10	1	0	1	0	0	1	0.64
11	1	0	1	0	1	0	0.66
12	1	0	1	0	1	1	0.67
13	1	0	1	1	0	0	0.69
14	1	0	1	1	0	1	0.70
15	1	0	1	1	1	0	0.72
16	1	0	1	1	1	1	0.73
17	1	1	0	0	0	0	0.75
18	1	1	0	0	0	1	0.77
19	1	1	0	0	1	0	0.78
20	1	1	0	0	1	1	0.80
21	1	1	0	1	0	0	0.81
22	1	1	0	1	0	1	0.83
23	1	1	0	1	1	0	0.84
24	1	1	0	1	1	1	0.86
25	1	1	1	0	0	0	0.88
26	1	1	1	0	0	1	0.89
27	1	1	1	0	1	0	0.91
28	1	1	1	0	1	1	0.92
29	1	1	1	1	0	0	0.94
30	1	1	1	1	0	1	0.95
31	1	1	1	1	1	0	0.97
32	1	1	1	1	1	1	0.98
33	0	0	0	0	0	0	1.00
34	0	0	0	0	0	1	1.02
35	0	0	0	0	1	0	1.03
36	0	0	0	0	1	1	1.05
37	0	0	0	1	0	0	1.06
38	0	0	0	1	0	1	1.08
39	0	0	0	1	1	0	1.09
40	0	0	0	1	1	1	1.11
41	0	0	1	0	0	0	1.13
42	0	0	1	0	0	1	1.14
43	0	0	1	0	1	0	1.16
44	0	0	1	0	1	1	1.17
45	0	0	1	1	0	0	1.19
46	0	0	1	1	0	1	1.20
47	0	0	1	1	1	0	1.22
48	0	0	1	1	1	1	1.23
49	0	1	0	0	0	0	1.25
50	0	1	0	0	0	1	1.27
51	0	1	0	0	1	0	1.28
52	0	1	0	0	1	1	1.30
53	0	1	0	1	0	0	1.31
54	0	1	0	1	0	1	1.33
55	0	1	0	1	1	0	1.34
56	0	1	0	1	1	1	1.36
57	0	1	1	0	0	0	1.38
58	0	1	1	0	0	1	1.39
59	0	1	1	0	1	0	1.41
60	0	1	1	0	1	1	1.42
61	0	1	1	1	0	0	1.44
62	0	1	1	1	0	1	1.45
63	0	1	1	1	1	0	1.47
64	0	1	1	1	1	1	1.48

B-CHANNEL

	GNB5	GNB4	GNB3	GNB2	GNB1	GNB0	GAIN FACTOR G_{UGCB} (NOMINAL)
1	1	0	0	0	0	0	0.50
2	1	0	0	0	0	1	0.52
3	1	0	0	0	1	0	0.53
4	1	0	0	0	1	1	0.55
5	1	0	0	1	0	0	0.56
6	1	0	0	1	0	1	0.58
7	1	0	0	1	1	0	0.59
8	1	0	0	1	1	1	0.61
9	1	0	1	0	0	0	0.63
10	1	0	1	0	0	1	0.64
11	1	0	1	0	1	0	0.66
12	1	0	1	0	1	1	0.67
13	1	0	1	1	0	0	0.69
14	1	0	1	1	0	1	0.70
15	1	0	1	1	1	0	0.72
16	1	0	1	1	1	1	0.73
17	1	1	0	0	0	0	0.75
18	1	1	0	0	0	1	0.77
19	1	1	0	0	1	0	0.78
20	1	1	0	0	1	1	0.80
21	1	1	0	1	0	0	0.81
22	1	1	0	1	0	1	0.83
23	1	1	0	1	1	0	0.84
24	1	1	0	1	1	1	0.86
25	1	1	1	0	0	0	0.88
26	1	1	1	0	0	1	0.89
27	1	1	1	0	1	0	0.91
28	1	1	1	0	1	1	0.92
29	1	1	1	1	0	0	0.94
30	1	1	1	1	0	1	0.95
31	1	1	1	1	1	0	0.97
32	1	1	1	1	1	1	0.98
33	0	0	0	0	0	0	1.00
34	0	0	0	0	0	1	1.02
35	0	0	0	0	1	0	1.03
36	0	0	0	0	1	1	1.05
37	0	0	0	1	0	0	1.06
38	0	0	0	1	0	1	1.08
39	0	0	0	1	1	0	1.09
40	0	0	0	1	1	1	1.11
41	0	0	1	0	0	0	1.13
42	0	0	1	0	0	1	1.14
43	0	0	1	0	1	0	1.16
44	0	0	1	0	1	1	1.17
45	0	0	1	1	0	0	1.19
46	0	0	1	1	0	1	1.20
47	0	0	1	1	1	0	1.22
48	0	0	1	1	1	1	1.23
49	0	1	0	0	0	0	1.25
50	0	1	0	0	0	1	1.27
51	0	1	0	0	1	0	1.28
52	0	1	0	0	1	1	1.30
53	0	1	0	1	0	0	1.31
54	0	1	0	1	0	1	1.33
55	0	1	0	1	1	0	1.34
56	0	1	0	1	1	1	1.36
57	0	1	1	0	0	0	1.38
58	0	1	1	0	0	1	1.39
59	0	1	1	0	1	0	1.41
60	0	1	1	0	1	1	1.42
61	0	1	1	1	0	0	1.44
62	0	1	1	1	0	1	1.45
63	0	1	1	1	1	0	1.47
64	0	1	1	1	1	1	1.48

Table 4. Gain Approximations for User Gain Control (UGC) Block

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CHANNEL	REGISTER/BIT VALUES	GAIN FACTOR
A	REGISTER D, BIT D1 = "BOOSTA" = 0	G_{SGCA} = 1
	REGISTER D, BIT D1 = "BOOSTA" = 1	G_{SGCA} = 1.25
B	REGISTER D, BIT D2 = "BOOSTB" = 0	G_{SGCB} = 1
	REGISTER D, BIT D2 = "BOOSTB" = 1	G_{SGCB} = 1.25

Table 5. SGC Gain Mode

CLAMP GATE SIGNAL	CLAMP LEVEL	OUTPUT	CLAMP CURRENT
0	X	X	0
1	00	OUT < 16	700µA
	00	OUT > 16	−700µA
	01	OUT < 64	700µA
	01	OUT > 64	−700µA
	10	OUT < 24	700µA
	10	OUT > 24	−700µA
	11	OUT < 128	700µA
	11	OUT > 128	−700µA

Table 6: Clamp Current for Various Clamp Levels

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REGISTER INFORMATION AND ORGANIZATION

REGISTER	ADDRESS	DATA BIT	NAME	DESCRIPTION	BIT CODE RANGE
A	000	A0	CLPA0	Sets Clamp Level for the A Channel	See Table 3
		A1	CLPA1	Sets Clamp Level for the A Channel	See Table 3
		A2	Reserved	Reserved	Don't Care
		A3	Reserved	Reserved	Don't Care
		A4	CLPB0	Sets Clamp Level for the B Channel	See Table 3
B	001	B0	CLPB1	Sets Clamp Level for the B Channel	See Table 3
		B1	STDB0	Selects Standard Preset Gain Level for B Channel	See Table 2
		B2	STDB1	Selects Standard Preset Gain Level for B Channel	See Table 2
		B3	STDA0	Selects Standard Preset Gain Level for A Channel	See Table 2
		B4	STDA1	Selects Standard Preset Gain Level for A Channel	See Table 2
C	010	C0	GNA0	Sets User Defined Gain Level for A Channel	See Table 4
		C1	GNA1	Sets User Defined Gain Level for A Channel	See Table 4
		C2	GNA2	Sets User Defined Gain Level for A Channel	See Table 4
		C3	GNA3	Sets User Defined Gain Level for A Channel	See Table 4
		C4	GNA4	Sets User Defined Gain Level for A Channel	See Table 4
D	011	D0	GNA5	Sets User Defined Gain Level for A Channel	See Table 4
		D1	BOOSTA	Provides 25% Extra Gain on A Channel	0 = 1 x Gain; 1 = 1.25 x Gain; See Table 5
		D2	BOOSTB	Provides 25% Extra Gain on B Channel	0 = 1 x Gain; 1 = 1.25 x Gain; See Table 5
		D3	CV/S_Mode	Select Dual Composite Mode or S-Video Mode	0 = S-Video Mode; 1 = Dual Composite Mode
		D4	GNB0	Selects User Defined Gain Level for B Channel	See Table 4
E	100	E0	GNB1	Sets User Defined Gain Level for B Channel	See Table 4
		E1	GNB2	Sets User Defined Gain Level for B Channel	See Table 4
		E2	GNB3	Sets User Defined Gain Level for B Channel	See Table 4
		E3	GNB4	Sets User Defined Gain Level for B Channel	See Table 4
		E4	GNB5	Sets User Defined Gain Level for B Channel	See Table 4
F	101	F0	Reserved	Set to 0 for Proper Operation	F0 = 0
		F1	APEAK	Sets A Channel for $1V_{P-P}$ or $2V_{P-P}$ inputs	$1 = 1V_{P-P}$ $0 = 2V_{P-P}$
		F2	BPEAK	Sets A Channel for $1V_{P-P}$ or $2V_{P-P}$ inputs	$1 = 1V_{P-P}$ $0 = 2V_{P-P}$
		F3	CLKDIV	Sets Internal Clock Frequency to Divide-by-2	$1 = 1V_{P-P}$ $0 = 2V_{P-P}$
		F4	Reserved	Recommend 0 for RESET and 1 for Normal Operation	0 or 1 is Acceptable

Note: Volt Peak-to-Peak = V_{P-P}

Table 7: Control Register Summary

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REGISTER INFORMATION AND ORGANIZATION

REGISTER	ADDRESS	DATA BIT	NAME	DESCRIPTION	DEFAULT SETTING
A	000	A0	CLPA0	Sets Clamp Level for the A Channel to 16	0
		A1	CLPA1		0
		A2	Reserved	Reserved	X
		A3	Reserved	Reserved	X
		A4	CLPB0	Sets Clamp Level for the B Channel to 128	X
B	001	B0	CLPB1	Sets Clamp Level for the B Channel to 128	0
		B1	STDB0	Selects Standard Preset Gain Level for B Channel (See Table 2)	0
		B2	STDB1	Selects Standard Preset Gain Level for B Channel (See Table 2)	0
		B3	STDA0	Selects Standard Preset Gain Level for A Channel (See Table 2)	0
		B4	STDA1	Selects Standard Preset Gain Level for A Channel (See Table 2)	0
C	010	C0	GNA0	Sets User Defined Gain Level for A Channel (See Table 4)	0
		C1	GNA1	Sets User Defined Gain Level for A Channel (See Table 4)	0
		C2	GNA2	Sets User Defined Gain Level for A Channel (See Table 4)	0
		C3	GNA3	Sets User Defined Gain Level for A Channel (See Table 4)	0
		C4	GNA4	Sets User Defined Gain Level for A Channel (See Table 4)	0
D	011	D0	GNA5	Sets User Defined Gain Level for A Channel (See Table 4)	1
		D1	BOOSTA	Provides 25% Extra Gain on A Channel	0 = 1 x Gain
		D2	BOOSTB	Provides 25% Extra Gain on B Channel (See Table C)	0 = 1 x Gain
		D3	CV/S_Mode	Select Dual Composite Mode or S-Video Mode	0 = S-Video Mode
		D4	GNB0	Selects User Defined Gain Level for B Channel (See Table 4)	0
E	100	E0	GNB1	Sets User Defined Gain Level for B Channel (See Table 4)	0
		E1	GNB2	Sets User Defined Gain Level for B Channel (See Table 4)	0
		E2	GNB3	Sets User Defined Gain Level for B Channel (See Table 4)	0
		E3	GNB4	Sets User Defined Gain Level for B Channel (See Table 4)	0
		E4	GNB5	Sets User Defined Gain Level for B Channel (See Table 4)	1
F	101	F0	Reserved	Set to 0 for Proper Operation	0
		F1	APEAK	Sets A Channel for $1V_{P-P}$ or $2V_{P-P}$ inputs	$0 = 2V_{P-P}$
		F2	BPEAK	Sets A Channel for $1V_{P-P}$ or $2V_{P-P}$ inputs	$0 = 2V_{P-P}$
		F3	CLKDIV	Sets Internal Clock Frequency to Divide-by-2	0 = CLK
		F4	Reserved	Recommend 0 for RESET and 1 for Normal Operation	0

Note: X = Don't Care

Note: Volt Peak-to-Peak = V_{P-P}

Table 8: RESET Control Valures of Control Register

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REGISTER INFORMATION AND ORGANIZATION

DEVICE INFORMATION
  DEVICE ADDRESS: B5
  REGISTOR ADDRESS BITS:
    RA <2:0>
  DATA BITS: <4:0>X

CONTROL REGISTERS:

REGISTER A
ADDRESS RA <2:0> = <000>

MSB

A4	A3	A2	A1	A0	X

  REGISTER A
    ADDRESS RA <2:0> = <000>
    DATABITS A <4:0> X

REGISTER B
ADDRESS RA <2:0> = <001>

MSB

B4	B3	B2	B1	B0	X

  REGISTER B
    ADDRESS RA <2:0> = <001>
    DATABITS B <4:0> X

REGISTER C
ADDRESS RA <2:0> = <010>

MSB

C4	C3	C2	C1	C0	X

  REGISTER C
    ADDRESS RA <2:0> = <010>
    DATABITS C <4:0> X

REGISTER D
ADDRESS RA <2:0> = <011>

MSB

D4	D3	D2	D1	D0	X

  REGISTER D
    ADDRESS RA <2:0> = <011>
    DATABITS D <4:0> X

REGISTER E
ADDRESS RA <2:0> = <100>

MSB

E4	E3	E2	E1	E0	X

  REGISTER E
    ADDRESS RA <2:0> = <100>
    DATABITS E <4:0> X

REGISTER F
ADDRESS RA <2:0> = <101>

MSB

F4	F3	F2	F1	F0	X

  REGISTER F
    ADDRESS RA <2:0> = <101>
    DATABITS F <4:0> X

X = DUMMY BIT FOR ACKNOWLEDGE

Figure 1. Register Organization and Information

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TIMING CONTROL

The ML6411 operates in master mode where all internal timing is derived from the clock input at the CLK pin. Figure 2 provides timing diagrams for both the Dual Composite and Y/C modes. Note that the REF OUT pin provides the internal timing to the REF IN pin. These pins are shorted together for normal operation.

Serial Bus Timing. Figure 3 provides timing of serial bus mode. Figure 4 provides a detailed timing for device, register, and data insertion to the control registers. As shown in Figure 1, there are six independent 5-bit registers in the Control Block. To load a register, the 3-bit address is loaded in first followed by the 5-bit data values and a dummy bit. This is a total of 9-bits to load a register with the last bit being a dummy bit. Note that all of the registers can be loaded in succession before the STOP condition is enabled.

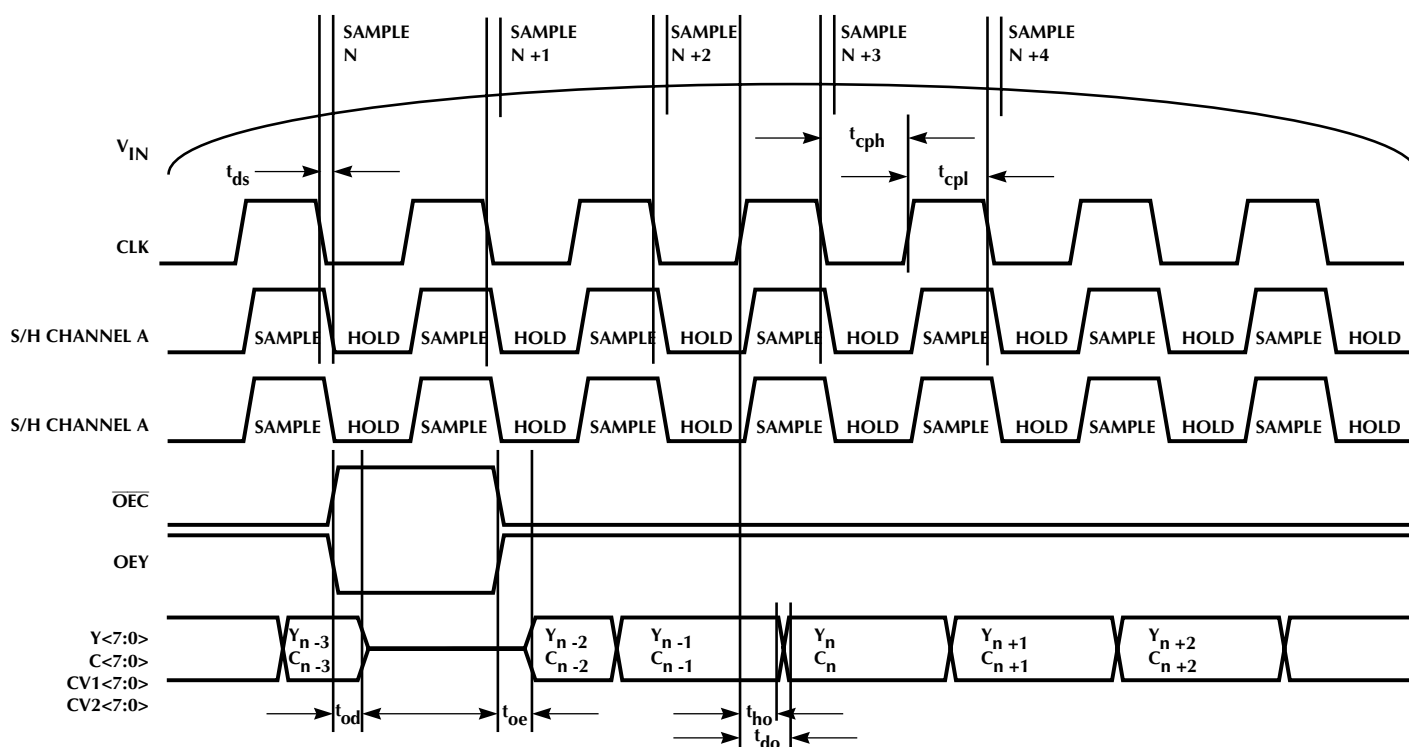The CLKDIV function provides an internal divide-by-2 clock. This function is enable via control register.
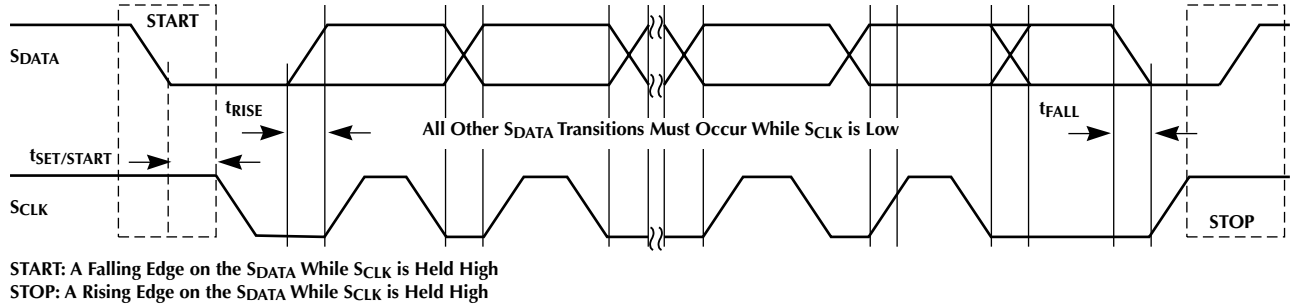

Figure 2. Y/C and Dual CV Mode

START: A Falling Edge on the S$_{DATA}$ While S$_{CLK}$ is Held High
STOP: A Rising Edge on the S$_{DATA}$ While S$_{CLK}$ is Held High

Figure 3. Definition of START & STOP on Serial Data Bus
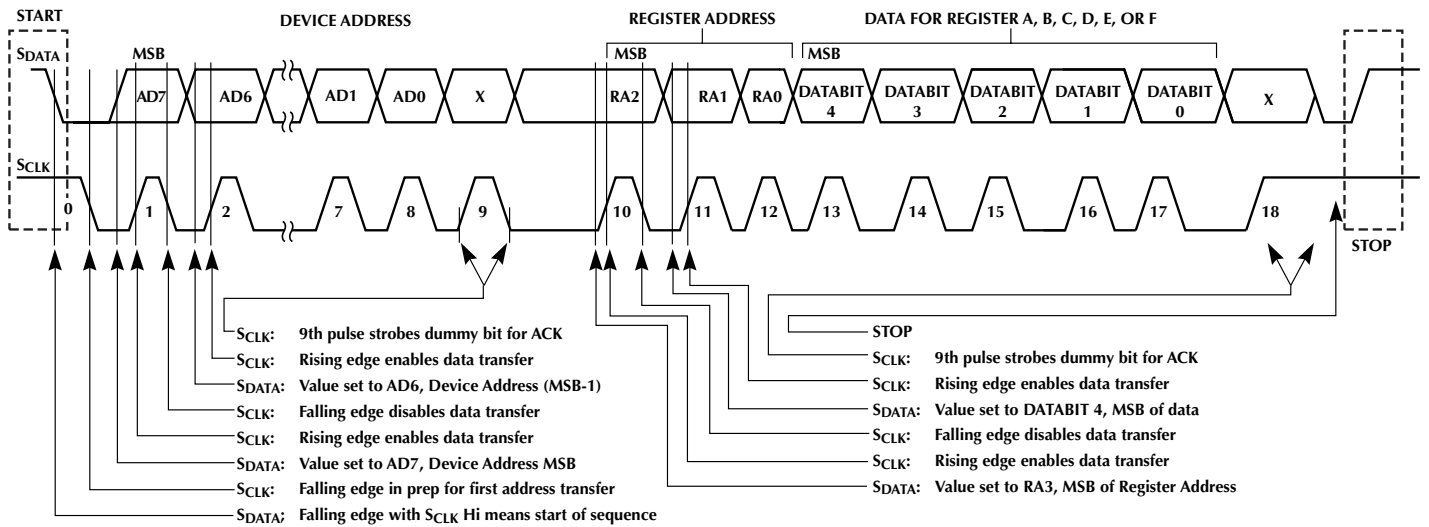

Figure 4. Definition of ADDRESS and DATA FORMAT on Serial Data Bus

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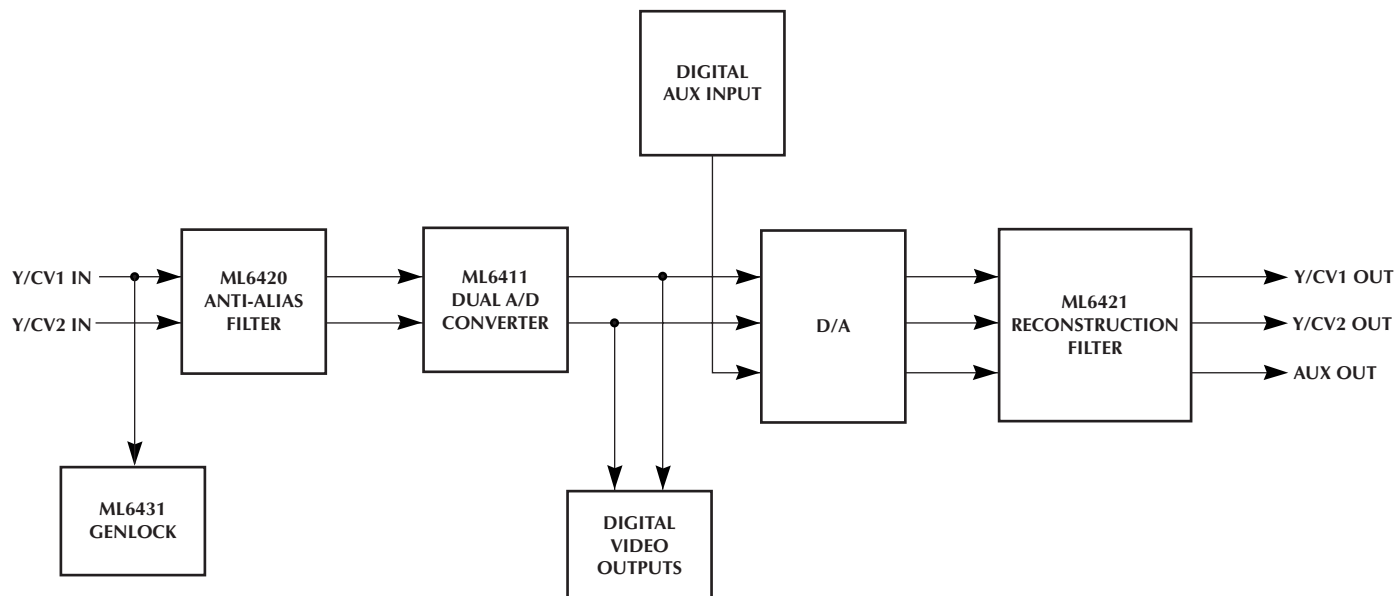
APPLICATION 1: VIDEO EDITING SYSTEMS

Figure 5. Typical S-video and Composite Video Capture System
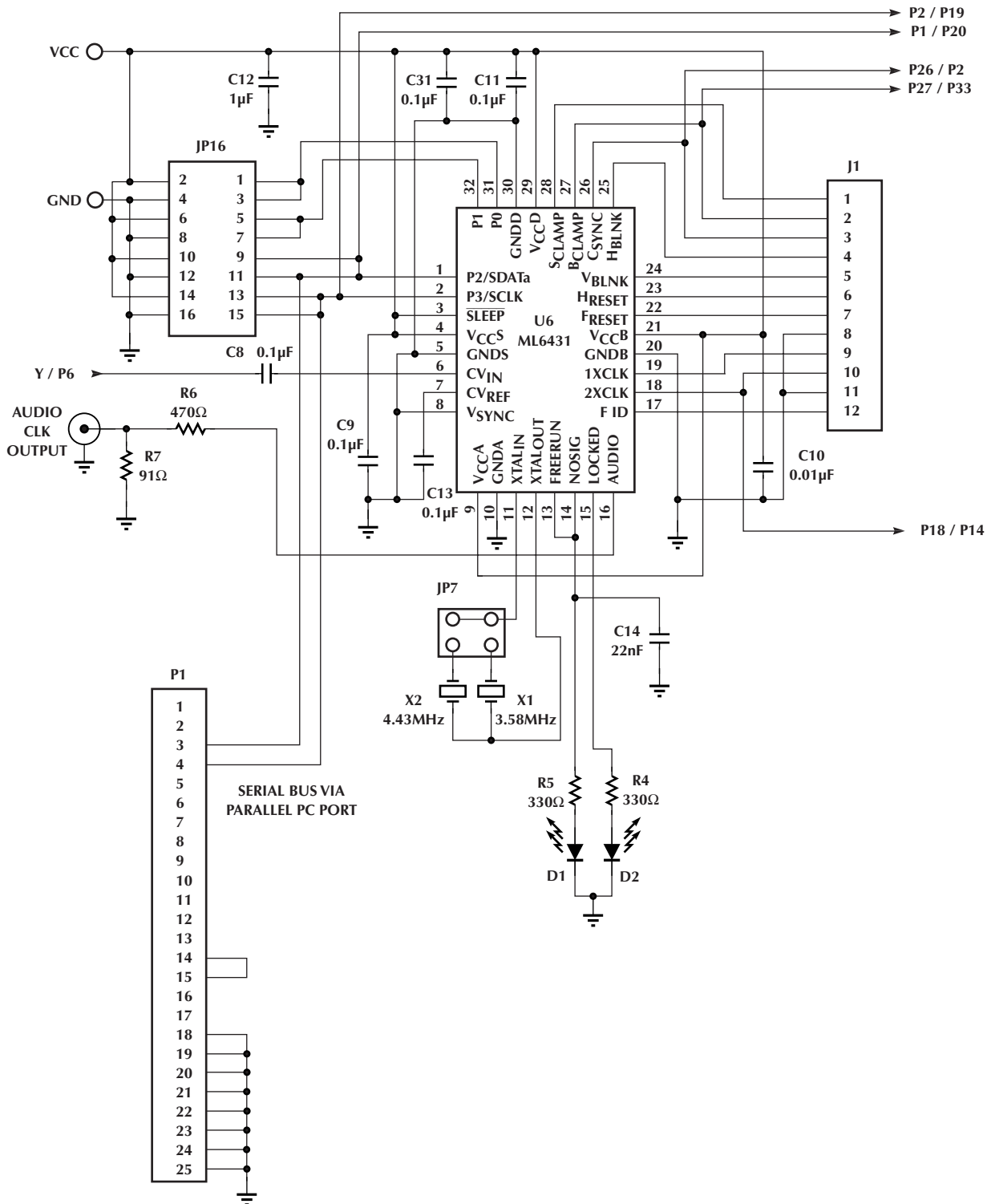
APPLICATION 1: VIDEO EDITING SYSTEMS

Figure 6 (Page 1 of 3). Application Schematic Detailing Block Diagram of Figure 5
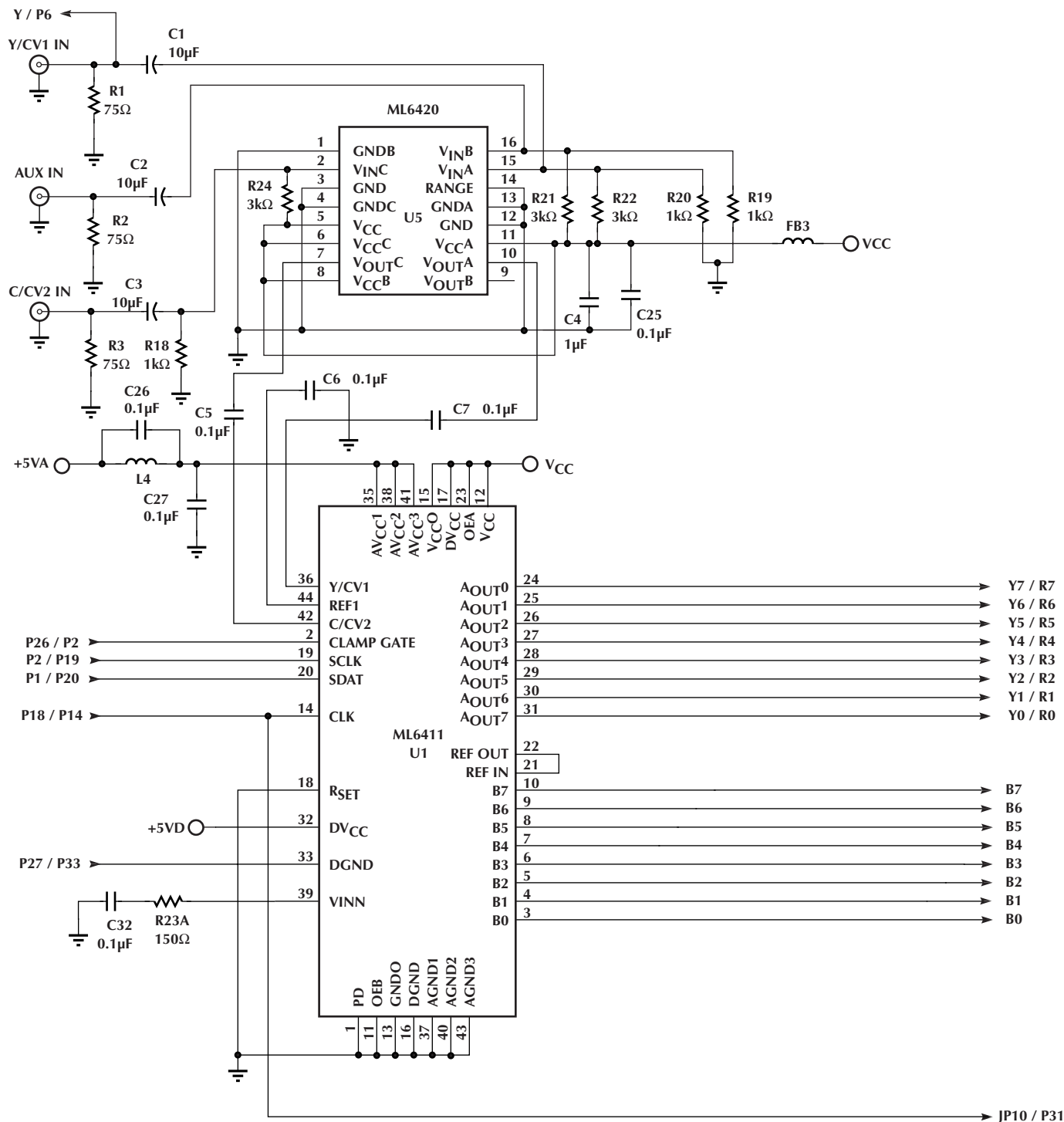
Micro Linear

Figure 6 (Page 2 of 3). Application Schematic Detailing Block Diagram of Figure 5

APPLICATION 1: VIDEO EDITING SYSTEMS

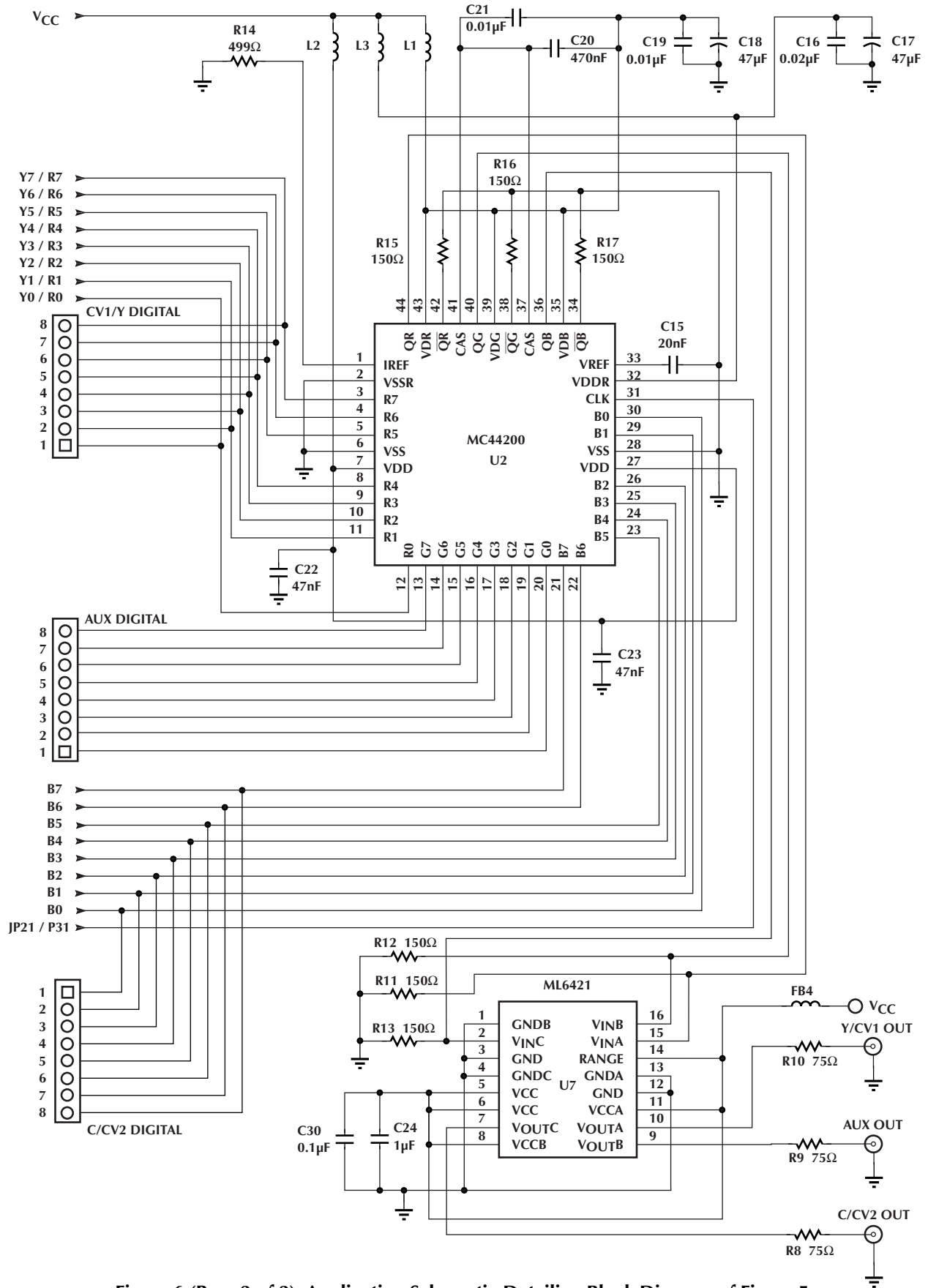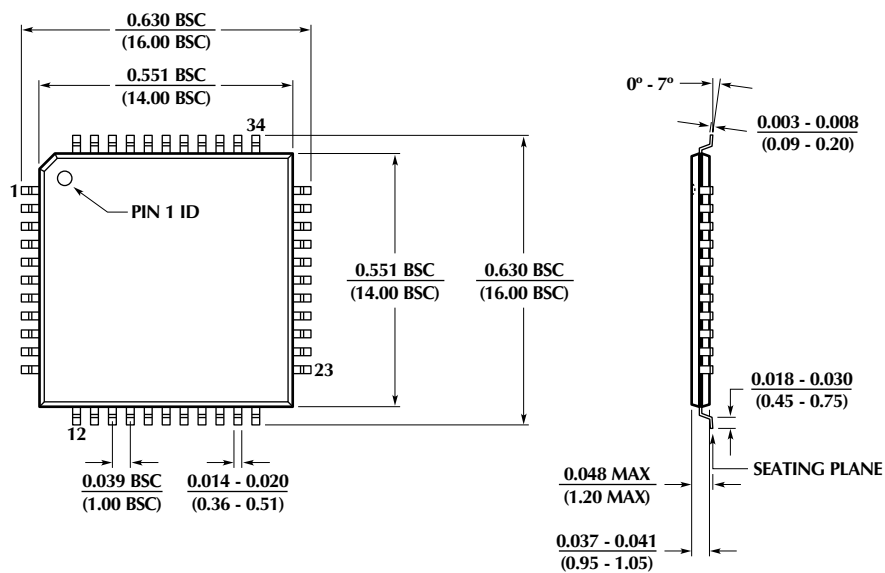**Figure 6 (Page 3 of 3). Application Schematic Detailing Block Diagram of Figure 5**

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PHYSICAL DIMENSIONS inches (millimeters)

Package: H44-14
44-Pin (14 x 14 x 1mm) TQFP

0.630 BSC
(16.00 BSC)

0.551 BSC
(14.00 BSC)

34

1

PIN 1 ID

0.551 BSC
(14.00 BSC)

0.630 BSC
(16.00 BSC)

23

12

0.039 BSC
(1.00 BSC)

0.014 - 0.020
(0.36 - 0.51)

0° - 7°

0.003 - 0.008
(0.09 - 0.20)

0.018 - 0.030
(0.45 - 0.75)

SEATING PLANE

0.048 MAX
(1.20 MAX)

0.037 - 0.041
(0.95 - 1.05)

ML6411

ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML6411		0°C to 70°C	44 Pin TQFP (H44)

Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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