

Product Brief

MPC555PB/D
Rev. 3, 2/2003

MPC555 Product Brief



This document provides an overview of the MPC555 microcontroller, including a block diagram showing the major modular components and sections that list the major features. The MPC555 member of the Motorola MPC500 RISC Microcontroller family.

Table 1. MPC555 Features

Device	Flash	Code Compression
MPC555	448 Kbytes	Code compression not supported

1 Introduction

The MPC555 device offers the following features:

- PowerPC™ core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes Flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCAN™)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40 °C to 125 °C with dual supply (3.3 V, 5 V) (-55 °C to 125 °C for the suffix A device)
- 32-bit architecture (PowerPC ISA architecture compliant)
- Core performance measured at 52.7-Kbyte Dhrystones (v2.1) @ 40 MHz
- Fully static, low power operation
- Integrated double-precision floating-point unit
- Precise exception model

www.DataSheet.in

Block Diagram

- Extensive system development support
 - On-chip watchpoints and breakpoints
 - Program flow tracking
 - BDM on-chip emulation development interface

1.1 Block Diagram

Figure 1 is a block diagram of the MPC555.

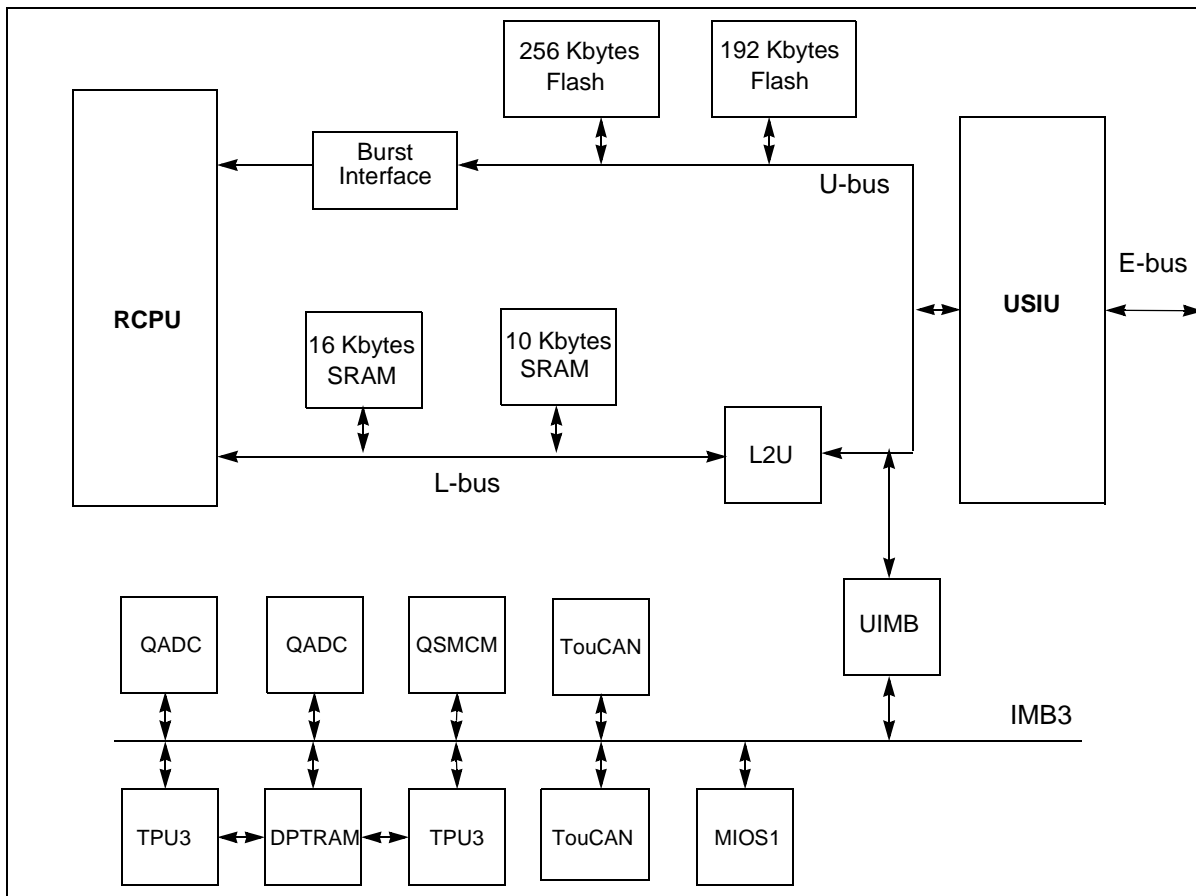


Figure 1. MPC555 Block Diagram

1.2 Key Features

The MPC555 key features are explained in the following sections.

1.2.1 Four-Bank Memory Controller

- Works with SRAM, EPROM, Flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks

www.DataSheet.in

1.2.2 U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- MPC555 decremter and time base
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port
- External bus interface
 - 24 address pins, 32 data pins
 - Supports multiple master designs
 - Four-beat transfer bursts, two-clock minimum bus transactions
 - Supports 5V inputs, provides 3.3-V outputs

1.2.3 Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.4 448-Kbyte Flash EEPROM Memory

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

1.2.5 26-Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

1.2.6 General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
- Nine general-purpose I/O pins in MIOS1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V tolerant inputs/outputs

1.2.7 Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
 - A dedicated micro-engine operates independently of the RCPU
 - 16 independent programmable channels and pins
 - Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
 - Nine pre-programmed timer functions are available
 - Any channel can perform any time function
 - Each timer function can be assigned to more than one channel
 - Two timer count registers with programmable prescalers
 - Each channel can be synchronized to one or both counters
 - Selectable channel priority levels
 - 5-V tolerant inputs/outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

1.2.8 18-Channel Modular I/O System (MIOS1)

- Ten double action submodules (DASM)
- Eight dedicated PWM sub-modules (PWMSM)
- Two 16-bit modulus counter submodules (MCSM)
- Two parallel port I/O submodules (PIOSM)
- 5-V tolerant inputs/outputs

1.2.9 Two Queued Analog-to-Digital Converter Modules (QADC64)

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10 μ s (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned
- 5-V reference and range

1.2.10 Two CAN 2.0B Controller Modules (TouCAN)

Each TouCAN provides these features:

- Full implementation of CAN protocol specification, version 2.0A and 2.0B
- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

1.2.11 Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - 160-byte queue buffer
 - Programmable transfer length: from 8 to 16 bits, inclusive
 - Synchronous interface with baud rate of up to system clock divided by 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g., – serial A/D converters, I/O latches, etc.)
- Two serial communications interfaces (SCI). Each SCI offers these features:
 - UART mode provides NRZ format and half-or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer (SCI1 only)
 - Advanced error detection and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits and double buffering of data
 - Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
 - External source clock for baud generation
 - Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs, allowing realization of a low-speed serial protocol

2 MPC555 Address Map

The internal memory map is shown in Figure 2.

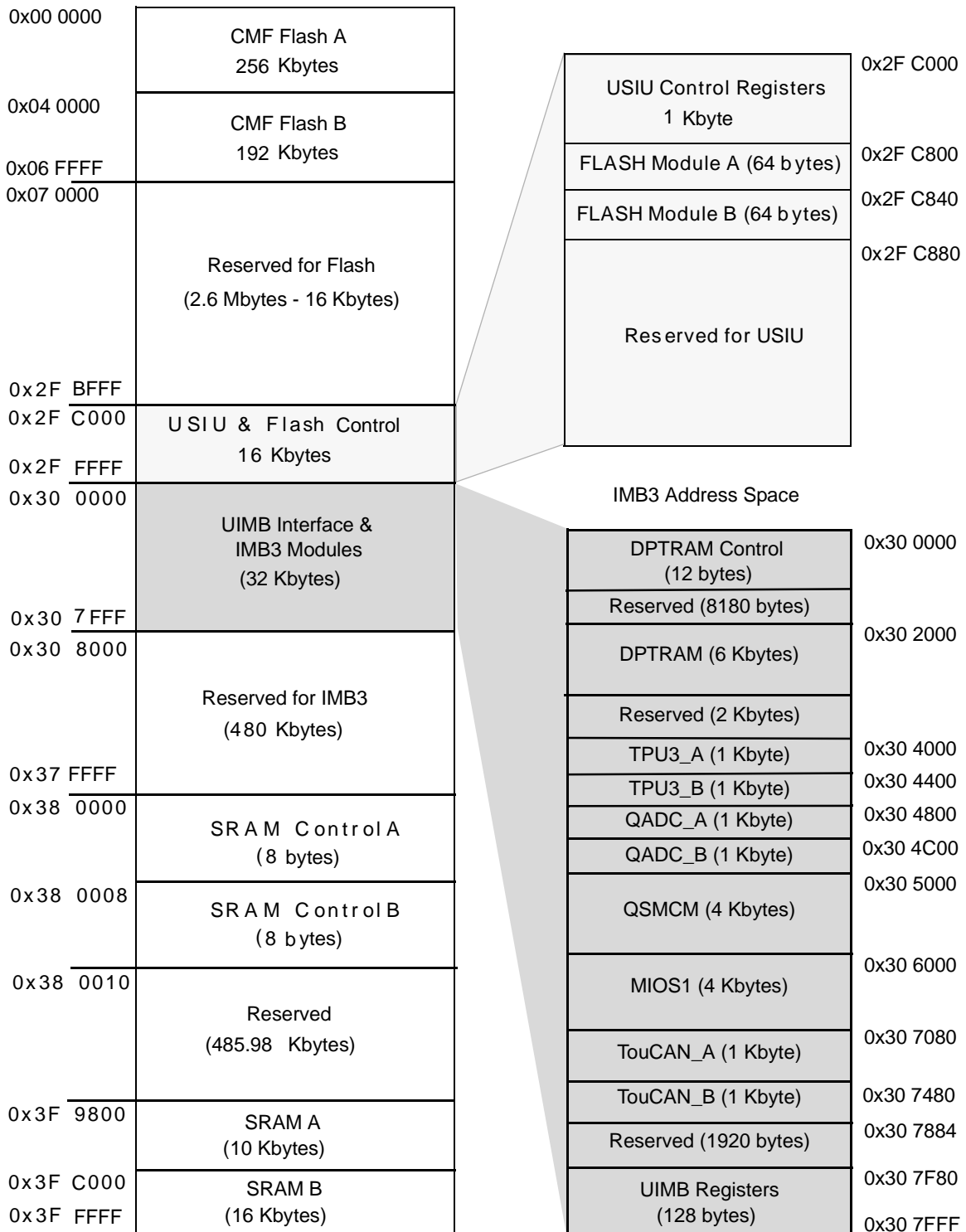


Figure 2. MPC555 Internal Memory Map

3 MPC555 Pinout Diagram

Figure 3 shows the pinout for the MPC555.

MPC555 Ball Map

A	VDDH	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	A_TPUCH16	VRL	AAN0_POB0	AAN4_POB4	AAN8_POB8	BAN2_POB2	BAN6_POB6	BAN10_POB10	BAN14_POB14	BAN18_POB18	MDA13	VDDH	MDA28	
B	B_TZCLK	VDDH	A_TPUCH6	A_TPUCH10	A_TPUCH14	VRH	AAN3_POB3	AAN7_POB7	AAN11_POB11	AAN15_POB15	BAN4_POB4	BAN8_POB8	BAN12_POB12	BAN16_POB16	MDA15	VDDH	MDA32		
C	B_TPUCH8	A_TZCLK	A_TPUCH9	A_TPUCH13	VDDA	VBDA	AAN2_POB2	AAN6_POB6	AAN10_POB10	AAN14_POB14	BAN5_POB5	BAN9_POB9	BAN13_POB13	BAN17_POB17	MDA14	MDA27	MDA31		
D	B_TPUCH11	B_TPUCH13	A_TPUCH0	A_TPUCH2	VSSA	VSSA	AAN1_POB1	AAN5_POB5	AAN9_POB9	AAN13_POB13	BAN3_POB3	BAN7_POB7	BAN11_POB11	BAN15_POB15	MPVM1	MPVM2	MPVM3		
E	B_TPUCH7	B_TPUCH10	B_TPUCH4	VDDL											MPVM0	MPVM19	MPVM20		
F	B_TPUCH5	B_TPUCH6	B_TPUCH8	B_TPUCH12											MPVM16	MPVM18	MPVM19		
G	B_TPUCH2	B_TPUCH3	B_TPUCH4	B_TPUCH9											MPIO5	MPIO8	MPIO12		
H	B_TPUCH1	B_TPUCH0	B_CNTRX0	B_CNTRX0											MPIO10	MPIO15	MPIO13		
J	TCK_DSCK	TDO_DSCK	TRST_B	VDDSRAM											VF18_MPIO2	VF19_MPIO3	VF20_MPIO1		
K	TMS	TDL_DSDI	SGP_FRZ	VDDL											VFLS1_MPIO4	VFLS1_MPIO4	A_CNTRX0		
L	IMP1_VFLS	IMP0_VFLS	IRC0B_SGP	IRC0B_SGP											PC31_SGP	PC31_SGP	MISO_OGP		
M	IRC0B_SGP	IRC0B_SGP	SGP_IRROUTB	SGP_IRROUTB											PC32_SGP	PC32_SGP	ECK		
N	WEB_AT10	BRB_IMP2	BBB_IMP3	BBB_IMP3											RXD1_OGP1	TXD1_OGP0	TXD2_OGP0		
P	WEB_AT11	WEB_AT12	WEB_AT13	CS/B											VPP	EFEF	VSSF		
R	RD_VRB	CS/B	CS/B	CS/B											VDDL	VDDF	VDDSYN		
T	OEB	TEAB	TSZ1	VDDL											VDDI	KAPWR	VSSSYN		
U	TSZ0	TAB	TSB	BDIFB											RCRB_TXP	EXTCLK	ECK_BUCK		
V	BURSTB	BIB_STB	Addr_SGP11	Addr_SGP10	Addr_SGP9	Addr_SGP8	Addr_SGP22	Addr_SGP21	Addr_SGP20	Addr_SGP19	Data_SGP24	Data_SGP23	Data_SGP22	Data_SGP21	Data_SGP18	CLKOUT	PORESETB		
W	Addr_SGP12	VDDH	Addr_SGP14	Addr_SGP13	Addr_SGP16	Addr_SGP15	Addr_SGP2	Addr_SGP1	Addr_SGP0	Data_SGP3	Data_SGP5	Data_SGP7	Data_SGP9	Data_SGP11	Data_SGP13	Data_SGP17	IRCB_SGP	VDDH	
Y	VDDH	Addr_SGP15	Addr_SGP16	Addr_SGP17	Addr_SGP18	Addr_SGP21	Addr_SGP24	Data_SGP0	Data_SGP1	Data_SGP2	Data_SGP4	Data_SGP6	Data_SGP8	Data_SGP10	Data_SGP12	Data_SGP14	ROBB_mck2	IRQ7B_mck3	VDDH
	VSSB	-3 volt power (I/O)	VDDI	-3 volt power (internal)	VSS	-ground	VSS	-5 volt power	VDDH	-Misc power									

Note: The pinout is a top down view of the package.

Version 10.2
21 November 1997
Substrate 9/30/97a
Y Dees

Figure 3. MPC555 Pinout Diagram

4 Supporting Documentation List

This list contains references to currently available and planned documentation.

- *MPC555 User's Manual* (MPC555UM/AD)
- *RCPURM Reference Manual* (RCPURM/AD)
- *Board Strategies for Ensuring Optimum Frequency Synthesizer Performance* (AN1282/D)
- *Using the MIOS on the MPC555 Evaluation Board* (AN1778/D)
- *Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family* (AN1821/D)
- *Non-Volatile Memory Technology Overview* (AN1837/D)
- *Designing Expansion Boards for the Motorola EVB555/ETAS ES200* (AN2001/D)
- *MPC555 Interrupts* (AN2109/D)
- *EMC Guidelines for MPC500-Based Automotive Powertrain Systems* (AN2127/D)
- Nexus Standard Specification (non-Motorola document)
- Nexus Web Site: <http://www.nexus5001.org/>
- IEEE 1149.1 Specification (non-Motorola document)

5 Revision History

Table 2. Revision History

Revision Number	Substantive Changes	Date of Release
2	Existing Document.	September 2001
2.1	Added temperature range for suffix A device.	11 December 2002
3	Updated template and formats.	11 February 2003

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

HOW TO REACH US:**USA/EUROPE/LOCATIONS NOT LISTED:**

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

<http://www.motorola.com/semiconductors>

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein.

Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.



Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. digital dna is a trademark of Motorola, Inc. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola, Inc. 2003

MPC555PB/D