DATA SHEET

P87CL881H

Low-voltage microcontroller with 63-kbyte OTP program memory and 2-kbyte RAM

Product specification
File under Integrated Circuits, IC17

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Philips
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CONTENTS

Low-voltage microcontroller with 63-kbyte OTP program memory and 2-kbyte RAM

P87CL881H

1 FEATURES

- Full static 80C51 CPU; enhanced 8-bit architecture with:
  - Minimum 6 cycles per instruction (twice as fast as a standard 80C51 core)
  - Non-page oriented instructions
  - Direct addressing
  - Four 8-byte RAM register banks
  - Stack depth limited only by available internal RAM (maximum 256 bytes)
  - Multiply, divide, subtract and compare instructions.
- Very low current consumption
- Single supply voltage of 2.7 to 3.6 V
- Frequency: 1 to 10 MHz
- Operating temperature: –25 to +70 °C
- 44-pin LQFP package
- Four 8-bit ports (32 I/O lines)
- 63-kbyte One-Time Programmable (OTP) program memory; programmable in parallel mode or in-system via I^{2}C-bus interface.
- 256-byte internal RAM
- 1792-byte internal AUX-RAM
- External address range: 64 kbytes of ROM and 64 kbytes of RAM
- Amplitude Controlled Oscillator (ACO) suitable for use with a quartz crystal or ceramic resonator
- Improved Power-on/Power-off reset circuitry (POR)
- Low Voltage Detection (LVD) with 11 software programmable levels
- 8 interrupts on Port 1, edge or level sensitive triggering selectable via software power-saving use for keyboard control
- Twenty source, twenty vector interrupt structure with two priority levels
- Wake-up from Power-down mode via LVD or external interrupts at Port 1
- Two 16-bit timer/event counters
- Additional 16-bit timer/event counters, with capture, compare and PWM function
- Watchdog Timer
- Full duplex enhanced UART with double buffering
- I^{2}C-bus interface for serial transfer on two lines, maximum operating frequency 400 kHz.

2 GENERAL DESCRIPTION

The P87CL881 is an 8-bit microcontroller especially suited for pager applications.

The P87CL881 is manufactured in an advanced CMOS technology and is based on single chip technology.

The device is optimized for low power consumption and has two software selectable features for power reduction: Idle and Power-down modes. In addition, all derivative blocks switch off their clock if they are inactive.

The instruction set of the P87CL881 is based on that of the 80C51. The P87CL881 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

This data sheet details the specific properties of the P87CL881; for details of the P87CL881 core and the derivative functions see the *"TELX family"* data sheet and *"8051-Based 8-bit Microcontrollers; Data Handbook IC20"*.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PRODUCT TYPE	PACKAGE		
		NAME	DESCRIPTION	VERSION
P87CL881H/000	Blank OTP	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P87CL881H/xxx	Factory-programmed OTP			

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and options.

4 BLOCK DIAGRAM

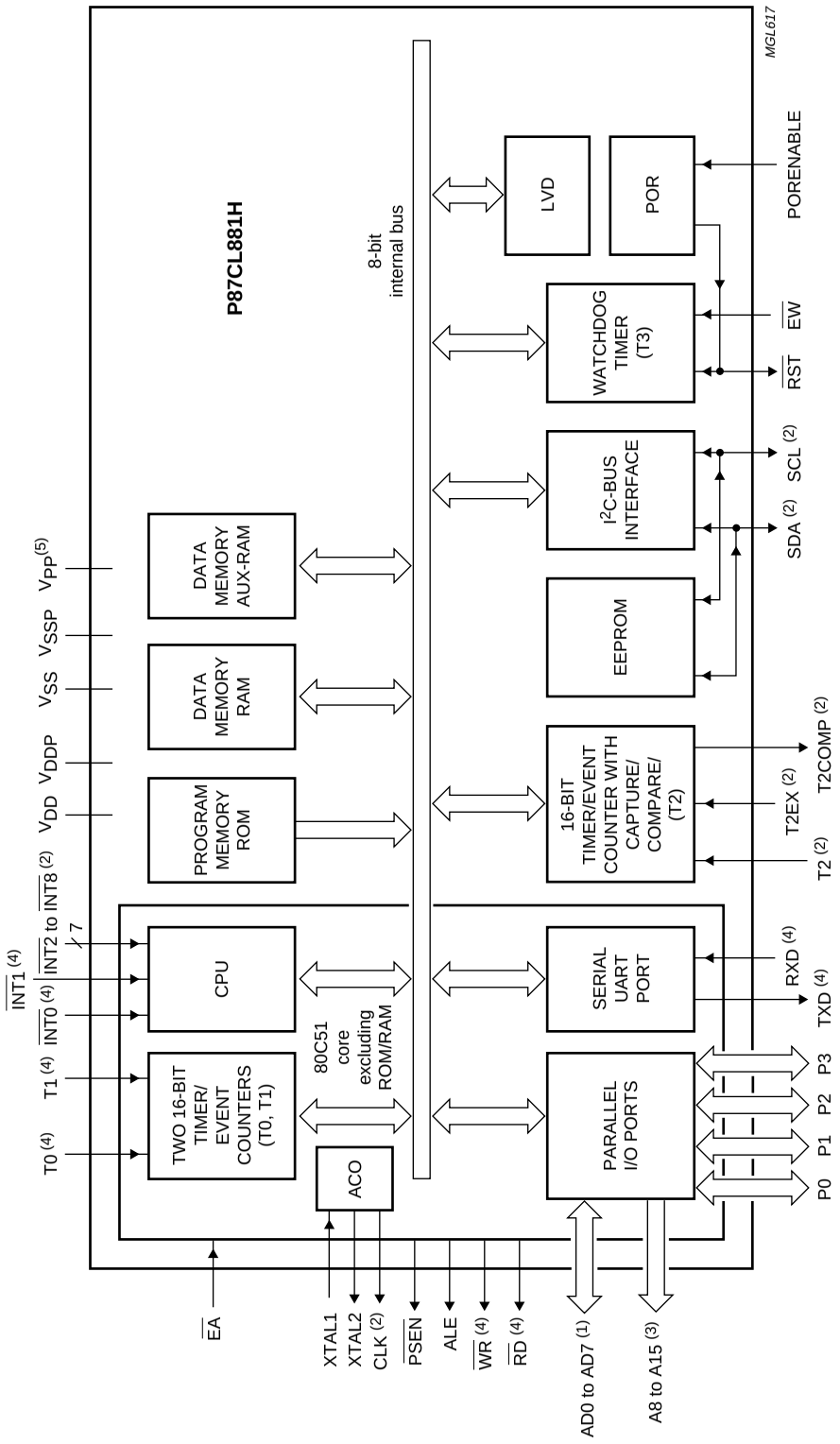


Fig.1 Block diagram.

(1) Alternative function of Port 0.
(2) Alternative function of Port 1.
(3) Alternative function of Port 2.
(4) Alternative function of Port 3.
(5) Alternative function of pin 6.

5 PINNING INFORMATION

5.1 Pinning

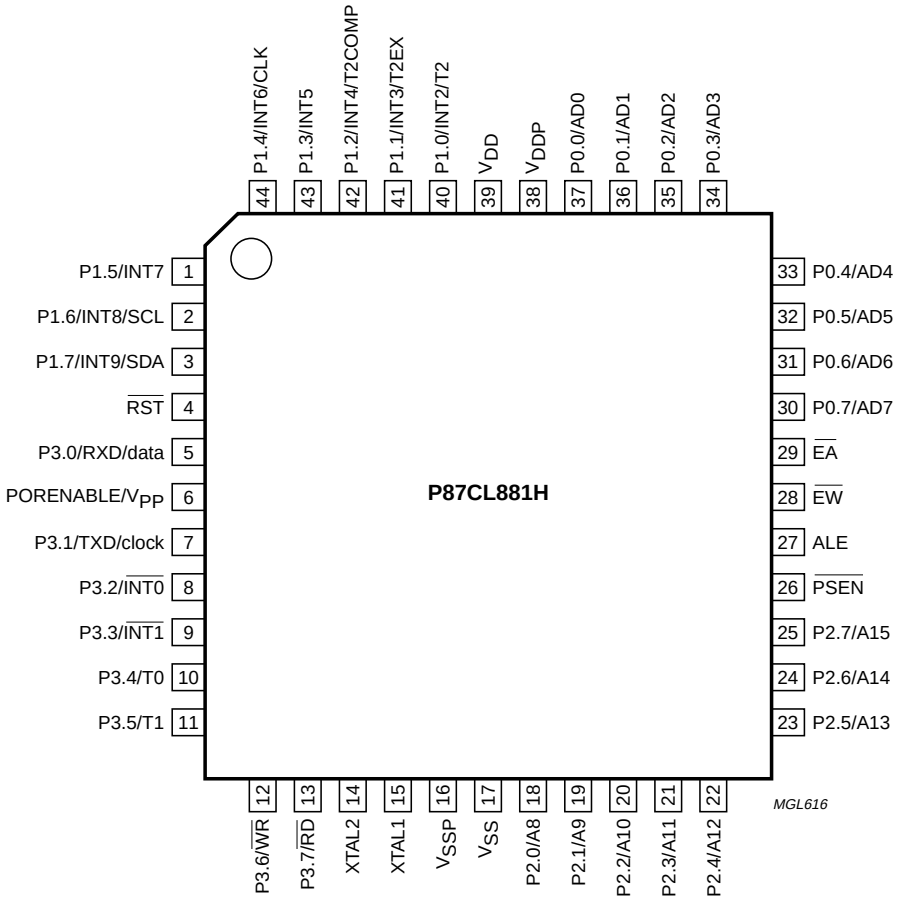


Fig.2 Pin configuration.

5.2 Pin description

Table 1 LQFP package

SYMBOL	PIN	DESCRIPTION
V_{DD}	39	**Power supply** for core.
V_{DDP}	38	**Power supply** for I/O ring.
V_{SS}	17	**Ground** for core.
V_{SSP}	16	**Ground** for I/O ring.
$\overline{RST}$	4	**RESET.** A LOW level on this pin for two machine cycles while the oscillator is running, resets the device. The $\overline{RST}$ pin is also an output which can be used to reset other ICs.
PORENABLE/V_{PP}	6	**PORENABLE.** If set to a logic 1, the internal Power-on reset circuit is enabled. If external reset circuitry is used, it is recommended to keep PORENABLE LOW in order to achieve the lowest power consumption. This pin is also used for the OTP programming voltage V_{PP}.
$\overline{EW}$	28	Enable Watchdog Timer.
XTAL2	14	**Crystal output.** Output of the amplitude controlled oscillator. If an external oscillator clock is used this pin not used.
XTAL1	15	**Crystal input.** Input to the amplitude controlled oscillator. Also the input for an externally generated clock source.
$\overline{PSEN}$	26	**Program Store Enable.** Read strobe to external program memory. When executing code out of external program memory, $\overline{PSEN}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{PSEN}$ activations are skipped. During Power-down mode the $\overline{PSEN}$ pin stays HIGH.
ALE	27	**Address Latch Enable.** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods and may be used for external timing or clocking purposes. For improved EMC behaviour, the toggle of the ALE pin can be disabled by setting the RFI bit in the PCON register by software. This bit is cleared on reset and can be set and cleared by software. When set, the ALE pin will be pulled-down internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE if external memory is accessed. ALE will retain its normal HIGH state during Idle mode and a LOW state during the Power-down mode while in the EMC mode. Additionally, during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal program memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, whether the RFI bit is set or not.
$\overline{EA}$	29	**External Access.** When $\overline{EA}$ is held HIGH, the CPU executes out of the internal program memory (unless the program counter exceeds the highest address for internal program memory). When $\overline{EA}$ is held LOW, the CPU executes out of external program memory regardless of the value of the program counter. The state of the $\overline{EA}$ pin is internally latched at reset.

SYMBOL	PIN	DESCRIPTION
P0.0/AD0	37	**Port 0.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. AD7 to AD0 provide the multiplexed low-order address and data bus during accesses to external memory.
P0.1/AD1	36	
P0.2/AD2	35	
P0.3/AD3	34	
P0.4/AD4	33	
P0.5/AD5	32	
P0.6/AD6	31	
P0.7/AD7	30	
P1.0/INT2/T2	40	**Port 1.** 8-bit bidirectional I/O port with alternative functions. Every port pin except P1.6 and P1.7 (I^2C-bus pins) can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 1 also serves the alternative functions INT2 to INT9 interrupts, Timer 2 external input and Timer 2 compare output, external clock output CLK and I^2C-bus clock and I^2C-bus data in/outputs.
P1.1/INT3/T2EX	41	
P1.2/INT4/ T2COMP	42	
P1.3/INT5	43	
P1.4/INT6/CLK	44	
P1.5/INT7	1	
P1.6/INT8/SCL	2	
P1.7/INT9/SDA	3	
P2.0/A8	18	**Port 2.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. Port 2 emits the high order address byte during accesses to external memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses the strong internal pull-ups when emitting logic 1's. During accesses to external memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
P2.1/A9	19	
P2.2/A10	20	
P2.3/A11	21	
P2.4/A12	22	
P2.5/A13	23	
P2.6/A14	24	
P2.7/A15	25	
P3.0/RXD/data	5	**Port 3.** 8-bit bidirectional I/O port with alternative functions. Every port pin can be used as open-drain, standard port, high-impedance input or push-pull output, according to Section 6.2. RXD/data is the serial port receiver data input (asynchronous) or data I/O (synchronous). TXD/clock is the serial port transmitter data output (asynchronous) or clock output (synchronous). $\overline{INT0}$ and $\overline{INT1}$ are external interrupt lines. T0 and T1 are external inputs for Timers 0 and 1 respectively. $\overline{WR}$ is the external memory write strobe and $\overline{RD}$ is the external memory read strobe.
P3.1/TXD/clock	7	
P3.2/$\overline{INT0}$	8	
P3.3/$\overline{INT1}$	9	
P3.4/T0	10	
P3.5/T1	11	
P3.6/$\overline{WR}$	12	
P3.7/$\overline{RD}$	13	

6 FUNCTIONAL DESCRIPTION

For the functional and block descriptions of the P87CL881, refer to the *"TELX family"* data sheet.

6.1 Special Function Registers

Table 2 Special Function Registers memory map and reset values; note 1

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
80C51 core			
Accumulator	ACC	E0H	0000 0000
B Register	B	F0H	0000 0000
Data Pointer Low byte	DPL	82H	0000 0000
Data Pointer High byte	DPH	83H	0000 0000
Program Counter High byte	PCH	no SFR	0000 0000
Program Counter Low byte	PCL	no SFR	0000 0000
Power Control Register	PCON	87H	0000 0000
Prescaler Register	PRESC	F3H	0000 0000
Program Status Word	PSW	D0H	0000 0000
Stack Pointer	SP	81H	0000 0111
XRAM Page Register	XRAMP	FAH	XXXX X000
Timers 0 and 1			
Timer/Counter Control Register	TCON	88H	0000 0000
Timer/Counter 0 High byte	TH0	8CH	0000 0000
Timer/Counter 1 High byte	TH1	8DH	0000 0000
Timer/Counter 0 Low byte	TL0	8AH	0000 0000
Timer/Counter 1 Low byte	TL1	8BH	0000 0000
Timer/Counter Mode Control Register	TMOD	89H	0000 0000
Ports			
Alternative Port Function Control Register	ALTP	A3H	0000 0000
Port P0 output data Register	P0	80H	1111 1111
Port P0 Configuration A Register	P0CFGA	8EH	1111 1111
Port P0 Configuration B Register	P0CFGB	8FH	0000 0000
Port P1 output data Register	P1	90H	0111 1111
Port P1 Configuration A Register	P1CFGA	9EH	0000 1000
Port P1 Configuration B Register	P1CFGB	9FH	0111 1111
Port P2 output data Register	P2	A0H	1111 1111
Port P2 Configuration A Register	P2CFGA	AEH	1111 1111
Port P2 Configuration B Register	P2CFGB	AFH	0000 0000
Port P3 output data Register	P3	B0H	1111 1111
Port P3 Configuration A Register	P3CFGA	BEH	1111 1110
Port P3 Configuration B Register	P3CFGB	BFH	1111 1111

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
Timer 2			
Timer 2 Compare High byte	COMP2H	ABH	0000 0000
Timer 2 Compare Low byte	COMP2L	AAH	0000 0000
Timer 2 Reload/Capture High byte	RCAP2H	CBH	0000 0000
Timer 2 Reload/Capture Low byte	RCAP2L	CAH	0000 0000
Timer/Counter 2 Control Register	T2CON	C8H	0000 0000
Timer/Counter 2 High byte	TH2	CDH	0000 0000
Timer/Counter 2 Low byte	TL2	CCH	0000 0000
Interrupt logic			
Interrupt Enable Register 0	IEN0	A8H	0000 0000
Interrupt Enable Register 1	IEN1	E8H	0000 0000
Interrupt Enable Register 2	IEN2	F1H	0000 0000
Interrupt Priority Register 0	IP0	B8H	0000 0000
Interrupt Priority Register 1	IP1	F8H	0000 0000
Interrupt Priority Register 2	IP2	F9H	0000 0000
Interrupt Sensitivity Register 1	ISE1	E1H	0000 0000
Interrupt Polarity Register	IX1	E9H	0000 0000
Interrupt Request Flag Register 1	IRQ1	C0H	0000 0000
Low Voltage Detection			
LVD Control Register	LVDCON	F2H	0000 0000
PORACO			
Reset Status Register	RSTAT	E6H	XXX1 1000
UART			
Serial Port Buffer	S0BUF	99H	0000 0000
Serial Port Control Register	S0CON	98H	0000 0000
I^2C-bus interface			
Address Register	S1ADR	DBH	0000 0000
Serial Control Register	S1CON	D8H	0000 0000
Data Shift Register	S1DAT	DAH	0000 0000
Serial Status Register	S1STA	D9H	1111 1000
Watchdog timer			
Watchdog Timer Control Register	WDCON	A5H	1010 0101
Watchdog Timer Interval Register	WDTIM	FFH	0000 0000

REGISTER NAME	REGISTER MNEMONIC	SFR ADDRESS	RESET VALUE(2)
OTP interface			
OTP Address High Register	OAH	D5	X00X XXXX
OTP Address Low Register	OAL	D4	XXXX XXXX
OTP Data Register	ODATA	D6	XXXX XXXX
OTP In-System Programming Register	OISYS	DC	000X 0000
OTP Test Register	OTEST	D7	0000 0000

Notes

1. E7H and FDH are reserved locations and must not be written to.
2. Where: X = undefined state.

6.2 I/O facilities

6.2.1 PORTS

The P87CL881 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the following alternative functions:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- P1.0 to P1.7 provides the inputs for the external interrupts INT2 to INT9
- P1.0/T2 and P1.1/T2EX for external inputs of Timer 2
- P1.2/T2COMP for external activation and compare output of Timer 2
- P1.4/CLK for the clock output
- P1.6/SCL and P1.7/SDA for the I^2C-bus interface are real open-drain outputs or high-impedance; no other port configurations are available.

Port 2 Provides the high-order address bus when expanding the device with external program memory and/or external data memory.

Port 3 Pins can be configured individually to provide:

- P3.0/RXD/data and P3.1/TXD/clock which are serial port receiver input and transmitter output (UART)
- P3.2/$\overline{\text{INT0}}$ and P3.3/$\overline{\text{INT1}}$ are external interrupt request inputs
- P3.4/T0 and P3.5/T1 as counter inputs
- P3.6/$\overline{\text{WR}}$ and P3.7/$\overline{\text{RD}}$ are control signals to write and read to external memories.

To enable a port pin alternative function, the port bit latch in its SFR must contain a logic 1.

Each port consists of a latch (Special Function Registers P0 to P3), an output driver and input buffer. All ports have internal pull-ups. Figure 3(a) shows that the strong transistor P1 is turned on for only 1 oscillator period after a LOW-to-HIGH transition in the port latch. When on, it turns on P3 (a weak pull-up) through the inverter IN1. This inverter and transistor P3 form a latch which holds the logic 1.

6.2.2 PORT I/O CONFIGURATION

I/O port output configurations are determined by the settings in the port configuration SFRs. Each port has two associated SFRs: PnCFGA and PnCFGB, where ‘n’ indicates the specific port number (0 to 3). One bit in each of the 2 SFRs relates to the output setting for the corresponding port pin, allowing any combination of the 2 output types to be mixed on those port pins.
For example, the output type of P1.3 is controlled by setting bit 3 in the SFRs P1CFGA and P1CFGB.

The port pins may be individually configured via the SFRs with one of the following modes (P1.6 and P1.7 can be open-drain or high-impedance but never have any diodes against V_{DD}).

Mode 0 Open-drain; quasi-bidirectional I/O with n-channel open-drain output. Use as an output (e.g. Port 0 for external memory accesses ($\overline{\text{EA}}$ = 0) or access above the built-in memory boundary) requires the connection of an external pull-up resistor. The ESD protection diodes against V_{DD} and V_{SS} are still present. Except for the I^2C-bus pins P1.6 and P1.7, ports which are configured as open-drain still have a protection diode to V_{DD}. See Fig.3a.

Mode 1 Standard port; quasi-bidirectional I/O with pull-up. The strong pull-up p1 is turned on for only one oscillator periods after a LOW-to-HIGH transition in the port latch. After these two oscillator periods the port is only weakly driven through p2 and 'very weakly' driven through p3. See Fig.3b.

Mode 2 High-impedance; this mode turns all port output drivers off. Thus, the pin will not source or sink current and may be used as an input-only pin with no internal drivers for an external device to overcome. See Fig.3c.

Mode 3 Push-pull; output with drive capability in both polarities. In this mode, pins can only be used as outputs. See Fig.3d.

Tables 2 and 3 show the configuration register settings for the four output configurations. The electrical characteristics of each output configuration are specified in Chapter 8. The default port configuration after reset is given in Table 2.

In case of external memory access, the appropriate options for ports P0, P2 and P3.6/P3.7 ($\overline{WR}$/$\overline{RD}$, only in case of external data memory access) must be set by software.

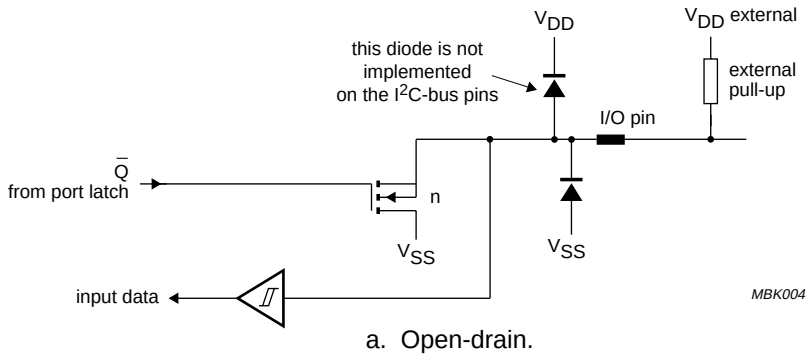
For Special Function Registers for port configurations/data please refer to Table 2, note 1.

Table 3 Port configuration register settings

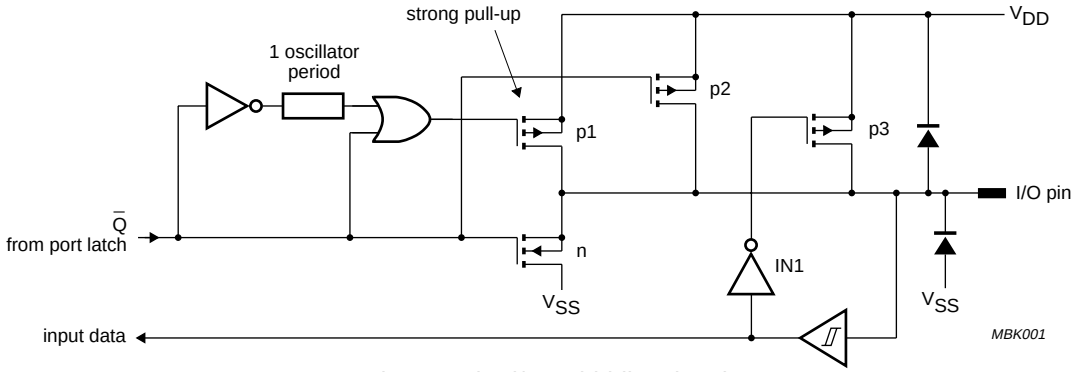
MODE(1)	PnCFGA	PnCFGB	PORT OUTPUT CONFIGURATION	
			NORMAL PORTS	I^2C-BUS PORTS (P1.6 AND P1.7)
0	0	0	open-drain	open-drain
1	1	0	quasi-bidirectional	open-drain
2	0	1	high-impedance	high-impedance
3	1	1	push-pull	open-drain

Note

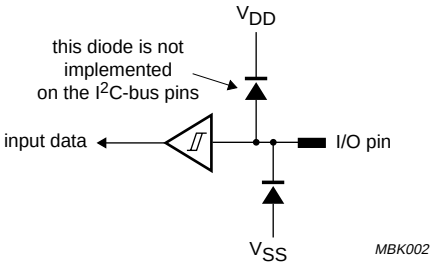
1. Mode changes may cause glitches to occur during transitions. When modifying both registers, write instructions should be carried out consecutively.



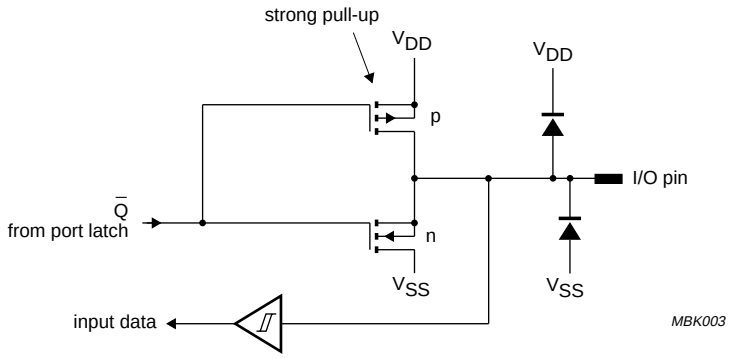
a. Open-drain.



b. Standard/quasi-bidirectional.



c. High-impedance.



d. Push-pull.

Fig.3 Port configuration options.

6.3 Internal data memory

The internal data memory is divided into three physically separated parts:

256 bytes of RAM, 128 bytes of Special Function Registers and 1792 bytes of AUX-RAM. These can be addressed each in a different way (see also Table 4).

1. RAM 0 to 127 can be addressed directly and indirectly as in the 80C51; address pointers are R0 and R1 of the selected register-bank
2. RAM 128 to 255 can only be addressed indirectly; address pointers are R0 and R1 of the selected register bank
3. AUX-RAM 0 to 1791 is indirectly addressable via the AUX-RAM Page Register (XRAMP) and MOVX-Ri instructions, unless it is disabled by setting ARD = 1. AUX-RAM 0 to 1791 is also indirectly addressable as external data memory via MOVX-datapointer instruction, unless it is disable by setting ARD = 1. When executing from internal program memory, an access to AUX-RAM 0 to 1791 when ARD = 0 will not affect the ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 1791 will be performed with the MOVX @ DPTR instructions in the same way as in the 80C51 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that the external data memory cannot be accessed with R0 and R1 as address pointer if the AUX-RAM is enabled (ARD = 0, default after reset).

The Special Function Registers (SFR) can only be addressed directly in the address range from 128 to 255.

Four register banks, each 8 registers wide, occupy locations 0 through 31 in the lower RAM area. Only one of these banks may be enabled at a time. The next 16 bytes, locations 32 through 47, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal 256 bytes RAM. The stack depth is only limited by the available internal RAM space of 256 bytes (see Fig.4).

Table 4 Internal data memory map

LOCATION	ADDRESS	ADDRESSING
RAM	0 to 127	direct and indirect
AUX-RAM	0 to 1791	indirect only with MOVX
RAM	128 to 255	indirect only
SFR	128 to 255	direct only

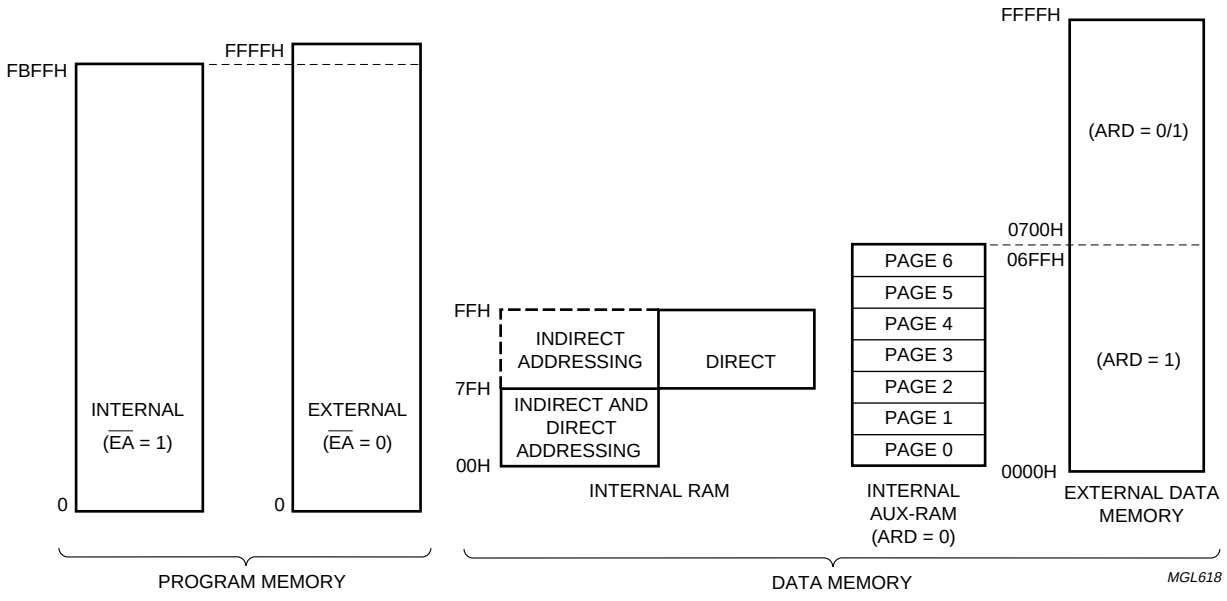


Fig.4 Memory map.

6.3.1 AUX-RAM PAGE REGISTER (XRAMP)

The AUX-RAM Page Register is used to select one of the seven 256 bytes pages of the internal 1792-byte AUX-RAM for MOVX-accesses via R0 or R1. Its reset value is 'XXXX X000' (AUX-RAM page 0).

Table 5 AUX-RAM Page Register (SFR address FAH)

7	6	5	4	3	2	1	0
–	–	–	–	–	XRAMP2	XRAMP1	XRAMP0

Table 6 Description of XRAMP bits

BIT	SYMBOL	FUNCTION
7 to 3	–	reserved, undefined during read, a write operation must write logic 0 to these locations
2	XRAMP2	AUX-RAM page select bit 2
1	XRAMP1	AUX-RAM page select bit 1
0	XRAMP0	AUX-RAM page select bit 0

Table 7 Memory locations for all possible MOVX accesses

ARD(1)	XRAMP2	XRAMP1	XRAMP0	ACCESS	INSTRUCTION TYPE
0	0	0	0	AUX-RAM page 0 (address 0 to 255)	MOVX @ Ri, A and MOVX @ A, Ri
0	0	0	1	AUX-RAM page 1 (address 256 to 511)	
0	0	1	0	AUX-RAM page 2 (address 512 to 767)	
0	0	1	1	AUX-RAM page 3 (address 768 to 1023)	
0	1	0	0	AUX-RAM page 4 (address 1024 to 1279)	
0	1	0	1	AUX-RAM page 5 (address 1280 to 1535)	
0	1	1	0	AUX-RAM page 6 (address 1536 to 1791)	
0	1	1	1	no valid memory access	
1	X	X	X	external RAM locations 0 to 255	
0	X	X	X	AUX-RAM locations 0 to 1791 external RAM locations 1792 to 65535	MOVX @ DPTR, A and MOVX A, DPTR
1	X	X	X	external RAM locations 0 to 65535	

Note

1. ARD (AUX-RAM Disable) corresponds to bit 6 in the Special Function Register PCON (address 87H).

6.4 OTP programming

6.4.1 OTP PROGRAMMING

The 63-kbyte One-Time Programmable (OTP) memory can be programmed by using an OM4260 programmer together with a programmer adapter OM5510. Since the memory is programmable only once, programming an already programmed address results in a logical AND of the old and new code. The OTP code can be read out by the programmer for verification.

6.4.1.1 Signature bytes

The OTP memory contains three signature bytes which can be read by the programmer to identify the device. A special address space has been used for these bytes which does not influence the user address space. The values of the signature bytes are:

(030H) = 15H, indicates manufactured by Philips Semiconductors

(031H) = D6H, indicates P87CL881H

(060H) = 00H, currently not used.

6.4.2 IN-SYSTEM PROGRAMMING MODE

In the In-System Programming mode the OTP can be programmed under control of the CPU. A program to control programming has to be available in the OTP. This mode can be used to program several bytes in the OTP if the chip is already in a system e.g. to store tuning parameters.

In the In-System Programming mode the complete address space OTP can be programmed.

The user should take care not to overwrite the existing code.

For In-System Programming four SFRs are used to control the OTP.

Table 8 SFRs for In-System Programming

SFR NAME	DESCRIPTION
OAH	OTP Address High Register
OAL	OTP Address Low Register
ODATA	OTP Data Register
OISYS	OTP In-System Register

6.4.2.1 OTP In-System Programming Register (OISYS)

The OISYS SFR controls the In-System Programming mode. The data that has to be programmed is stored in the SFR ODATA and the address for this data in the SFRs OAH and OAL.

Table 9 OTP In-System Programming Register (SFR address DCH)

7	6	5	4	3	2	1	0
–	–	–	VPon	0	SIG	WE	InSysMode

Table 10 Description of OISYS bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	These bits are reserved.
4	VPon	V_{PP} status (read only).
3	0	This bit is reserved and must be kept to logic 0.
2	SIG	Signature bytes enable.
1	WE	Write Enable, enables programming.
0	InSysMode	In-System Programming status bit.

6.4.2.2 *Mode entry*

The In-System Programming mode is entered by setting the InSysMode bit of the OISYS SFR. The I^2C-bus is used for data transfer in this mode. If the I^2C-bus interface is addressed by an external master, the interface generates an interrupt request. The interrupt handler can now read the OISYS SFR and determine the status of the external high voltage (VPon). If high voltage is not present the interrupt is a standard I^2C-bus interrupt.

If high voltage is present the In-System program interrupt routine has to start that writes the InSysMode bit (OISYS.0) and controls the address and data transfer.

The program voltage has to be available and stable for at least 10 μs before the mode is entered and has to be stable until the circuit has left the In-System Programming mode. The high voltage can be applied for maximum 60 seconds during the complete lifetime of the circuit.

6.4.2.3 *Program cycle*

The data and address must be supplied to the microcontroller and the control program has to write the SFRs: ODATA, OAH and OAL. A timer has to be initialized for a 100 μs cycle and the WE bit of the OISYS SFR must be set. Now the core has to be set into Idle mode. As long as the circuit is in Idle mode a programming pulse is applied. After the interrupt request of the timer the OTP is available for normal code fetching.

The address applied to the OAH and OAL SFRs must be in the 63 kbytes address space.

6.4.2.4 *Verify for In-System Programming*

Verify is done in similar way as programming. The circuit is put into Idle mode and at the start of this mode the sense amplifiers are switched to verify mode and a read cycle is started. The timer has to be initialized for a cycle of at least 1 μs. The address is supplied by the SFRs OAH and OAL. The WE bit of the OISYS SFR has to be reset. The OTP output data is latched in the ODATA SFR. After Idle mode is finished this SFR can be read in a normal way. To be sure that the verified data is written into the SFR it is advised to write FFH into the ODATA SFR before a verify is started.

6.4.2.5 *Signature bytes*

The signature bytes can be read by setting the SIG bit of the OISYS SFR and applying the address of the signature byte. Applying a write pulse while the SIG bit of the OISYS SFR is HIGH is forbidden although the contents of the signature bytes will never be destroyed.

The signature bytes (and other test addresses) are always readable independent of the security.

6.4.2.6 *How to connect the PORENABLE/V_{PP} pin in the In-System Programming mode*

If the V_{PP} pin is dual-mode (e.g. PORENABLE/V_{PP}), ICs connected to the signal PORENABLE must be able to withstand up to 13 V, i.e. cannot have clamping diodes or low break-down voltages. If the pin is connected to a fixed voltage (V_{DD} or V_{SS}) there must be a way of switching-off this connection on the PCB. A possible implementation is presented in Fig.5.

In the example (see Fig.5) the POR is enabled in normal mode of operation (pin PORENABLE/V_{PP} = 1 by the pull-up), but the V_{PP} source must supply enough current in R_p in order to guarantee a minimum 12.5 V on the PORENABLE/V_{PP} pin.

Note that if in the application the Power-on reset is disabled (pin PORENABLE/V_{PP} = 0), applying a high voltage to the PORENABLE/V_{PP} pin will also enable the POR circuit. This will cause a reset independent of the actual V_{DD} value.

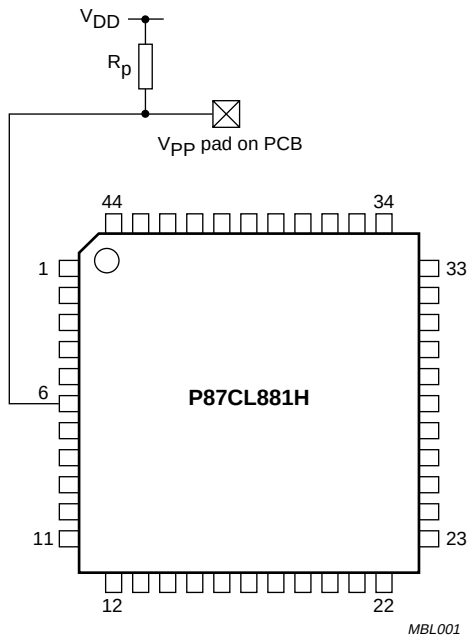


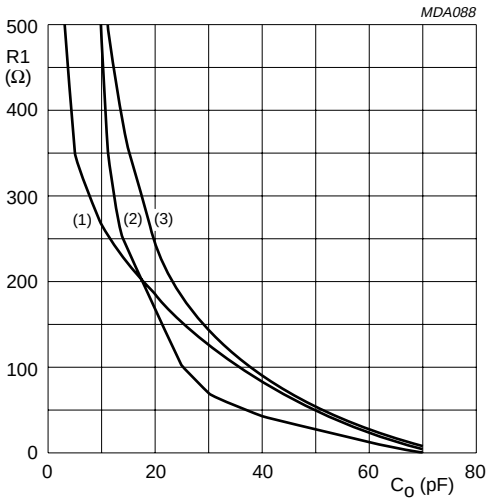
Fig.5 Example of PORENABLE/V_{PP} connection on a PCB.

6.5 Oscillator circuitry

General information on the oscillator circuitry can be found in the *"TELX family"* data sheet.

6.5.1 RESONATOR REQUIREMENTS

For correct function of the oscillator, the values of R_1 and C_0 of the chosen resonator (quartz or PXE) must be below the line shown in Fig.6a. The value of the parallel resistor R_0 must be less than 47 kΩ. The wiring between chip and resonator should be kept as short as possible.



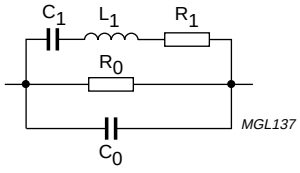
C_{1e} and C_{2e} are the external load capacitances; normally not needed due to integrated load capacitances of typically 10 pF.

(1) $C_{1e} = C_{2e} = 22$ pF.

(2) $C_{1e} = C_{2e} = 0$ pF.

(3) $C_{1e} = C_{2e} = 12$ pF.

a. Resonator curves for 3.58 MHz.



b. Resonator equivalent circuit.

Fig.6 Resonator requirements for the ACO.

6.6 Non-conformance

6.6.1 PROGRAMMING INTERFACE/TRANSPARENT MODE

The transparent mode is a special operating mode of the microcontroller used for parallel and In-System OTP programming.

For certain combinations of data written to Port 2 (used for control signal during parallel programming mode) the Transparent mode may be incorrectly active during normal operation of the microcontroller. In this case, a transition on any of the Port 0 pins can influence the read out of the on-chip program memory resulting in incorrect code execution.

To avoid this problem, the InSysMode bit in the OTP In-System Programming Register (SFR address DCH) **must** be set in the start-up sequence of the program code.

Apart from preventing incorrect operation as described above, the setting of this bit does not affect the normal operation.

6.6.2 MOVC INSTRUCTION LIMITATION

The 'MOVC' access to a data or program byte stored in internal ROM/OTP-memory is inhibited while fetching code from external program memory in roll-over mode.

Roll-over mode means that the CPU executes code out of the external program memory because the program counter exceeds the highest address for internal program memory. The affected address range is FC00H to FFFFH.

6.6.3 LOW VOLTAGE DETECTION

The LVDI bit (LVDCON.6) may be incorrectly set due to a glitch on the LVD output when the LVD is enabled by changing the bits LVDCON<3:0> from '0000' to any value within the range '0001' to '0101'. If bit EA in register IEN0 is enabled, an unwanted interrupt may occur.

A software workaround for this problem exist. During the initialisation sequence:

- Enable LVD by writing to register LVDCON
- Enable LVD interrupt by writing to register IEN2
- Clear the LVDI bit by writing to LVDCON a second time
- Set bit EA in register IEN0 (ensures LVDI to be cleared after initialisation).

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+4.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	–	800	mW
T_{stg}	storage temperature	–65	+150	°C

8 DC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; V_{SS} = 0 V; f_{xtal} = 1 to 10 MHz; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.7	–	3.6	V
	RAM data retention in Power-down mode		1.0	–	3.6	V
V_{PP}	OTP programming voltage		12.5	–	13.0	V
I_{DD}	supply current operating	V_{DD} = 3 V; f_{xtal} = 7 MHz; note 1	–	–	4.8	mA
		T_{amb} = 25 °C	–	3.7	–	mA
$I_{DD(id)}$	supply current Idle mode	V_{DD} = 3 V; f_{xtal} = 7 MHz; note 2	–	–	0.7	mA
		T_{amb} = 25 °C	–	0.58	–	mA
$I_{DD(pd)}$	supply current Power-down mode	V_{DD} = 3 V; T_{amb} = 25 °C; note 3				
		POR and LVD enabled	–	2	5	µA
		POR and LVD disabled	–	50	–	nA
$I_{DD(block)}$	supply current per block:	V_{DD} = 3 V; f_{xtal} = 7 MHz; T_{amb} = 25 °C; notes 4 and 5				
	Watchdog		–	220	–	µA
	I^2C-bus		–	180	–	µA
	UART		–	180	–	µA
	Timer T2		–	180	–	µA
	Timer T0 or T1		–	10	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs (ports, $\overline{RST}$ and PORENABLE)						
V_{IL}	LOW-level input voltage	notes 6 and 7	0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage	note 6	$0.8V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	LOW-level input current (ports in Mode 1)	V_{IN} = 0.4 V; note 8 and Fig.8	–	10	50	µA
$\lvert I_{IL(T)} \rvert$	LOW-level input current; HIGH-to-LOW transition (ports in Mode 1)	$V_{IN} = 0.2V_{DD}$; note 8 and Fig.8	–	200	1000	µA
$\lvert I_{ILEAK} \rvert$	input leakage current (ports in Mode 0 or 2)	$V_{SS} \leq V_I \leq V_{DD}$	–	–	1	µA
Outputs (ports and $\overline{RST}$)						
I_{OL}	LOW-level output current; except SDA and SCL	V_{OL} = 0.4 V	2	–	–	mA
I_{OL2}	LOW-level output current; SDA and SCL	V_{OL} = 0.4 V; note 9	3	–	–	mA
I_{OH}	HIGH-level output current except (push-pull options only)	$V_{OH} = V_{DD} - 0.4$ V	2	–	–	mA
$I_{\overline{RST}}$	$\overline{RST}$ pull-up current source	V_{DD} = 3 V; $V_{OH} = V_{DD} - 0.4$ V	0.05	0.2	–	µA
		V_{DD} = 3 V; $V_{OH} = V_{SS}$	–	0.6	2.5	µA
POR (Power-on reset) for the LVD (Low Voltage Detection), see note 10						
V_{PORH}	trip level HIGH	(option 5 in *"TELX family specification"*)	2.13	2.37	2.61	V
V_{PORL}	trip level LOW	(option B in *"TELX family specification"*)	–	1.30	–	V
ACO (Amplitude Controlled Oscillator)						
V_{XTAL1}	external clock signal amplitude peak-to-peak		500	–	V_{DD}	mV
$z_{i(XTAL1)}$	input impedance on XTAL1		300	1000	–	kΩ
C_{1i}; C_{2i}	input capacitance on XTAL1 and XTAL2	notes 5 and 11	–	10	–	pF
In-System Programming for the OTP						
t_{prog}	program cycle time		90	100	110	µs
$t_{prog(security)}$	program cycle time security	note 12	180	200	220	µs
t_{ver}	verify cycle time		1	–	–	µs
$t_{VPP(setup)}$	program voltage setup time		10	–	–	µs
$t_{VPP(max)}$	maximum program voltage time	cumulative for the product lifetime	–	–	60	s
I_{VPP}	program voltage current	In-System Programming	–	–	40	mA

Notes

1. The operating supply current is measured with all output pins disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{RST} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; fetch of NOP instructions; all derivative blocks disabled.
2. The Idle mode supply current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 driven with square wave; XTAL2 not connected; all derivative blocks disabled.
3. The power-down current is measured with all output pins and $\overline{RST}$ disconnected; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL1 and XTAL2 not connected.
4. The typical currents are only for the specific block. To calculate the typical power consumption of the microcontroller, the current consumption of the CPU must be added. Example: the typical current consumption of the microcontroller in operating mode with CPU, Watchdog and UART active can be calculated as (3.7 + 0.220 + 0.18) mA = 4.1 mA at V_{DD} = 3 V and f_{XTAL} = 7 MHz.
5. Verified on sampling basis.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1.
7. For pin PORENABLE the V_{IL} max is $0.1V_{DD}$.
8. Not valid for pins SDA, SCL, $\overline{RST}$ and PORENABLE.
9. The maximum allowed load capacitance C_L is in this case limited to around 200 pF.
10. The LVD is tested according to the *"TELX family specification, Chapter - Low voltage detection"*.
11. C_{1i}/C_{2i} are the total internal capacitances (including gate capacitance and leadframe capacitance).
12. Can also be done by two 100 μs pulses.

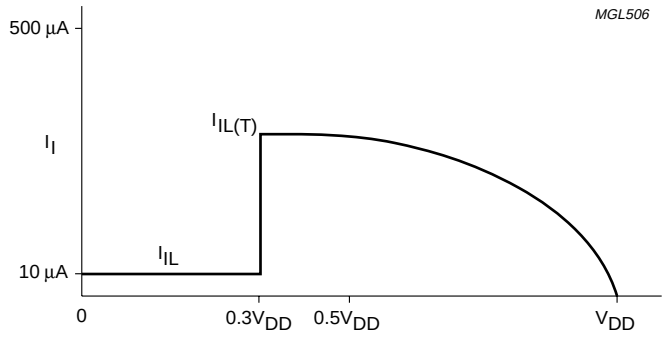


Fig.7 Input current.

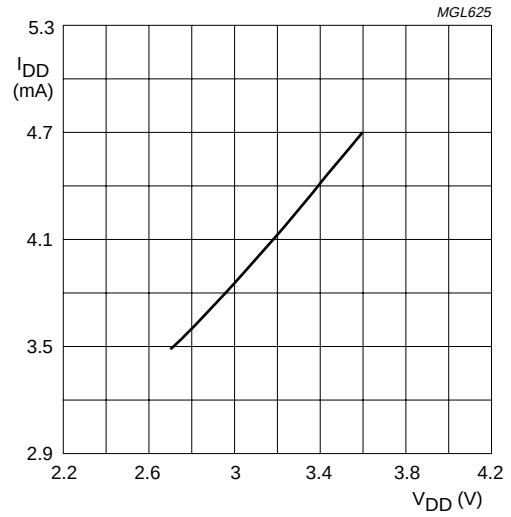


Fig.8 Typical operating current as a function of V_{DD}; T_{amb} = 25 °C; f_{xtal} = 7 MHz.

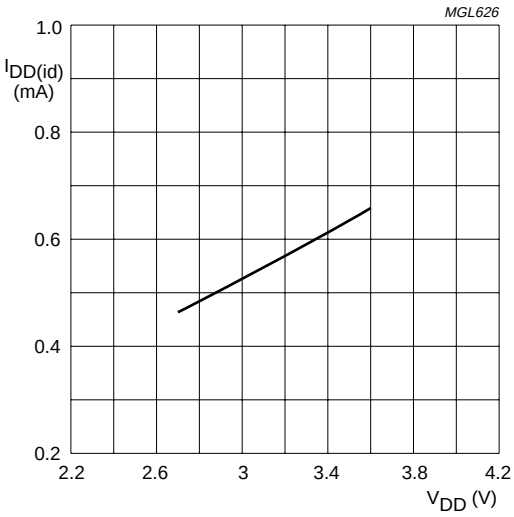
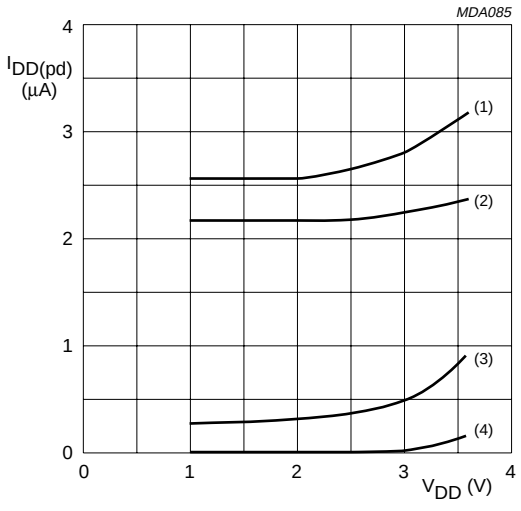


Fig.9 Typical Idle current as a function of V_{DD}; T_{amb} = 25 °C; f_{xtal} = 7 MHz.



(1) POR and LVD enabled (T_{amb} = 70 °C).
(2) POR and LVD enabled (T_{amb} = 25 °C).
(3) POR and LVD disabled (T_{amb} = 70 °C).
(4) POR and LVD disabled (T_{amb} = 25 °C).

Fig.10 Typical power-down current as a function of V_{DD}.

9 AC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified. All values verified on sampling basis.

SYMBOL	PARAMETER	VARIABLE CLOCK		UNIT
		MIN.	MAX.	
External program memory				
t_{LHLL}	ALE pulse width	t_{CLK}	–	ns
t_{AVLL}	address valid to ALE LOW	$0.5t_{CLK} - 10$	–	ns
t_{LLAX}	address hold after ALE LOW	$0.5t_{CLK}$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	$2t_{CLK} - 25$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	$0.5t_{CLK}$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	$1.5t_{CLK}$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	$1.5t_{CLK} - 35$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	$0.5t_{CLK}$	ns
t_{AVIV}	address to valid instruction in	–	$2.5t_{CLK} - 35$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	–	5	ns
External data memory				
t_{RLRH}	$\overline{RD}$ pulse width	$3t_{CLK}$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	$3t_{CLK}$	–	ns
t_{AVLL}	address valid to ALE LOW	$0.5t_{CLK}$	–	ns
t_{LLAX}	address hold after ALE LOW	$0.5t_{CLK}$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	$2.5t_{CLK}$	ns
t_{RHDX}	data hold after $\overline{RD}$	0	–	ns
t_{RHDZ}	data float after $\overline{RD}$	–	t_{CLK}	ns
t_{LLDV}	ALE LOW to valid data in	–	$4t_{CLK}$	ns
t_{AVDV}	address to valid data in	–	$4.5t_{CLK} - 30$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	$1.5t_{CLK} - 15$	$1.5t_{CLK} + 15$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	$2t_{CLK}$	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	$0.5t_{CLK}$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	$3.5t_{CLK}$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	$0.5t_{CLK}$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	0	ns

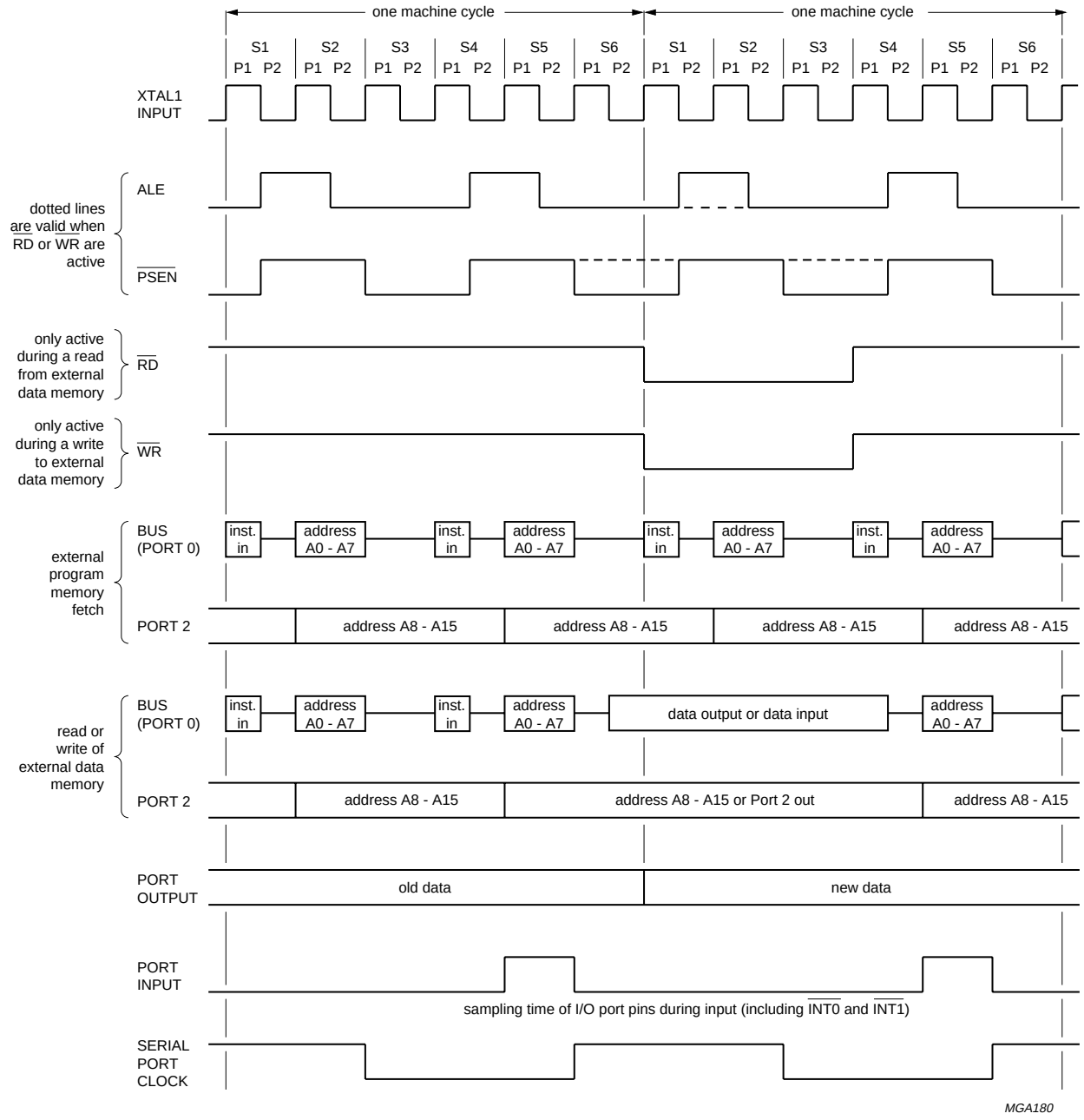


Fig.11 Instruction cycle timing.

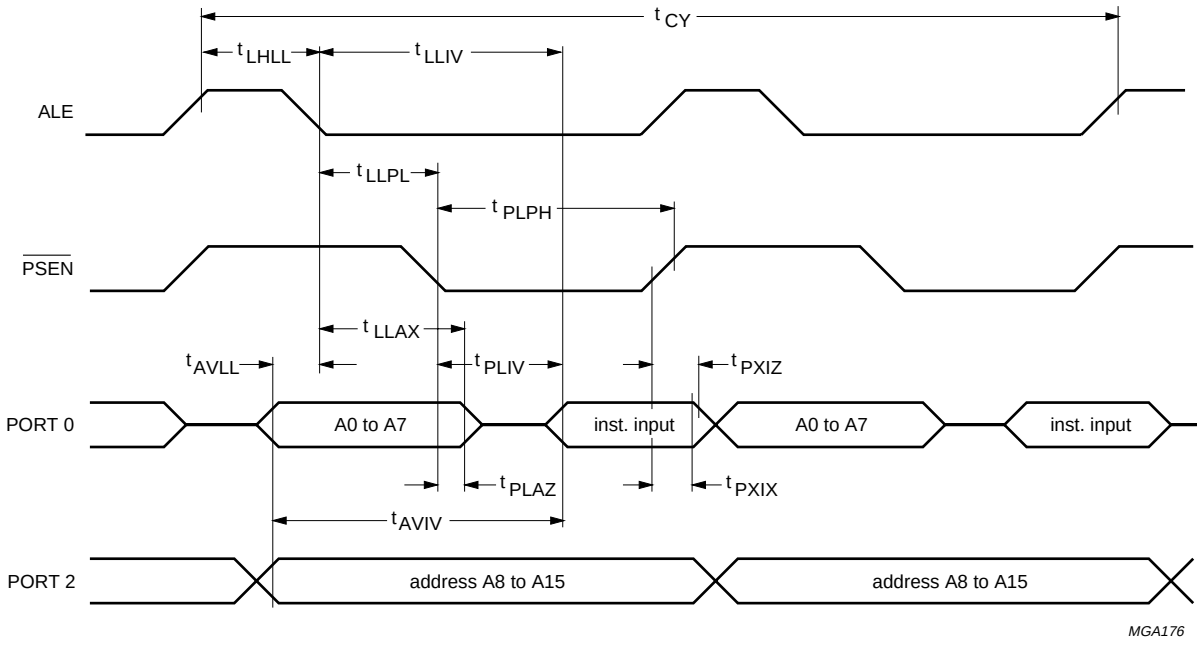


Fig.12 Read from external program memory.

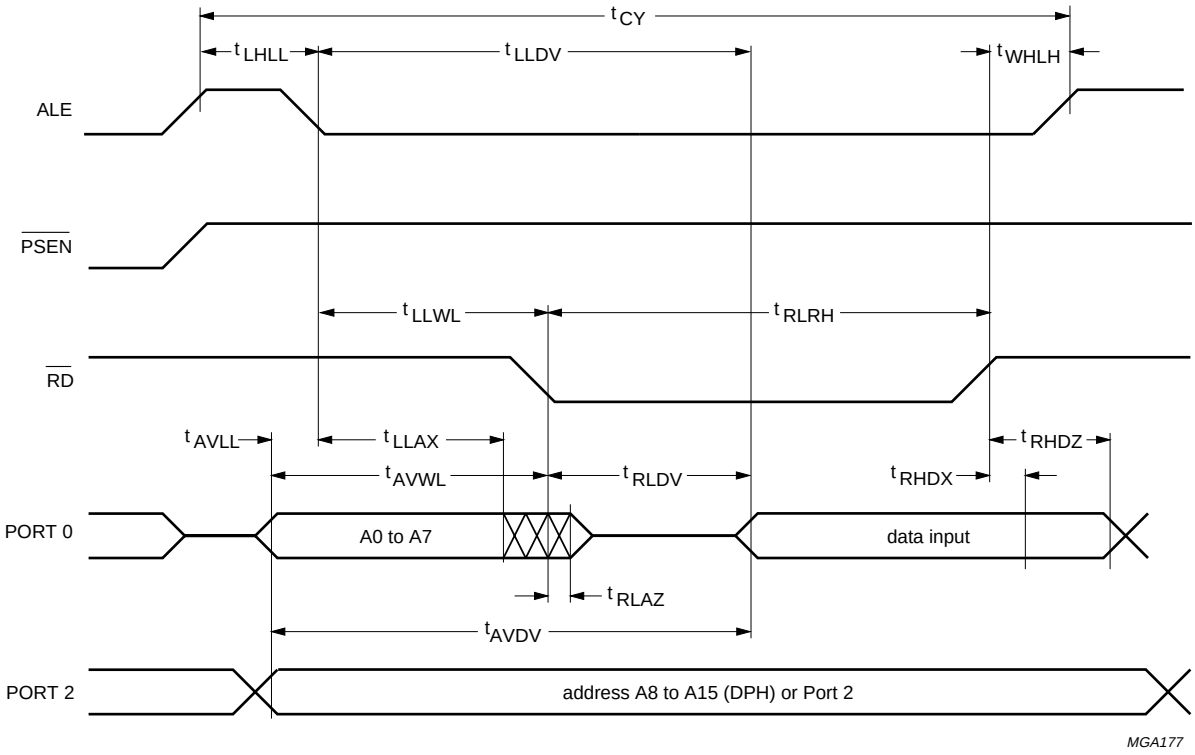


Fig.13 Read from external data memory.

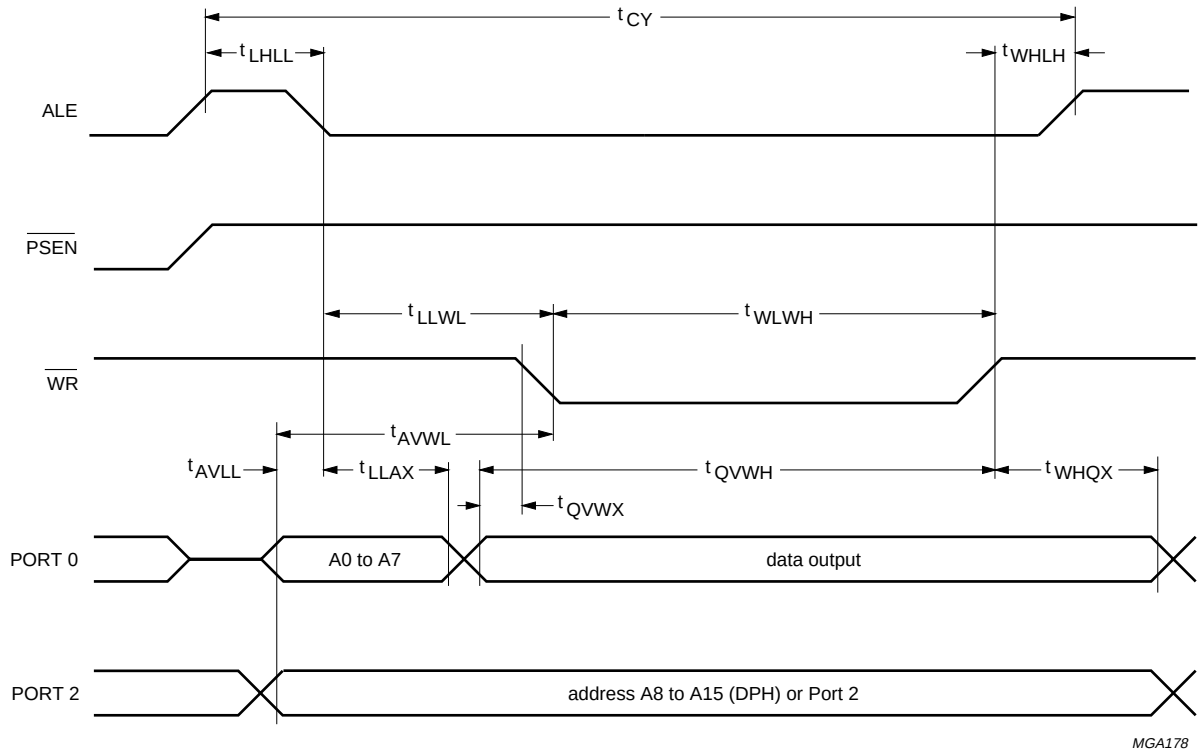
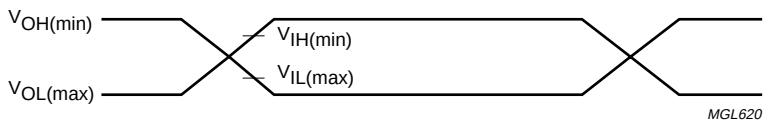


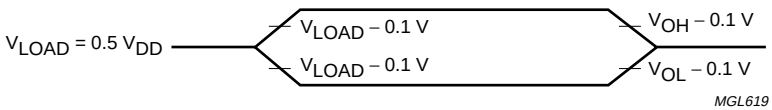
Fig.14 Write to external data memory.

9.1 AC testing

AC testing inputs are driven at 2.4 V for a HIGH level and 0.45 V for a LOW level. Timing measurements are taken at 2.0 V for a HIGH level and 0.8 V for a LOW level, see Fig.15a. The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 μA at the voltage test levels, see Fig.15b.



a. AC inputs during testing are driven at $V_{OH(min)}$ for a logic 1 and $V_{OL(max)}$ for a logic 0. Timing measurements are made at $V_{IH(min)}$ for a logic 1 and $V_{IL(max)}$ for a logic 0.

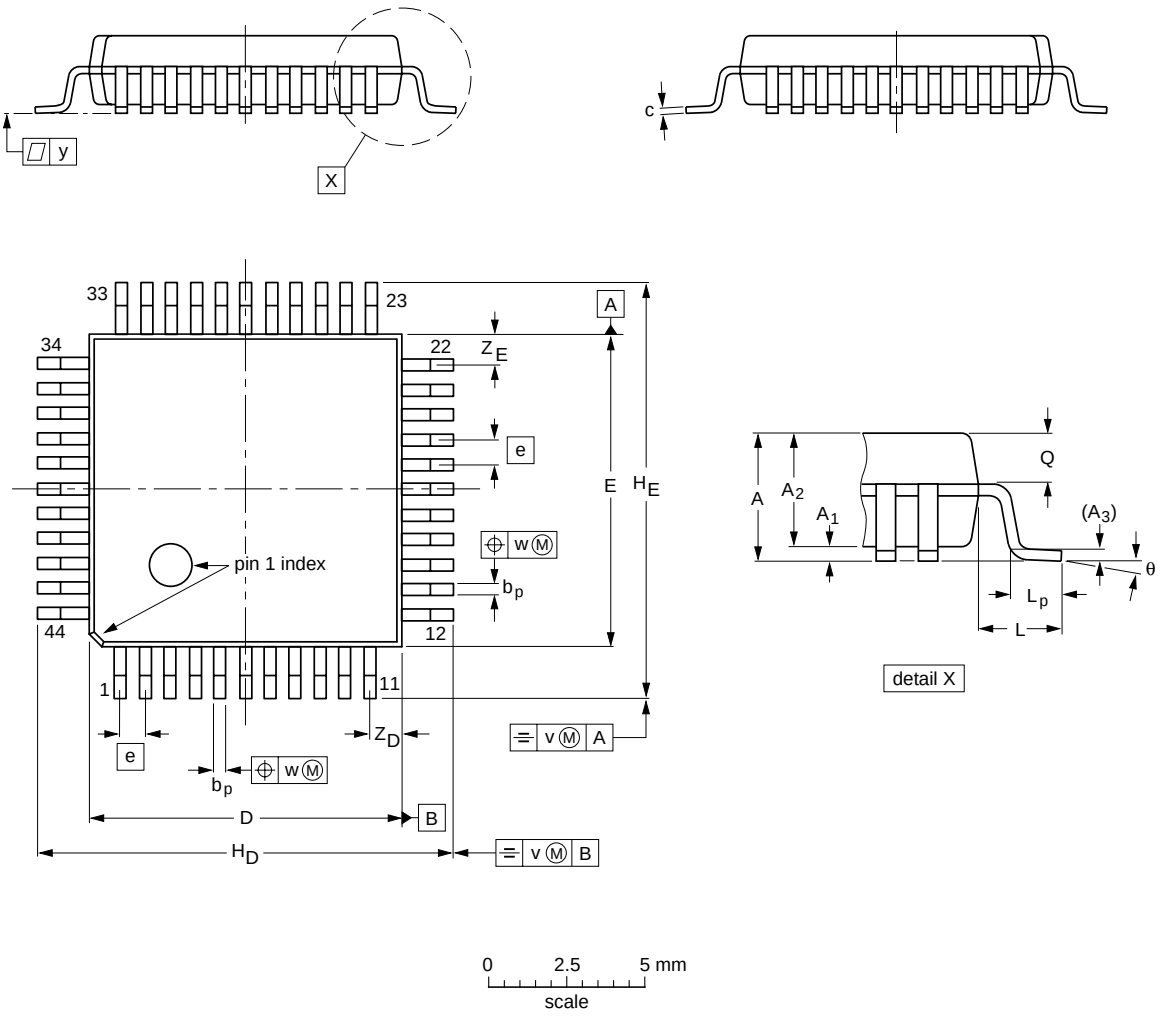


b. For timing purposes, a port is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} > 1.6$ mA.

Fig.15 AC testing input, output waveform (a) and float waveform (b).

10 PACKAGE OUTLINE

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.10 9.90	10.10 9.90	0.80	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.70 0.57	0.20	0.20	0.10	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT389-1						95-12-19

11 SOLDERING

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

12 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

13 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

14 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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