POSITIVE / PSEUDO ECL (PECL) CLOCK TERMINATION NETWORK

Features
- Stable resistor network
- Reduces power dissipation on the clock lines
- Ideal for high-speed clock termination
- Reduces board space by 70% vs. 1206 discretes and component count by more than 50%

Applications
- PECL clock termination

Application Note

High speed microprocessors line Intel's Pentium/P6®, Apple PowerPC®, SPARC® and other CISC and RISC based systems need well-controlled and precise clock signals to maintain a synchronous systems. The fast edge rated clock signals will exhibit transmission line effects on the clock lines resulting in undershoots and overshoots. The integrated PECL termination is designed to suppress the undershoots and overshoots on the clock lines. The PECL RC terminator dissipates very low power compared to the resistor termination network.

Why thin.film R networks? The PECL termination is an integrated R network fabricated on a silicon substrate using advanced thin film technology. This will have a fixed time constant and will not create additional skew on the clock lines. It has a low parasitic inductance compared to discrete and conventional thick film R terminators and provide effective termination at high frequencies.

STANDARD VALUES		
$R_1 (\Omega) \pm 1\%$	$R_2 (\Omega) \pm 1\%$	$R_3 (\Omega) \pm 1\%$
50	50	46.4
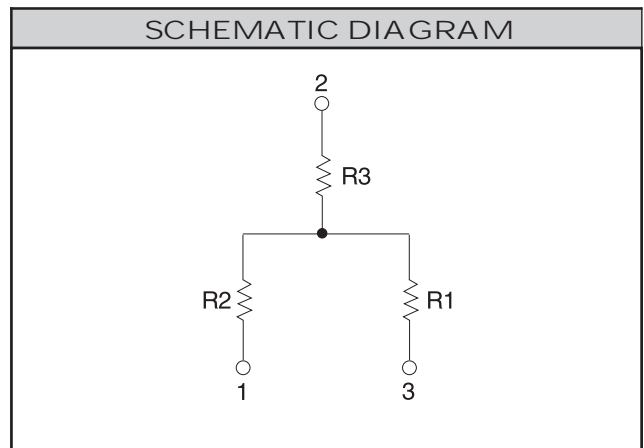
SCHEMATIC DIAGRAM

STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Pins	Style	Part Marking
3	SOT-23	PRN299

When placing an order please specify desired shipping: Tubes or Tape & Reel.

ABSOLUTE MAXIMUM RATINGS		
Parameter	Rating	Unit
V_{CC1}, V_{CC2}, V_{CC3} & V_{CC4} supply voltage	GND-0.5, +6.0	V
Diode D1 forward current	100	uA
DC voltage at inputs:		V
VIDEO_1, VIDEO_2, VIDEO_3	GND-0.5, V_{CC1}+0.5	V
TERM_1, TERM_2, TERM_3	-6.0, +6.0	V
DDC_IN1, DDC_IN2	GND-0.5, V_{CC2}+0.5	
DDC_OUT1, DDC_OUT2	GND-0.5, V_{CC3}+0.5	V
SYNC_IN1, SYNC_IN2	GND-0.5, V_{CC4}+0.5	V
Temperature:		
Storage	-40 to +150	ºC
Operating Ambient	0 to +70	ºC
Package power dissipation	1.0	W

| ELECTRICAL OPERATING CHARACTERISTICS (over operating conditions unless specified otherwise)						
Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	V_{CC1} = 5V; VIDEO inputs at V_{CC1} or GND			10	uA
$I_{CC2,3}$	V_{CC2}, V_{CC3} supply current	V_{CC2} = V_{CC3} = 5V			10	uA
I_{CC4}	V_{CC4} supply current	V_{CC4} = 5V; SYNC inputs at GND or V_{CC4}; PWR_UP pin at V_{CC4}; SYNC outputs unloaded		10		uA
		V_{CC4} = 5V; SYNC inputs at 3.0V; PWR_UP pin at V_{CC4}; SYNC outputs unloaded		200		uA
		V_{CC4} = 5V; PWR_UP input at GND; SYNC outputs unloaded			10	uA
V_{BIAS}	V_{BIAS} open circuit voltage	No external current drawn from V_{BIAS} pin		V_{CC4}-0.8		V
R_T	VIDEO termination resistance		71.25	75	78.75	Ω
	R_T resistance matching			1	2	%
V_{IH}	Logic High input voltage[1]	V_{CC4} = 5.0V	2.0			V
V_{IL}	Logic Low input voltage[1]	V_{CC4} = 5.0V			0.8	V
V_{OH}	Logic High output voltage[1]	I_{OH} = -4mA, V_{CC4} = 5.0V	4.4			V
V_{OL}	Logic Low output voltage[1]	I_{OL} = 4mA, V_{CC4} = 5.0V			0.4	V
R_b, R_p	Resistor value	PWR_UP, V_{CC3} = 5.0V	0.5	1	2	MΩ
R_c	V_{CC2} pull-down resistor	V_{CC2} = 3.0V	0.5	1.5	3	MΩ
I_{IN}	Input current					
	VIDEO inputs	V_{CC1} = 5V; V_{IN} = V_{CC1} or GND			±1	μA
	HSYNC, VSYNC inputs	V_{CC4} = 5V; V_{IN} = V_{CC4} or GND			±1	μA
I_{OFF}	OFF state leakage current, level shifting NFET	(V_{CC2} - V_{DDC_IN}) ≤ 0.4V; V_{DDC_OUT} = V_{CC2}			10	μA
		(V_{CC2} - V_{DDC_OUT}) ≤ 0.4V; V_{DDC_IN} = V_{CC2}			10	μA
V_{ON}	Voltage drop across level shifting NFET when turned ON	V_{CC2} = 2.5V; V_S = GND, I_{DS} = 3mA			0.15	V
C_{IN}	Input capacitance [3] VIDEO_1, VIDEO_2, VIDEO_3	V_{CC1} = 5.0V; V_{IN} = 2.5V; measured at 1MHz		4.0		pF
		V_{CC1} = 2.5V; V_{IN} = 1.25V; measured at 1MHz		4.5		
t_{PLH}	SYNC drivers L-H propagation delay	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		8	12	ns
t_{PHL}	SYNC drivers H-L propagation delay	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		8	12	ns
t_r, t_f	SYNC drivers output rise & fall times	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		7		ns
V_{ESD}	ESD withstand voltage[2,3]	V_{CC1} = V_{CC3} = V_{CC4} = 5V	±8			kV

Note 1: These parameter applies only to the HSYNC and VSYNC channels.

Note 2: Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. V_{CC1}, V_{CC3} and V_{CC4} must be bypassed to GND via a low impedance ground plane with a 0.2uF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SD1, SYNC_OUT2, SD2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard 2kV per the Human Body model (MIL-STD-883, Method 3015).

Note 3: This parameter is guaranteed by design and characterization.

Typical Connection Diagram
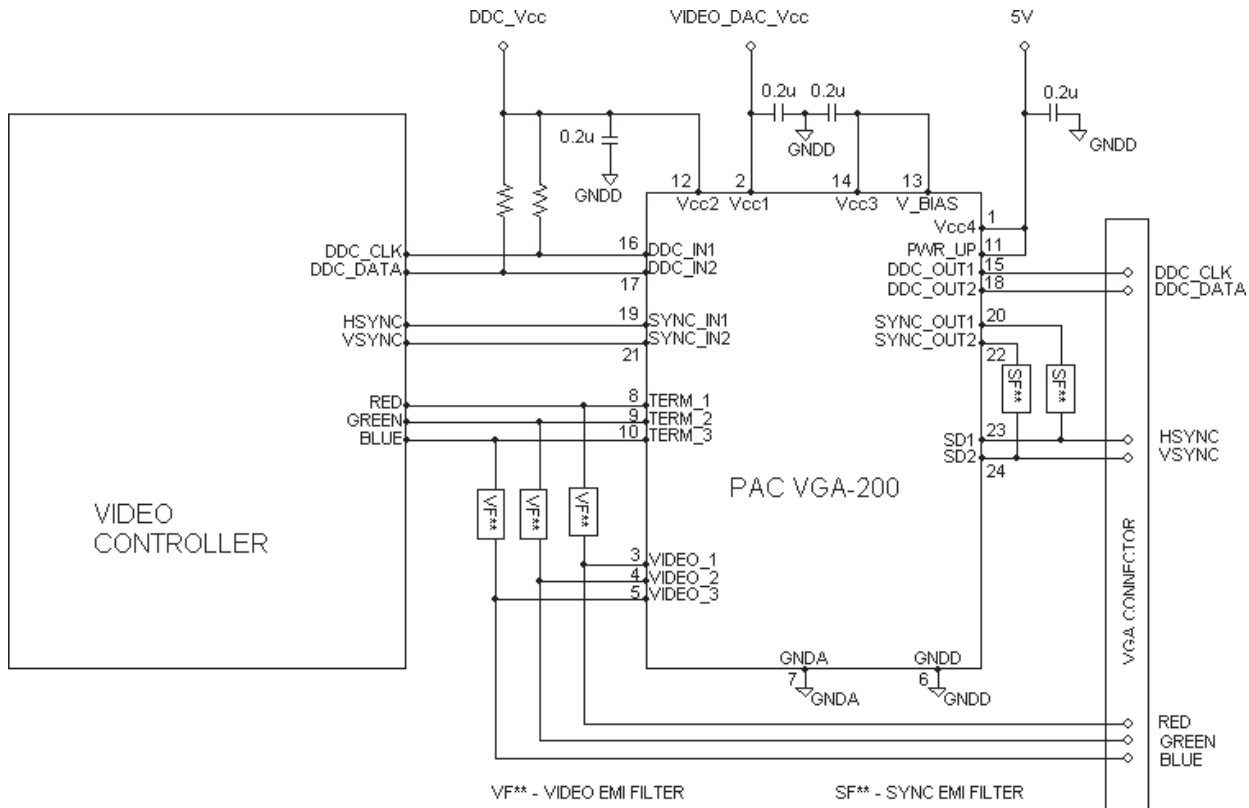
A resistor may be necessary between the V_{CC3} pin and ground if protection against a stream of ESD pulses is required while the PAC VGA200 is in the power-down state. The value of this resistor should be chosen such that the extra charge deposited into the V_{CC3} bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC-61000-4-2 standard is one pulse per second. When the PAC VGA200 is in the power-up state, an internal discharge resistor is connected to ground via an FET switch for this purpose.

For the same reason, V_{CC1} and V_{CC4} may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

GNDA, the reference voltage for the 75R resistors is not connected internally to GNDD and should ideally be connected to the ground of the video DAC IC.

STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Pins	Style	Part Marking
24	QSOP	PACVGA200Q

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