Ordering number: EN 3523A

No.3523A

Video Pack

VPH05

Wideband Video Output Module (Video Pack)

High Defintion Television, Projector Video Output Amplifier

Overview

A single-package product designed specifically for use as the video output stage in ultrahigh-resolution color CRT displays.

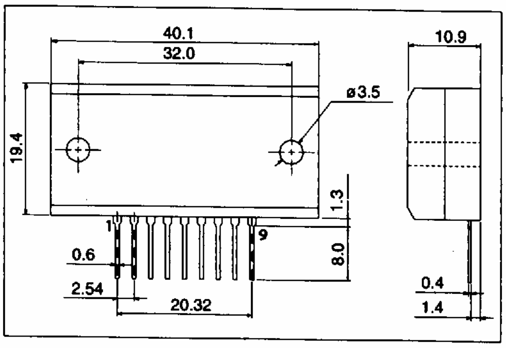
Features

- High output voltage and wide bandwidth; best suited for HDTV.
  [f_C(-3dB)(at V_{OUT}=100$V_{p\text{-}p}$) : 50MHz]
- High performance because of adoption of FBET and LSBT structure transistor chips.

Package Dimensions

unit : mm

2060



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	V_{CC} max		230	V
	V_{BB} max		20	V
Allowable Power Dissipation	P_D max		3.5	W
		Tc=25°C	20	W
Junction Temperature	T_j max		150	°C
Operating Ambient Temperature	T_{opr}		85	°C
Storage Temperature	T_{stg}		-20 ~ +110	°C

Recommended Operating Conditions at Ta=25°C

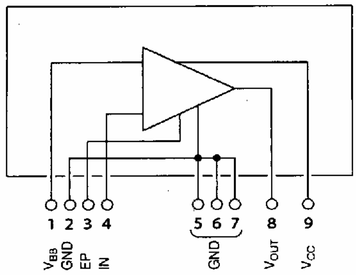
Parameter	Symbol	Conditions	Ratings	Unit
Recommended Supply Voltage	V_{CC} max	V_{OUT} ~ 100$V_{p\text{-}p}$	170	V
	V_{BB} max	V_{IN}(DC)=3.4V	12	V
	V_{CC} max	V_{OUT} ~ 120$V_{p\text{-}p}$	200	V
	V_{BB} max	V_{IN}(DC)=4.0V	12	V

Electrical Characteristics at Ta=25°C

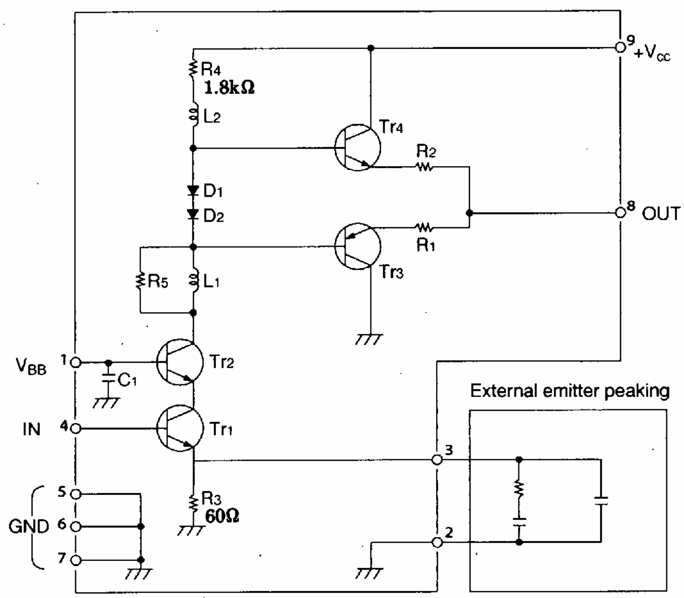
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Band	f_C(-3dB)	V_{OUT}=100$V_{p\text{-}p}$		50		MHz
		V_{OUT}=120$V_{p\text{-}p}$		45		MHz
Voltage Gain	V_G(DC)		26	29	32	times
Suplly Current	$I_{CC}1$	f=10MHz clock, C_L=10pF		60		mA
	$I_{CC}2$	f=50MHz clock, C_L=10pF		100		mA
	$I_{CC}3$	f=10MHz clock, C_L=10pF		76		mA
	$I_{CC}4$	f=30MHz clock, C_L=10pF		96		mA

Note : With optimum peaking

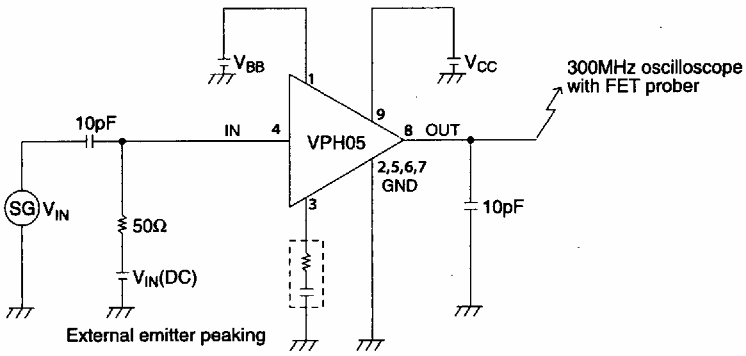
Electrical Connection



Internal Circuit



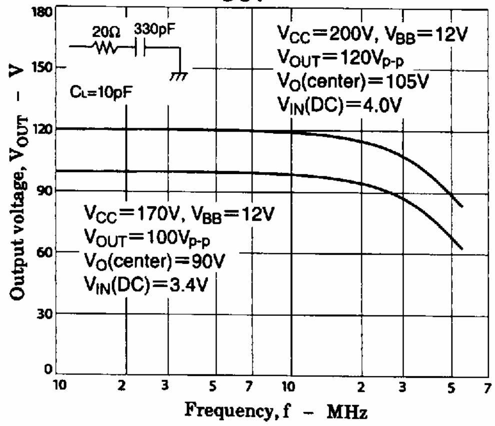
Test Circuit



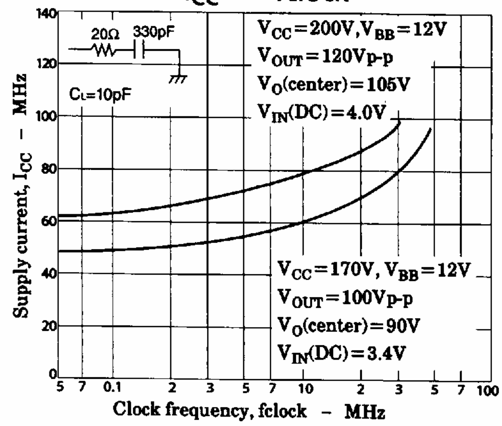
Precautions

1. Pins shoud not be short-circuited while power is applied.
2. See the thermal characteristics in "Heatsink Design" when designing a heatsink.
3. The recommended mounting torque is 39 to 58 N·cm (typical : 49 N·cm)

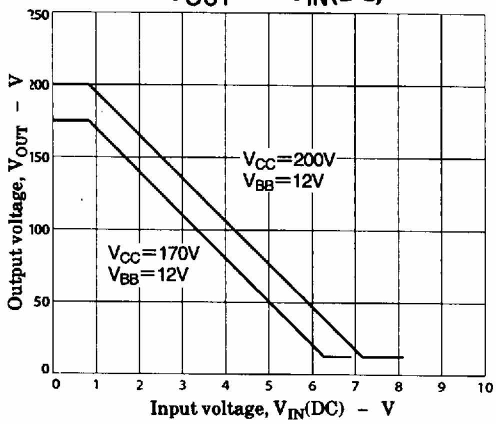
V_{OUT} – f



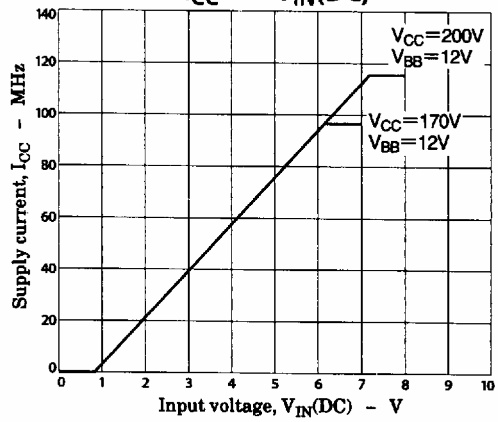
I_{CC} – fclock



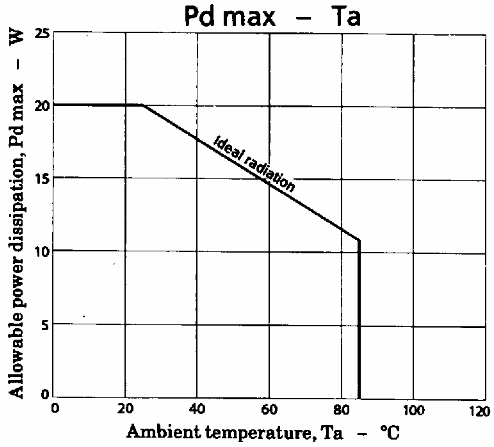
V_{OUT} – V_{IN}(DC)



I_{CC} – V_{IN}(DC)



Pd max – Ta



Heatsink Design

The data and example of heatsink design will be shown as follows.

The transistor junction temperature should be kept below 150°C. To achieve this, a heatsink should be designed to keep the case temperature below 85°C as a standard.

The temperature and the loss of the transistor chips depend on the operating frequency, and their values differ one another. Thermal calculations should be carried out for the largest-loss transistor at the maximum operating frequency of 30MHz (clock). The largest-loss transistor is Tr2 in the internal circuit schematic. It shares about 24% of the total loss shown in the Fig.1. Each transistor's Tj is calculated by next equation.

$$Tj(Tri) = \theta j\text{-}c(Tri) \times P_C(Tri) + \Delta Tc + Ta(°C) \quad \text{......(1)}$$

θ j-c(Tri)	: Junction-to-case thermal resistance of each chip.
P_C(Tri)	: Collector loss of each transistor.
ΔTc	: Case temperature rise.
Ta	: Ambient temperature inside a set.

Each transistor's θ j-c(Tri) is,

$$\theta j\text{-}c(Tr1) = 30°C/W \quad \text{......(2)}$$

$$\theta j\text{-}c(Tr2) \text{ to } (Tr4) = 20°C/W \quad \text{......(3)}$$

From the equations (1) and (2) we get P_C(Tr2) at 30MHz,

$$P_C(Tri)30MHz = P_D(total)30MHz \times 0.24 \quad \text{......(4)}$$

There is a relation shown below between θ h(thermal resistance of a heatsink) and ΔTc,

$$\Delta Tc = P_D(total) \times \theta h \quad \text{......(5)}$$

You can calculate required θ h by the equations (1) and (5).

Heatsink design example

Application conditions : f_H=32kHz (HDTV), f(video)=30MHz(clock)
V_{CC}=170V, V_{BB}=12V, V_{OUT}=100$V_{p\text{-}p}$, (C_1=10pF)
$Ta \leqq 60°C$

When a monitor is operated at the maximum frequency of 30MHz, the recommended θ h is,

$$\theta h = 1.8°C/W$$

If it is possible to keep Ta less than 40°C, θ h would be shrunk into,

$$\theta h = 3.3°C/W$$

(How to calculate θ h)

As mentioned above, the largest-loss transistor is Tr2, and the value is obtained from Figs. 1 and 2 and the equation (4) ;

$$P_C(Tr2) = 13.6 \times 0.24 = 3.26W \quad \text{......(6)}$$

Substituiting the value of the equation (6) in the equation (1) and defining Tj<150°C, ΔTc is,

$$150 > T_j = 20 \times 3.26 + \Delta Tc + 60$$

$$\therefore \Delta Tc < 25(°C)$$

Thus the case temperature rise, ΔTc, should be less than 25°C. To achieve this, θ h of the heatsink is obtained from the equation (5),

$$\theta h < \Delta Tc \div P_D(total) = 25 \div 13.6 \fallingdotseq 1.8$$

$$\therefore \theta h = 1.8°C/W$$

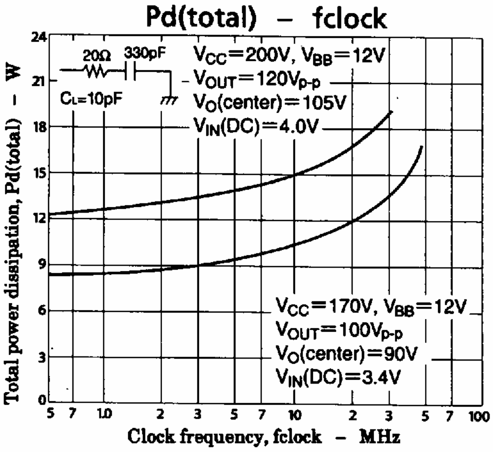

Pd(total) – fclock
20Ω 330pF
CL=10pF
VCC=200V, VBB=12V
VOUT=120Vp-p
VO(center)=105V
VIN(DC)=4.0V
VCC=170V, VBB=12V
VOUT=100Vp-p
VO(center)=90V
VIN(DC)=3.4V
Total power dissipation, Pd(total) – W
Clock frequency, fclock – MHz

Fig.1

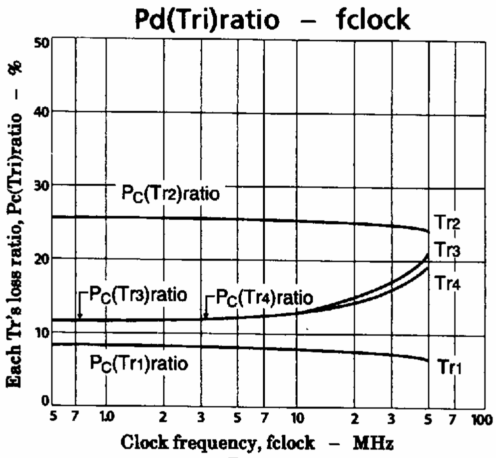

Pd(Tri)ratio – fclock
PC(Tr2)ratio
PC(Tr3)ratio
PC(Tr4)ratio
PC(Tr1)ratio
Tr2
Tr3
Tr4
Tr1
Each Tr's loss ratio, Pc(Tri)ratio – %
Clock frequency, fclock – MHz

Fig.2