Features

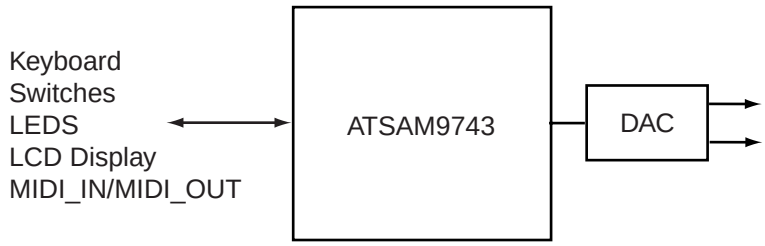
- **Integrates a 64-slot Digital Signal Processor (DSP), 16-bit Processor, 24K x 16 On-chip Flash Memory, 2K x 16 RAM, 64 Individually Programmable I/O Pins**
- **Alternate Group Selectable I/O Pins Allow External Memory Expansion, Host Parallel I/O, Serial MIDI_IN/MIDI_OUT, Additional Digital Audio-in/out**
- **Up to 64 Voices Polyphony, 24 dB Resonant Filter Per Voice, User Programmable Synthesis/Processing Algorithms**
- **Three Timers, One Timer Being Available for Orchestrations Tempo Control**
- **Ideal for Battery Operation**
- **3V to 4.5V Power Supply**
- **Power-down Mode**
- **Parameters Can Be Saved Into Built-in Flash Memory on a Single Word Write Basis.**
- **Compatible with ATSAM97xx Series Design Tools and Debugger**
- **Quick Time to Market**
- **Proven Reliable Synthesis Drivers**
- **In-circuit Emulation with Code View Debugger for Easy Prototype Development**
- **Built-in Flash Programming Algorithm**
- **Low frequency Input Clock at 256xFs Minimizes RFI, Built-in PLL Raises Frequency Internally**
- **PQFP100 Easy Mount Standard Package (Pitch 0.65 mm)**
- **Atmel Standard Flash Technology**

Description

The ATSAM9743 integrates into a single chip an ATSAM97xx core (64-slot DSP + 16-bit processor), a 24K x 16 Flash memory, a 2K x 16 RAM, and up to 64 individually programmable I/O pins. With the addition of a single external digital-to-analog converter or a codec, the ATSAM9743 can be used in a variety of musical and sound processing applications, like low-cost keyboards, equalizers and effect processors.

I/O pins can be configured for external memory expansion, allowing more sophisticated products with up to 4M bytes RAM or ROM.

Figure 1. Typical Application of the ATSAM9743



Sound Synthesis

ATSAM9743 Single-chip Music System

Rev. 1773B-DRMSD–11/02

Principal Elements

Key Circuitry in a Single Chip

The ATSAM9743 provides a new generation of integrated solutions for electronic musical instruments and sound processors. The ATSAM9743 places all key circuitry onto a single silicon chip: sound synthesizer/processor, 16-bit control processor, 24K x 16 Flash memory, 2K x 16 RAM, and up to 64 individually programmable I/O pins allowing direct interface with keyboard, switches, LCD display, etc.

ATSAM97xx Series Processing Core

The synthesis/sound processing core of the ATSAM9743 is taken from the ATSAM97xx series, whose quality has already been demonstrated through dozens of different musical products such as electric pianos, home keyboards, professional keyboards, classical organs, sound expanders and effect devices. The maximum polyphony is 64 voices without effects. A typical application will be 38-voice polyphony with reverb, chorus, 4-band equalizer and surround.

External Memory Expansion

Configuration options allow the ATSAM9743 to cover a wide range of products, from the lowest cost keyboard to the high range multi-effect processor. Thanks to flexible external memory expansion, up to 4M bytes additional external memory can be used for firmware, orchestrations, PCM data or delay lines. The external memory can be ROM, RAM or Flash. The internal Flash memory can be programmed on-board from the ATSAM9743 itself by a Flash programming algorithm, which resides in internal ROM on chip.

Standard Compliance Made Easier

The ATSAM9743 operates from a single 8 MHz crystal. A built-in PLL multiplies by 4 the crystal frequency for internal processing. This minimizes radio frequency interference (RFI), making it easier to comply with FCC, CSA and CE standards.

Battery Powered Usage

The ATSAM9743 is very suitable for battery-operated products:

- A power-down feature is included which can be controlled externally (PDWN/ pin).
- Built-in Flash memory words can be individually programmed by the firmware itself.
- Operational voltage is from 3V to 5.5V (I/O).

Quick Time to Market

The ATSAM9743 has been designed with final instrument quick time-to-market in mind. The ATSAM9743 product development program includes key features to minimize product development efforts:

- Specialized debug interface, providing on-target software development with a source code CodeView debugger.
- Standard sound generation/processing firmware.
- Windows® tools for sounds, soundbanks and orchestration developments.
- Standard soundbanks.
- Comprehensive technical support available directly from Atmel.

Internal Architecture

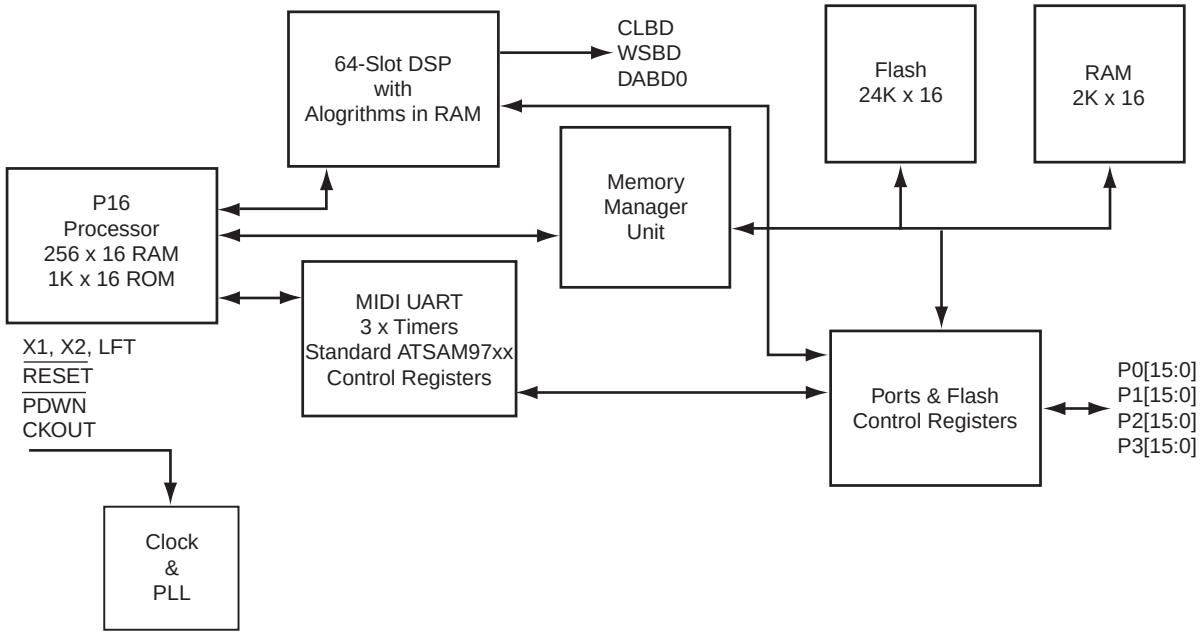
The highly-integrated architecture of the ATSAM9743 combines a specialized high-performance RISC-based digital signal processor (DSP) and a general-purpose 16-bit CISC-based control processor (P16). An on-chip memory management unit (MMU) allows the DSP and the control processor to share an internal 24K x 16 Flash memory, 2K x 16 RAM, as well as optional external ROM and/or RAM memory devices configured through the Ports & Flash control registers.

An intelligent peripheral I/O interface function handles other I/O interfaces, such as the on-chip MIDI UART and three timers, with minimum intervention from the control processor.

Four 16-bit I/O ports can have their bits individually configured as inputs or outputs, they can also be assigned alternate functions such as external memory access (address, data and control signals), 8-bit parallel MIDI port, serial MIDI_IN/MIDI_OUT, and additional digital audio-in/out.

See Table 2 on page 5 and Table 3 on page 6 for details.

Figure 2. Diagram of the Internal Architecture of the ATSAM9743



DSP Engine

The DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 microinstructions known as “algorithms”. Up to 32 DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications.

The DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical musical instrument application will use a little more than half the capacity of the DSP engine for synthesis, thus providing state-of-the-art 38-voice synthesis polyphony. The remaining processing power may be used for typical functions like reverberation, chorus, surround effect, equalizer, etc.

Frequently accessed DSP parameter data are stored in five banks of on-chip RAM memory. Sample data, which is accessed relatively infrequently, can be stored in the built-in Flash

memory, or in external ROM. The combination of localized micro-program memory and localized parameter data allows microinstructions to execute in 31 ns (32 MIPS). Separate buses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each microinstruction. With this architecture, a single microinstruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 192 million operations per second (MOPS).

P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core, which runs from external memory. A debug ROM is included on-chip for easy development of firmware directly on the target system. This ROM also contains the necessary code to directly program the built-in Flash memory. The P16 includes 256 words of local RAM data memory for use as registers, scratchpad data and stack.

The P16 control processor writes to the parameter RAM blocks within the DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART and then controls the DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the Ports & Flash control registers through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows Flash and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows the single built-in Flash memory to serve as sample memory storage for the DSP and as program storage for the P16 control processor. An internal 2K x 16 RAM is also connected to the MMU, allowing RAM resources to be shared between the DSP and the P16. Similarly, when using external memory, corresponding memory resources can be shared between the DSP and the P16.

Pin Description

Pins by Function

Table 1. Power Supply

Pin Name	Pin Number	Type	Function
GND	5, 10, 18, 22, 33, 45, 47, 59, 62, 75, 88, 99	PWR	Digital Ground: All pins should be connected to a ground plane
VC3	3, 11, 21, 27, 61	PWR	Core Power Supply, 3V to 3.8V: All pins should be connected
VCC	17, 31, 46, 57, 73, 87, 100	PWR	I/O Power Supply, 3V to 5.5V: All pins should be connected to a VCC plane

Note: Power supply decoupling: Like all high speed HCMOS ICs, proper decoupling is mandatory for reliable operation and RFI reduction. The recommended decoupling is 100 nF at each corner of the IC with an additional 10 µFT bulk capacitor close to the X1, X2 pins.

Table 2. Single Function Pins

Pin Name	Pin Number	Type	Function
CLBD	26	OUT	External DAC serial bit clock
WSBD	37	OUT	External DAC left/right clock
DABD0	35	OUT	External DAC serial stereo audio data
P3.12 - P3.14	81, 23, 24	Programmable	General purpose I/O
X1	13	IN	Crystal connection, or external clock input at 256*Fs, Fs being the sampling frequency. When used as an input, a 330 ohms serial resistor should be inserted. Typical crystal frequency is 8 MHz (Fs = 32 kHz)
X2	14	OUT	Other end of crystal connection. Cannot be used to drive external circuitry.
CKOUT	95	OUT	Buffered X2 output, can be used to drive external circuits, such as Sigma/Delta DACs
LFT	12	Analog	Built-in PLL compensation filter input
$\overline{\text{RESET}}$	15	IN	Master reset, active low, has built-in Schmitt trigger.
$\overline{\text{PDWN}}$	16	IN	Power down, active low
TEST[2:0]	42 - 44	IN	Test pins. Should be grounded for normal operation. TEST0 is used to start the built-in debugger. In this case TEST2 specifies the communication baud rate.

Note: Pin names exhibiting an overbar ($\overline{\text{PDWN}}$ for example) indicate that the signal is active low.

Table 3. Double Function Pins

Name #1	Name #2	Pin Number	Function
P0.0 - P0.15	WA[15:0]	48, 51, 52, 55, 56, 58, 60, 63 - 65, 67 - 72	#1 – General-purpose I/O #2 – External expansion memory address (output)
P1.0 - P1.15	WD[15:0]	83 - 86, 89 - 92, 96 - 98, 1, 2, 6, 8, 9	#1 – General-purpose I/O #2 – External expansion memory data (I/O)
P2.0	$\overline{\text{WCS0}}$	39	#1 – General Purpose I/O #2 – Expansion ROM chip select (output, active low)
P2.1	$\overline{\text{WCS1}}$	40	#1 – General-purpose I/O #2 – Expansion RAM chip select (output, active low)
P2.2	$\overline{\text{WOE}}$	41	#1 – General-purpose I/O #2 – Expansion memory enable (output, active low)
P2.3	$\overline{\text{WWE}}$	38	#1 – General-purpose I/O #2 – Expansion RAM write enable (output, active low)
P2.4	RBS	29	#1 – General-purpose I/O #2 – Expansion RAM byte select, allows connection of 8-bit external SRAM with 16-bit access in two cycles (output, active low)
P2.5 - P2.9	WA[20:16]	74, 78 - 80, 82	#1 – General-purpose I/O #2 – Expansion memory address, allows up to 2M x 16 external memory (output)
P2.10	$\overline{\text{CS}}$	94	#1 – General-purpose I/O #2 – Host processor chip select (input, active low)
P2.11	$\overline{\text{RD}}$	77	#1 – General-purpose I/O #2 – Host processor read (input, active low)
P2.12	$\overline{\text{WR}}$	76	#1 – General-purpose I/O #2 – Host processor write (input, active low)
P2.13	A0	66	#1 – General-purpose I/O #2 – Host processor data (0) – command/status (1) select (input)
P2.14	DABD1	36	#1 – General-purpose I/O #2 – Secondary DAC serial stereo audio data (output)
P2.15	DAAD0	34	#1 – General-purpose I/O #2 – External ADC serial stereo audio data (input)
P3.0 - P3.7	D[7:0]	25, 28, 30, 32, 49, 50, 53, 54	#1 – General-purpose I/O #2 – Host processor data bus (I/O)
P3.8	IRQ	4	#1 – General-purpose I/O #2 – Host processor interrupt request, active high, tri-state output
P3.9	RUN	20	#1 – General-purpose I/O #2 – High indicates that DSP synthesis is up and running

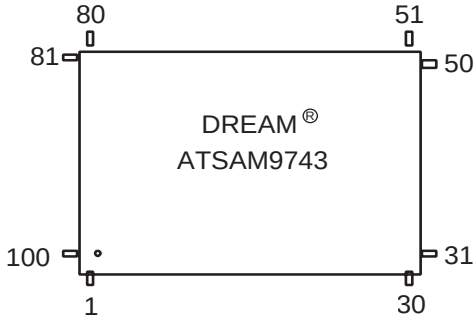
Table 3. Double Function Pins (Continued)

Name #1	Name #2	Pin Number	Function
P3.10	MIDI_IN	19	#1 – General-purpose I/O #2 – Serial MIDI_IN (input)
P3.11	MIDI_OUT	7	#1 – General-purpose I/O #2 – Serial MIDI_OUT (output)
P3.15	DAAD1	93	#1 – General-purpose I/O #2 – Secondary ADC serial stereo audio data (input)

Table 4. Pinout by Pin Number

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	P1.11/WD11	26	CLBD	51	P0.1/WA1	76	P2.12/$\overline{WR}$
2	P1.12/WD12	27	VC3	52	P0.2/WA2	77	P2.11/$\overline{RD}$
3	VC3	28	P3.1/D1	53	P3.6/D6	78	P2.6/WA17
4	P3.8/IRQ	29	P2.4/RBS	54	P3.7/D7	79	P2.7/WA18
5	GND	30	P3.3/D2	55	P0.3/WA3	80	P2.8/WA19
6	P1.13/WD13	31	VCC	56	P0.4/WA4	81	P3.12
7	P3.11/MIDI_OUT	32	P3.3/D3	57	VCC	82	P2.9/WA20
8	P1.14/WD14	33	GND	58	P0.5/WA5	83	P1.0/WD0
9	P1.15/WD15	34	P2.15/DAAD0	59	GND	84	P1.1/WD1
10	GND	35	DABD0	60	P0.6/WA6	85	P1.2/WD2
11	VC3	36	P2.14/DABD1	61	VC3	86	P1.3/WD3
12	LFT	37	WSBD	62	GND	87	VCC
13	X1	38	P2.3/$\overline{WWE}$	63	P0.7/WA7	88	GND
14	X2	39	P2.0/$\overline{WCS0}$	64	P0.8/WA8	89	P1.4/WD4
15	$\overline{RESET}$	40	P2.1/$\overline{WCS1}$	65	P0.9/WA9	90	P1.5/WD5
16	$\overline{PDWN}$	41	P2.2/$\overline{WOE}$	66	P2.13/A0	91	P1.6 /WD6
17	VCC	42	TEST0	67	P0.10/WA10	92	P1.7/WD7
18	GND	43	TEST1	68	P0.11/WA11	93	P3.15/DAAD1
19	P3.10/MIDI_IN	44	TEST2	69	P0.12/WA12	94	P2.10/$\overline{CS}$
20	P3.9/RUN	45	GND	70	P0.13/WA13	95	CKOUT
21	VC3	46	VCC	71	P0.14/WA14	96	P1.8/WD8
22	GND	47	GND	72	P0.15/WA15	97	P1.9/WD9
23	P3.13	48	P0.0/WA0	73	VCC	98	P1.10/WD10
24	P3.14	49	P3.4/D4	74	P2.5/WA16	99	GND
25	P3.0/D0	50	P3.5/D5	75	GND	100	VCC

Figure 3. Package Description: PQFP100, Pitch = 0.65 mm



Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Ambient Temperature (Power Applied) ..... -40°C to + 85°C Storage Temperature.....-65°C to + 150°C Voltage on any pin (except X1).....-0.5V to V_{CC} + 0.5V Voltage on X1 pin.....-0.5V to V_{C3} + 0.5V V_{CC} Supply Voltage.....-0.5V to + 6.5V V_{C3} Supply Voltage.....-0.5V t0 + 4.5V Maximum I_{OL} per I/O pin 4.4mA	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage (I/O)	3	3.3/5.0	5.5	V
V_{C3}	Supply voltage (Core)	3	3.3	3.8	V
t_A	Operating ambient temperature	0		70	°C

DC Characteristics

Table 7. DC Characteristics (T_A = 25°C, V_{CC} = 5V ± 10%, V_{C3} = 3.3V ± 10%)

Symbol	Parameter	V_{CC}	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V
V_{IH}	High-level input voltage	3.3 5.0	2.3 3.3		V_{CC} + 0.5 V_{CC} + 0.5	V
V_{OL}	Low-level output voltage at I_{OL} = -3.2 mA(1)	3.3 5.0			0.45 0.45	V
V_{OH}	High-level output voltage at I_{OH} = 0.8 mA(2)	3.3 5.0	2.8 4.5			V
I_{CC}	Power supply current (crystal frequency = 8 MHz)	3.3 5.0		60 TBD	80 TBD	mA
	Power down supply current			TBD	150	µA

Notes: 1. I_{OL}: Low-level output current.
2. I_{OH}: High-level output current.

Timing Diagrams

All timing conditions: V_{CC} = 5V, V_{C3} = 3.3V, T_A = 25°C, 30 pF load capacitance on all outputs except X2. All timings refer to t_{CK}, which is the internal master clock period.

$t_{CK} = t_{XTAL}/4$ (typ 31.25 ns).

External Memory (16 bits)

Figure 4. External ROM/RAM (16 bits)

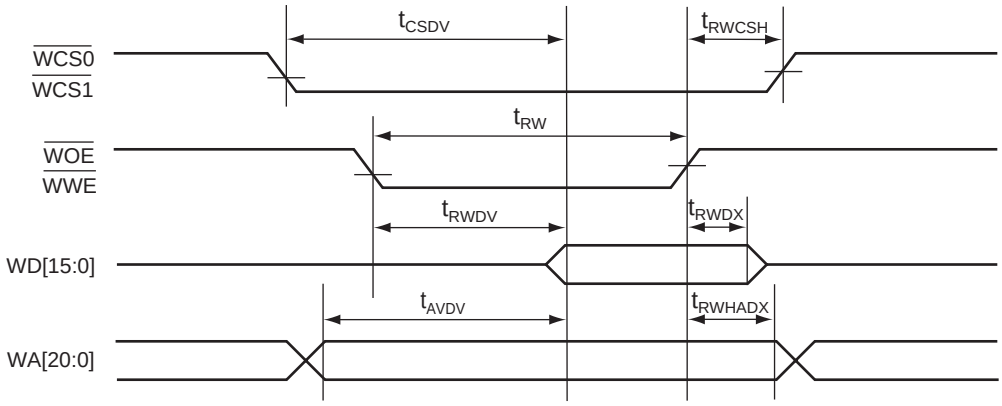
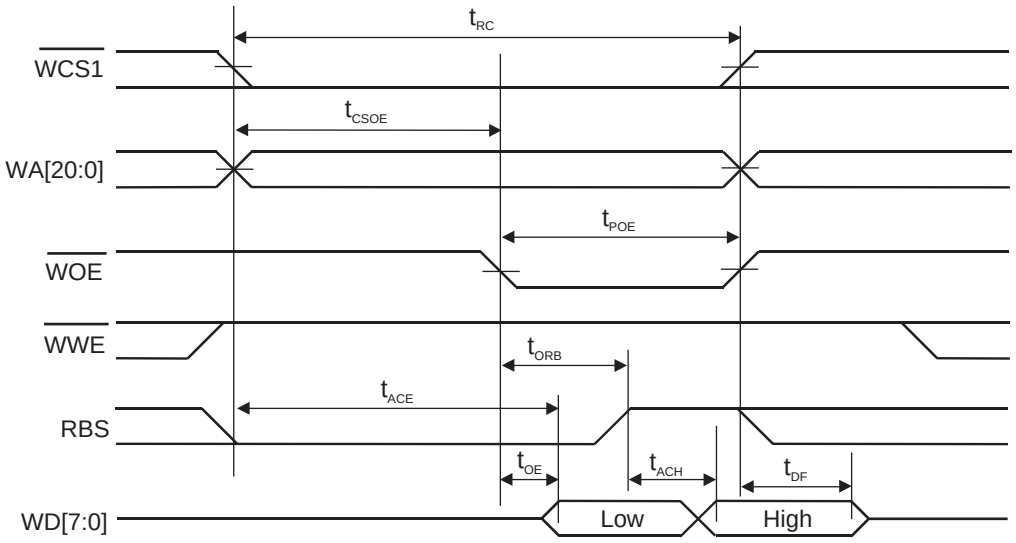


Table 8. Parameters for External Memory Read/Write Cycle (16 bits)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSDV}	Access time from $\overline{WCSx}$ low	5 x t_{CK} - 5			ns
t_{RWDV}	Access time from $\overline{WOE}$, $\overline{WWE}$ low	3 x t_{CK} - 5			ns
t_{AVDV}	Access time from address valid	5 x t_{CK} - 5			ns
t_{RW}	$\overline{WOE}$, $\overline{WWE}$ pulse width		4 x t_{CK}		ns
t_{RWHCSH}	$\overline{WCSx}$ high from rising $\overline{WOE}$ or $\overline{WWE}$	10			ns
t_{RWHADX}	Address valid after rising $\overline{WOE}$ or $\overline{WWE}$	10			ns
t_{RWDX}	Data hold time from rising $\overline{WOE}$ or $\overline{WWE}$	10	6 x t_{CK}		ns

External Ram (8 bits)

Figure 5. 8-bit SRAM Read Cycle



Note: By setting the SRAM 8-bit in the P16 control word, external RAM can be configured to read 16-bit with 2 x 8-bit accesses.

Figure 6. 8-bit SRAM Write Cycle

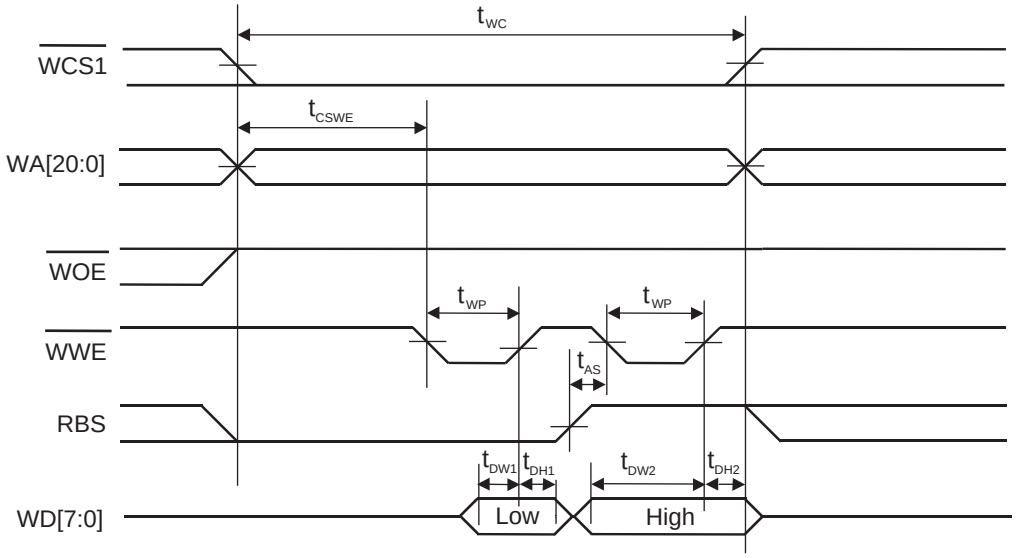


Table 9. Parameters for External 8-bit SRAM Read/Write

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Word (2 x bytes) read cycle time	5 x t_{CK}		6 x t_{CK}	ns
t_{CSOE}	Chip select low. Address valid to $\overline{WOE}$ low	2 x t_{CK} - 5		3 x t_{CK} + 5	ns
t_{POE}	Output enable pulse width		3 x t_{CK}		ns
t_{ACE}	Chip select. Access low byte access time.	3 x t_{CK} - 5			ns
t_{OE}	Output enable low byte access time	t_{CK} - 5			ns
t_{ORB}	Output enable low to byte select high		t_{CK}		ns
t_{ACH}	Byte select high byte access time	2 x t_{CK}- 5			ns
t_{DF}	Chip select or $\overline{WOE}$ high to input data HI-Z	0		2 x t_{CK} - 5	ns
t_{WC}	Write (2 x bytes) write cycle time	5 x t_{CK}		6 x t_{CK}	ns
t_{CSWE}	1st $\overline{WWE}$ low from $\overline{CS}$ or address or $\overline{WOE}$	2 x t_{CK} - 10			ns
t_{WP}	Write (low and high byte) pulse width	1.5 x t_{CK} - 5			ns
t_{DW1}	Data out low byte setup time	1.5 x t_{CK} - 10			ns
t_{DH1}	Data out low byte hold time	0.5 x t_{CK} + 10			ns
t_{AS}	RBS high to second write pulse	0.5 x t_{CK} - 5			ns
t_{DW2}	Data out high byte setup time	2 x t_{CK} - 10			ns
t_{DH2}	Data out high byte hold time	10			ns

Parallel Interface

Figure 7. Host Interface Read Cycle

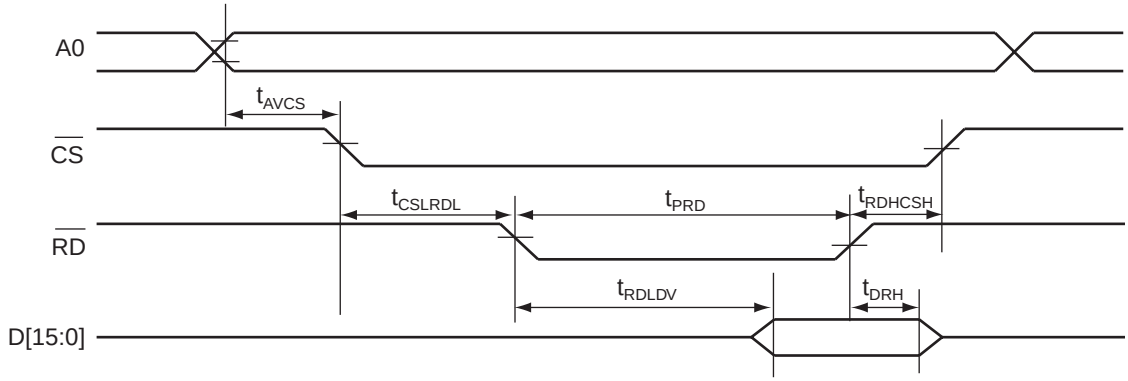


Figure 8. Host Interface Write Cycle

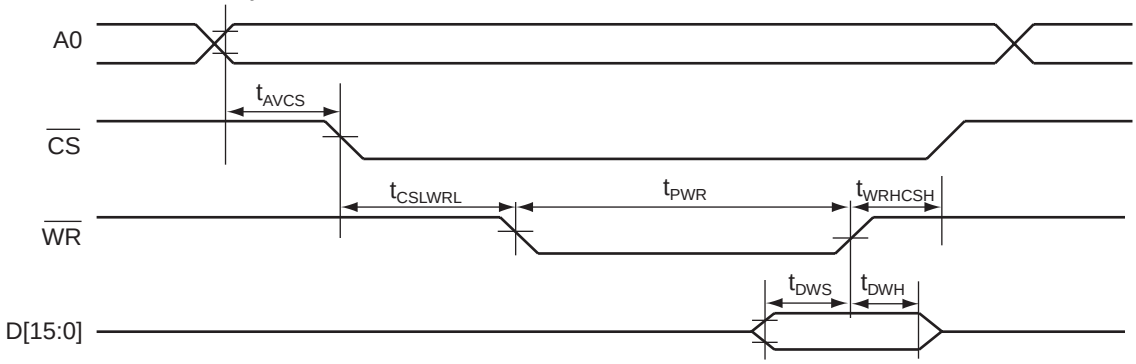


Table 10. Parameters for the Parallel Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0			ns
t_{CSLRDL}	Chip select low to $\overline{RD}$ low	5			ns
t_{RDHCSH}	$\overline{RD}$ high to $\overline{CS}$ high	5			ns
t_{PRD}	$\overline{RD}$ pulse width	50			ns
t_{RDLDV}	Data out valid from $\overline{RD}$			20	ns
t_{DRH}	Data out hold from $\overline{RD}$	5		10	ns
$t_{CSLRWRL}$	Chip select low to $\overline{WR}$ low	5			ns
t_{WRHCSH}	$\overline{WR}$ high to $\overline{CS}$ high	5			ns
t_{PWR}	$\overline{WR}$ pulse width	50			ns
t_{DWS}	Write data setup time	10			ns
t_{DWH}	Write data hold time	0			ns

Digital Audio Timing

Figure 9. Digital Audio Timing Diagram

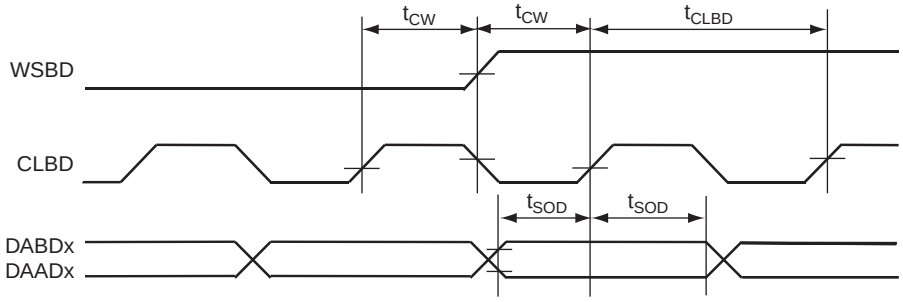


Figure 10. Digital Audio Frame Format

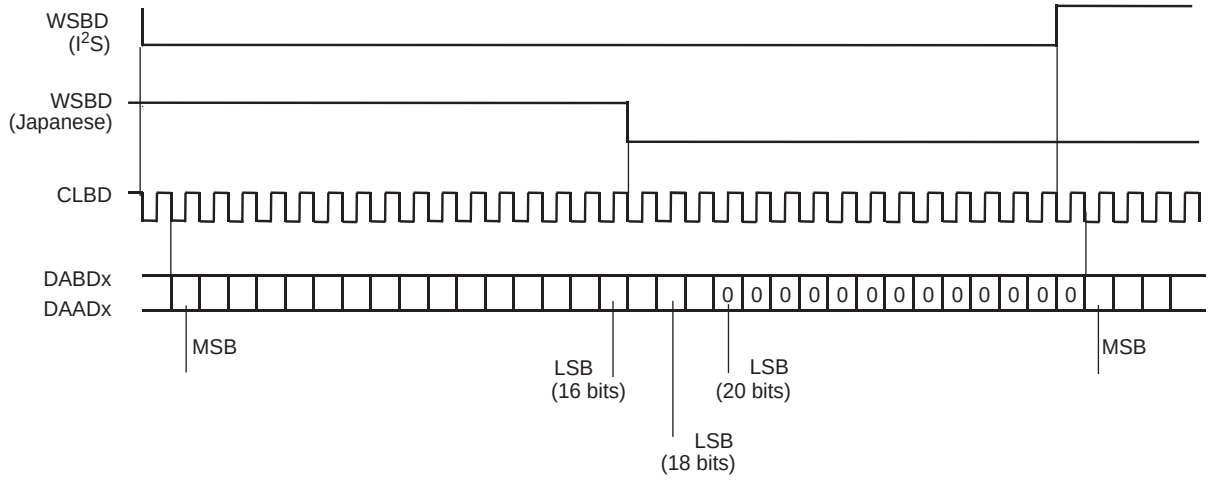


Table 11. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	8 x t_{CK} - 10			ns
t_{SOD}	DABDx/DAADx valid prior/after CLBD rising	8 x t_{CK} - 10			ns
t_{CLBD}	CLBD cycle time		16 x t_{CK}		ns

Overview of Operation

This section limits its contents to a description of the operation and registers specific to the ATSAM9743. A familiar understanding of the ATSAM97xx series operation is required.

Normal Operation Mode

TEST2 = TEST1 = TEST0 = O:

In this mode, the built-in Flash is assumed to be already programmed. After $\overline{\text{RESET}}$, all pins are in configuration #1 and all general purpose I/Os (64 pins) are in input mode with a weak pull-down resistor.

The P16 program starts at address 8000H, which is the first word of the internal Flash.

The program coded in Flash or into external memory has access to nine specific 16-bit registers as follows.

I/O Configuration Register Address 20:0808H (Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	MIDI_ OUT	MIDI_ IN	RUN	DAAD0	DABD1	IRQ	HOST	AD20	AD19	AD18	AD17	AD16	ROM	RAM

This register is cleared at reset. A one written to the register indicates that the corresponding alternate configuration #2 is selected as follows:

- RAM: WA[15:0], WD[7:0], $\overline{\text{WCS1}}$, $\overline{\text{WOE}}$, $\overline{\text{WWE}}$, RBS
- ROM: $\overline{\text{WCS0}}$, WD[15:8]
- AD[20:16], Respective WA[20:16] signals
- HOST: $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0, D[7:0]
- IRQ: IRQ
- DABD1, DABD0, RUN, MIDI_IN, MIDI_OUT: Corresponding pins

I/O Direction Registers Address 20:0804H to 20:0807H (Read/Write)

These four registers (one for each General-purpose I/O port P0 to P3) are cleared at reset, thus putting all port bits in input mode.

A one in a given bit position configures the corresponding port bit in output mode (assuming that no alternate function is selected for the port bit).

I/O Data Write Registers Address 20:0800H to 20:803H (Read/Write)

These four registers (one for each General Purpose I/O port P0 to P3) are cleared at power-up. A 0/1 written in a given bit position sets the corresponding port bit to 0/1, assuming that no alternate function is selected for the port bit and that the port bit is in output mode.

A read from the register always returns the value written to the register independently of the actual port configuration.

I/O Data Reads Registers Address 20:810H to 20:0813H (Read-only)

A read from these registers always returns the value of the pins independently of the configuration. For example, suppose that P3.10 is configured as MIDI_IN, then setting the direction to output and writing data to P3.10 will have no effect. However, the actual value of the MIDI_IN pin would be read.

On Board Flash Program/Debug Mode

TEST1 = 0, TEST0 = 1:

In this mode, the P16 program starts in the built-in debug ROM. All ports are set to input mode with a weak pull-down, except P3.10 and P3.11 which are set to MIDI_IN and MIDI_OUT, respectively.

If TEST2 = 0, the baud rate is set to the MIDI standard (31250 baud). If TEST2 = 1 the baud rate is set to 57600 baud. This later setting is useful when Flash programming time is a production cost issue.

Programming the built-in Flash, or debugging a P16 program, occurs exclusively through the MIDI_IN and MIDI_OUT pins, which means that any firmware can be debugged except the MIDI part of the firmware (note that as the ATSAM9743 is compatible with the ATSAM97xx series, it is easy to debug the MIDI with another development board such as 97PNP2).

MIDI_IN Commands

The following is only given for information purposes, as the CV9743 CodeView debugger takes care of all the protocol handling between a PC and the ATSAM9743 target board.

Commands are received through MIDI_IN, all commands except GO and GR are acknowledged. A new command should not be sent until the acknowledge from a previous command is received.

Note that the commands are compatible with the standard Debug program from the ATSAM97xx series.

The first command sent to the ATSAM9743 after reset should be INIT (0F0H).

Table 12. Parameters for MIDI_IN/MIDI_OUT Commands and Answers

MIDI_IN Command	Byte Parameters	MIDI_OUT Answer	Description
INIT 0F0H	–	Ack (0ACH)	Establish link. This should be the first command sent after reset.
RDIRAM 00H	ad	dl, dh	Read P16 IRAM at ad
WRIRAM 01H	ad, dl, dh	Ack (0ACH)	Write dh/dl at P16 IRAM address ad
RDXTMEM 02H	adl, adh, pl, ph	dl, dh	Read word of P16 external memory at address ph/pl:adh/adl. Note that from a P16 point of view, the built-in Flash and 2K x 16 SRAM are external memory.
WRXTMEM 03H	adl, adh, pl, ph, dl, dh	Ack (0ACH)	Write dh/dl word of data to P16 external memory at address ph/pl:adh/adl. If the address falls into the Flash range, then Flash-programming algorithm is applied. Ack is returned after the write is completed.
RDIO 04H	ioad	dl, dh	Read P16 I/O at ioad
WRIO 05H	ioad, dl, dh	Ack (0ACH)	Write dh/dl at I/O address ioad
RDSAML 06H	samadl, samadh	dl, dh	Read low word of synthesis DSP RAM at samadh/samadl
RDSAMH 07H	samadl, samadh	dl, dh	Read high word of synthesis DSP RAM at samadh/samadl
WRSAM 08H	samadl, samadh, d0, d1, d2, d3	Ack (0ACH)	Write 32 bits (d3/d2/d1/d0) of data to Synthesis DSP RAM at address samadh/samadl
GO 09H	adl, adh	See note	Jump to adh/adl (start firmware)
GR 0AH	Dummy	See note	Restore firmware context
RDBLOCK 0BH	adl, adh, pl, ph, sizel, sizeh	2*size bytes	Read size words of external memory starting at address ph/pl/adh/adl

Table 12. Parameters for MIDI_IN/MIDI_OUT Commands and Answers (Continued)

WRBLOCK 0CH	adl, adh, pl, ph, sizel, sizeh, 2*size data bytes	Ack (0ACH)	Write size words to external memory starting at address ph/pl:adh/adl. This will NOT work if the address is in the Flash range. Use WRFLASH command for block programming of the built-in Flash.
WRFLASH 0DH	adl, adh, size, 2*size bytes	Ack (0ACH)	Write size words (max 32) to Flash, starting at address 8000H + adh/adl. The block written shall not cross a 32 words Flash page. Before actually writing to the Flash, Ack is returned immediately after the last data byte is received, thereby allowing masked time Flash programming.
CHKFLASH 0EH	Dummy	Ack (0ACH)	Ack is returned when the current Flash write has been completed, thus allowing monitoring of the completion of the last WRFLASH.

Breakpoint Settings

Breakpoint is set by replacing a firmware instruction by the single word ROM Debug instruction. This instruction jumps into the ROM debug code, saves the caller program context and sends data AAH, 55H to MIDI_OUT. This signals the 9743CV program that a breakpoint has been reached. Further program execution will be done by restoring the instruction at the breakpoint address, modifying the context stack (IP = IP-1) and issuing a GR command. The GR command restores the user program context and resumes execution at the restored instruction.

Debugger Requirements

The debugger needs the following resources to operate:

- One word at address 18H in IRAM
- 18 words of stack
- 8 words starting at address 20:0000H in built-in SRAM for FIFO

An additional 32 words of SRAM (20:0008H to 20:0027H) are needed for block Flash programming (WRFLASH).

Specific Flash functions such as chip erase, signature fuse, etc. can be externally triggered by using combinations of the above commands.

Flash Program and Test Registers

Three additional write I/O registers and two read I/O registers are implemented for the built-in Flash program and test, as follows.

FADDTEST Register Address 0020:080AH (Read/Write)

This 15-bit register provides the addtest<14:0> address bus to the Flash block. This is the address register when programming the Flash.

FDI Register Address 0020:080BH (Read/Write)

This 16-bit register provides the di<15:0> data bus to the Flash block. This is the data register when programming the Flash.

FCOMMAND Register Address 0020:0809H (Cleared at $\overline{\text{RESET}}$ time) (Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					RSTT	CEN	WE	PAGEM	PAGE1	TM5	TM4	TM3	TM2	TM1	TM0

- RSTT,CEN, WE, PAGEM, PAGE1,TM5–TM0: Signals sent to corresponding Flash block inputs. These signals, with proper timing, provide Flash programming.

FSTATUS Register Address 0020:0809H (Read-only)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	TEST2	TEST1	TEST0	X	X	X	X	X	X	DOUTEN	RDYBSYN

- RDYBSYN and DOUTEN: These Flash signals provide write-progress monitoring respectively.
- TEST0–TEST2: Input pins, respectively.

FDOTEST Register (Read-only)

Reads the dotest <15:0> Flash data output bus for test modes.

Memory Map

Table 13. Description of the ATSAM9743 Memory Map

Address Low	Address High	Access
0000:0000	0000:00FF	ATSAM97xx Standard Routine ROM
0000:0100	0000:03FF	Built-in ROM for Flash program & debug routines
0000:400	0000:7FFF	Optional external ROM
0000:8000	0000:DFFF	Built-in Flash (24K x 16)
0000:E000	001F:FFFF	Optional external ROM ($\overline{WCS0}$)
0020:0000	0020:07FF	Built-in SRAM (2K x 16)
0020:0800	0020:0815	ATSAM9743 specific I/Os
0020:0816	01FF:FFFF	Not used
0200:0000	021F:FFFF	Optional external RAM ($\overline{WCS1}$)

Note: If programmed as an alternate function, $\overline{WCSO}$ is generated even if the firmware accesses the built-in Flash or ROM. In this case the external ROM data is not used.

Flash Programing Performance

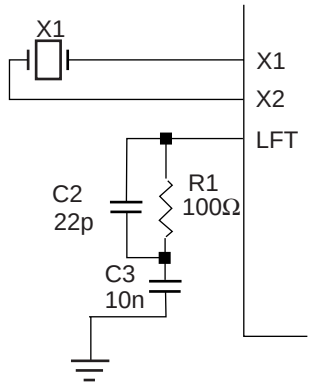
Typical programming times for the 24K x 16 Flash are as follows:

MIDI baud rate 31250 bauds, TEST0 = 1, TEST2 = 0: 33 seconds

57600 bauds, TEST0 = 1, TEST2 = 1: 19 seconds

Crystal Compensation/ LFT FIlter

Figure 11. Recommended Crystal Compensation and LFT Filter



Note: The ATSAM9743 uses a low power oscillator. No compensation capacitor is necessary. However, because the crystal drive is very small, it is mandatory to keep the X1/X2 traces as small as possible.

Mechanical Dimensions

Figure 12. ATSAM9743 Mechanical Dimensions

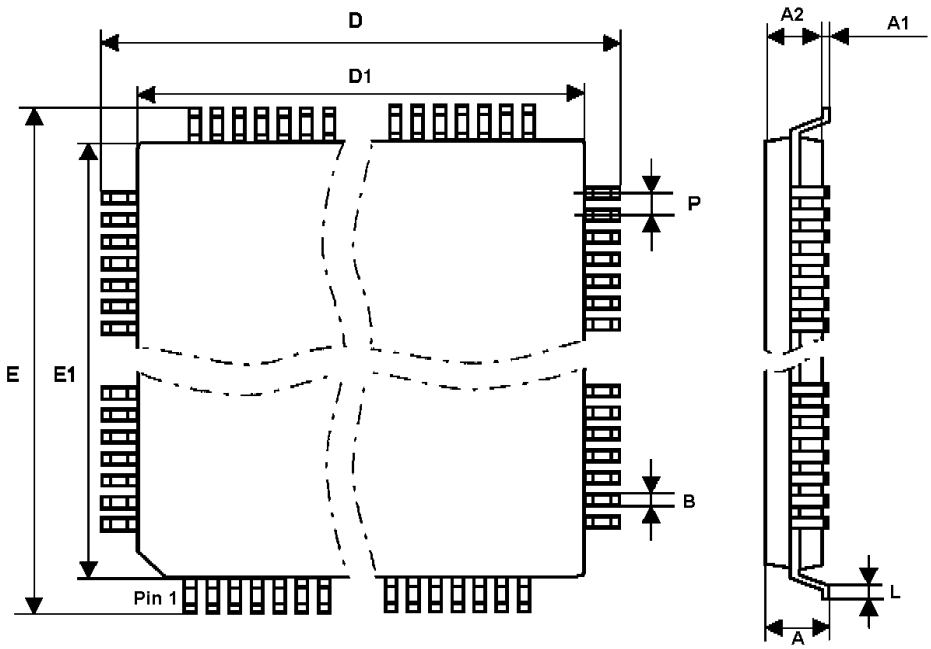


Table 14. ATSAM9743 Plastic Lead Quad Flat Pack (PQFP100)

	Min	Nom	Max
A			3.4
A1	0.25		
A2	2.55	2.8	3.05
D		17.9	
D1		14.0	
E		23.9	
E1		20	
L	0.65	0.88	1.03
P		0.65	
B	0.22		0.38

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

1773B–DRMSD–11/02 0M