

## ●Product Outline

■Type	BU7879KVT
■Function	30bit(+5bit) LVDS Receiver for Flat Panel Display
■Package	TQFP64V
■Supply voltage	3.3V±0.3V
■Temperature range	-20°C~85°C
■Frequency range	8~90MHz

## ●Feature

- Five channels of LVDS data stream are converted to 35bits data of parallel LVCMOS level outputs.
- 30bits of RGB output data, 5bits of timing and control output data(HSYNC, VSYNC, DE, CTL1 and CTL2) are available.
- Support clock frequency from 8MHz up to 90MHz.
- Support consumer video format including 480i, 480P, 720P and 1080i as well..
- Support many kinds of PC video formats such as VGA, SVGA, XGA and WXGA.
- Provide 630Mbps per 1ch or 3.15Gbps per device throughput rate using 90MHz clock rate.
- User programmable LVCMOS data output triggering timing by using either rising or falling edge of clock..
- 30bit LVDS transmitter is recommended to use BU7878KVT.

## ●Precaution

- The contents of this specifications might be changed without a previous notice.
- Please be careful of handling the contents of this specifications document because use of Foreign Exchange and Foreign Trade Control Law(technology in use of design, manufacture and use) have the possibility of violating the law.
- This chip is not designed to protected from radioactivity.

●Block Diagram

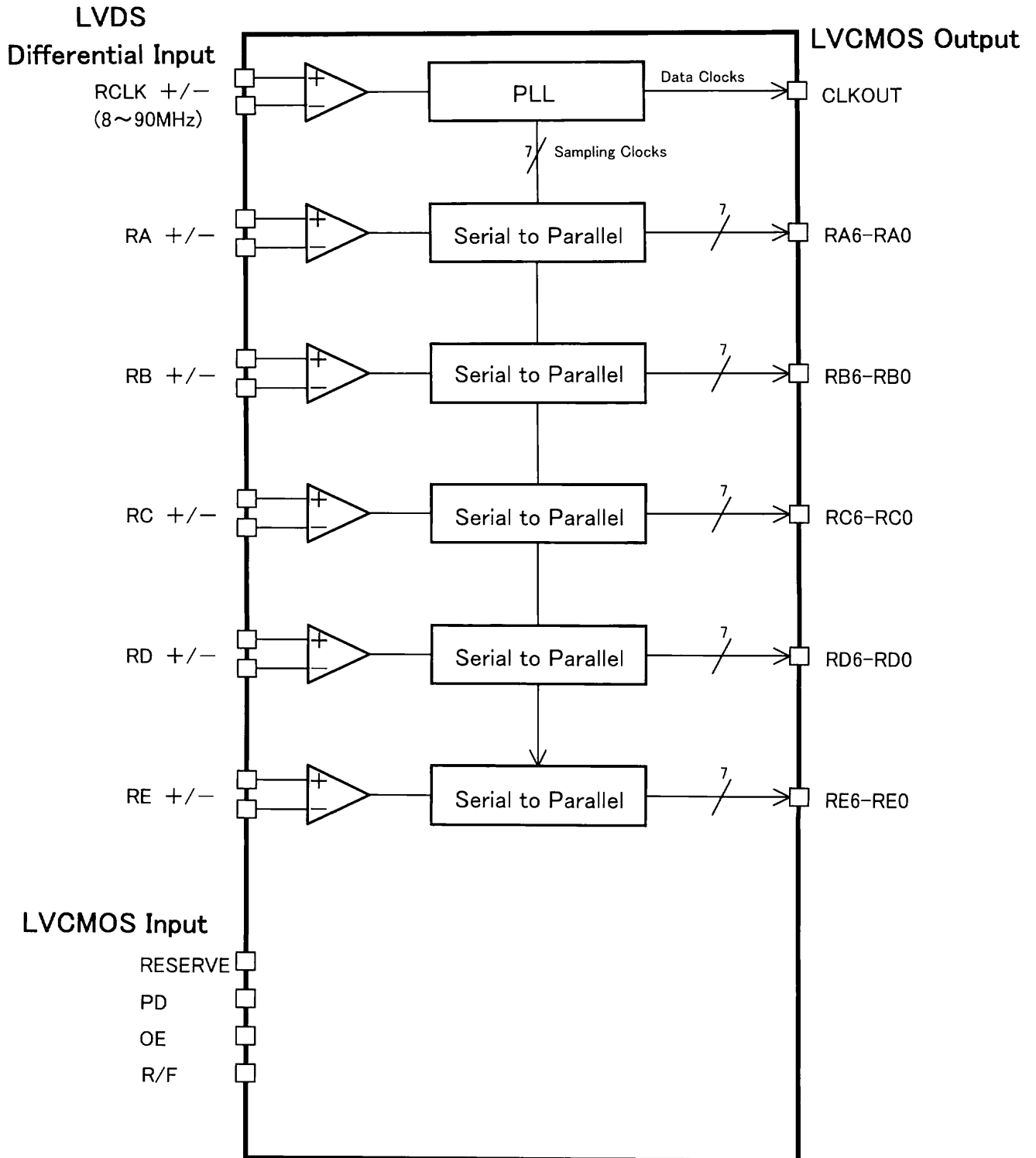


Figure-1 Block Diagram

● About the Power On Reset

Power on reset is not mandatory for this device.

(The PD pin should be set to high level when power on reset procedure is not used.)

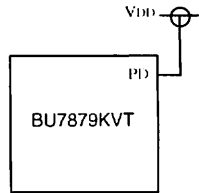
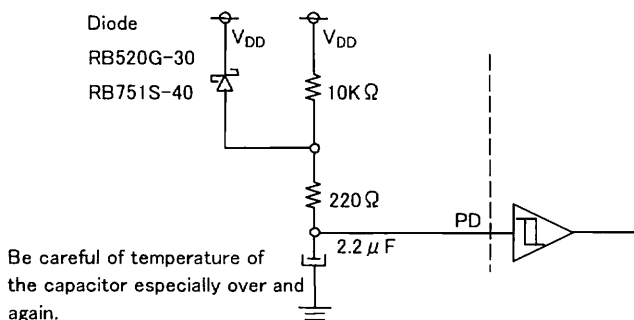


Figure-10 Terminal connection when power on reset is not used.

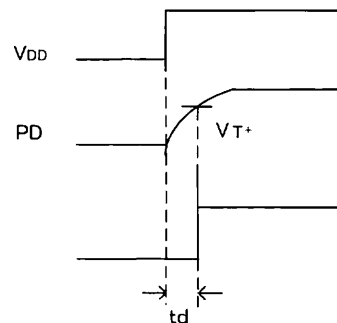
However, Power on reset procedure is strongly recommend for internal logic initialization by following two methods.

- ① The method of using CR circuit.
- ② The method of using external specific IC.

It is recommend to do enough examination for target application.

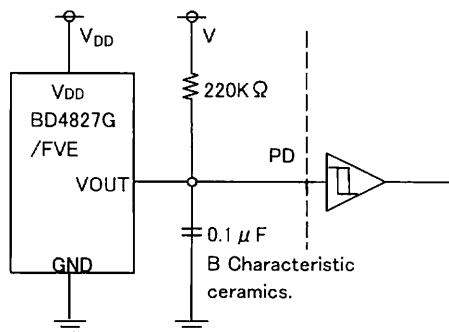


Be careful of temperature of the capacitor especially over and again.  
B characteristic ceramics and function polymer aluminum electrolysis are recommended.



td is approximately equal to 20ms when the left RC coeulus are applied.

Figure-11 Power on reset by external a CR circuit



Detection voltage is 2.7V when BD5327G is used.  
More detailed specification is available in dedicated device data sheet.

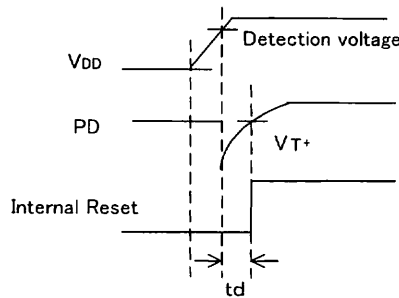


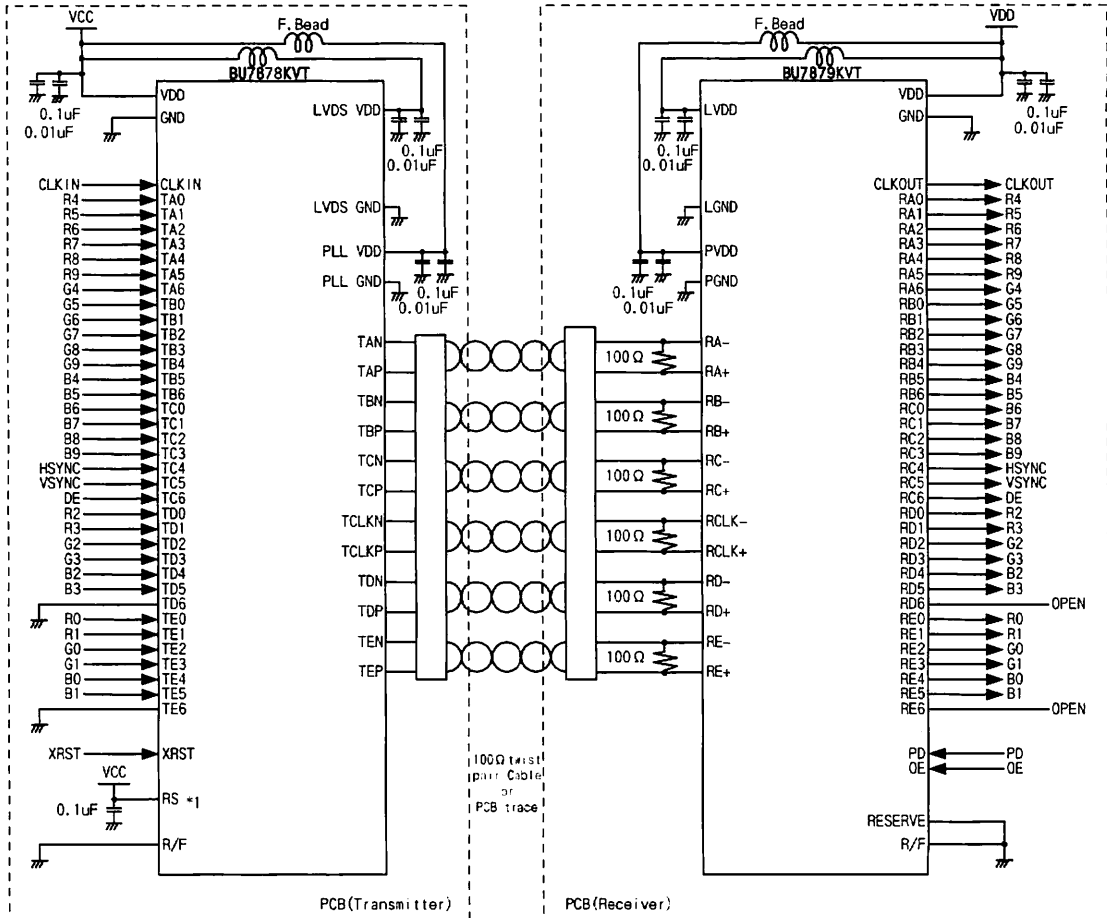
Figure-12 Power on reset by specific IC

● 10 LVDS Level Input & Output

Example:

BU7878KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output

BU7879KVT : LVCMOS level output/Falling edge



\* 1 :If RS pin is tied to VCC,LVDS swing is 350m V.  
If RS pin is tied to GND,LVDS swing is 200m V.

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