

## **700MHz Slew-Enhanced VFAs**

The EL5104, EL5105, EL5204, EL5205, and EL5304 represent high speed voltage feedback amplifiers based on the current feedback amplifier architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. This family is available in single, dual, and triple versions, with 200MHz, 400MHz, and 700MHz versions. This family operates on single 5V or  $\pm 5V$  supplies from minimum supply current. The EL5104 and EL5204 also feature an output enable function, which can be used to put the output in to a high-impedance mode. This enables the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

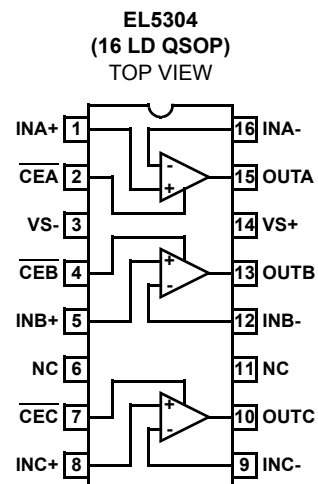
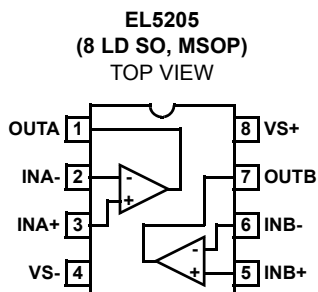
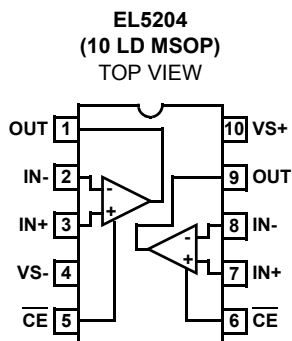
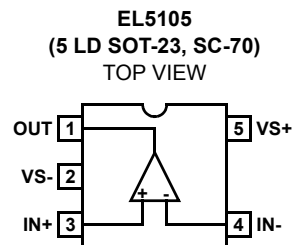
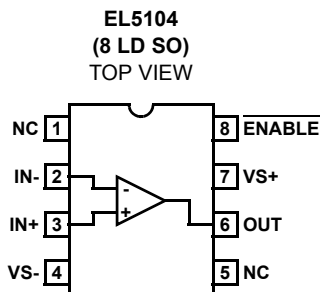
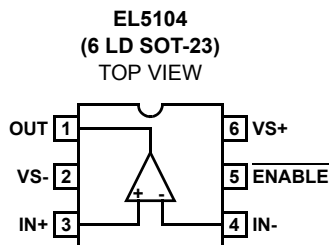
## **Features**

- Specified for 5V or  $\pm 5V$  applications
- Power-down to 17 $\mu A$
- -3dB bandwidth = 700MHz
- $\pm 0.1$ dB bandwidth = 45MHz
- Low supply current = 9.5mA
- Slew rate = 7000V/ $\mu s$
- Low offset voltage = 10mV max
- Output current = 160mA
- $A_{VOL} = 1400$
- Diff gain/phase = 0.01%/0.02°
- Pb-free plus anneal available (RoHS compliant)

## **Applications**

- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Pinouts



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5104IS	5104IS	-	8 Ld SO	MDP0027
EL5104IS-T7	5104IS	7"	8 Ld SO	MDP0027
EL5104IS-T13	5104IS	13"	8 Ld SO	MDP0027
EL5104ISZ (Note)	5104ISZ	-	8 Ld SO (Pb-Free)	MDP0027
EL5104ISZ-T7 (Note)	5104ISZ	7"	8 Ld SO (Pb-Free)	MDP0027
EL5104ISZ-T13 (Note)	5104ISZ	13"	8 Ld SO (Pb-Free)	MDP0027
EL5104IW-T7	n	7" (3K pcs)	6 Ld SOT-23	MDP0038
EL5104IW-T7A	n	7" (250 pcs)	6 Ld SOT-23	MDP0038
EL5104IWZ-T7 (Note)	BAEA	7" (3K pcs)	6 Ld SOT-23 (Pb-Free)	MDP0038
EL5104IWZ-T7A (Note)	BAEA	7" (250 pcs)	6 Ld SOT-23 (Pb-Free)	MDP0038
EL5105IC-T7	C	7" (3K pcs)	5 Ld SC-70	P5.049
EL5105IC-T7A	C	7" (250 pcs)	5 Ld SC-70	P5.049
EL5105IW-T7	f	7" (3K pcs)	5 Ld SOT-23	MDP0038
EL5105IW-T7A	f	7" (250 pcs)	5 Ld SOT-23	MDP0038
EL5105IWZ-T7 (Note)	BBMA	7" (3K pcs)	5 Ld SOT-23 (Pb-Free)	MDP0038
EL5105IWZ-T7A (Note)	BBMA	7" (250 pcs)	5 Ld SOT-23 (Pb-Free)	MDP0038

**Ordering Information** (Continued)

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5204IY	BTAAA	-	10 Ld MSOP	MDP0043
EL5204IY-T7	BTAAA	7"	10 Ld MSOP	MDP0043
EL5204IY-T13	BTAAA	13"	10 Ld MSOP	MDP0043
EL5204IYZ (Note)	BAAAF	-	10 Ld MSOP (Pb-Free)	MDP0043
EL5204IYZ-T7 (Note)	BAAAF	7"	10 Ld MSOP (Pb-Free)	MDP0043
EL5204IYZ-T13 (Note)	BAAAF	13"	10 Ld MSOP (Pb-Free)	MDP0043
EL5205IS	5205IS	-	8 Ld SO	MDP0027
EL5205IS-T7	5205IS	7"	8 Ld SO	MDP0027
EL5205IS-T13	5205IS	13"	8 Ld SO	MDP0027
EL5205ISZ (Note)	5205ISZ	-	8 Ld SO (Pb-Free)	MDP0027
EL5205ISZ-T7 (Note)	5205ISZ	7"	8 Ld SO (Pb-Free)	MDP0027
EL5205ISZ-T13 (Note)	5205ISZ	13"	8 Ld SO (Pb-Free)	MDP0027
EL5205IY	BVAAA	-	8 Ld MSOP	MDP0043
EL5205IY-T7	BVAAA	7"	8 Ld MSOP	MDP0043
EL5205IY-T13	BVAAA	13"	8 Ld MSOP	MDP0043
EL5205IYZ (Note)	BAAAG	-	8 Ld MSOP (Pb-free)	MDP0043
EL5205IYZ-T7 (Note)	BAAAG	7"	8 Ld MSOP (Pb-free)	MDP0043
EL5205IYZ-T13 (Note)	BAAAG	13"	8 Ld MSOP (Pb-free)	MDP0043
EL5304IU	5304IU	-	16 Ld QSOP	MDP0040
EL5304IU-T7	5304IU	7"	16 Ld QSOP	MDP0040
EL5304IU-T13	5304IU	13"	16 Ld QSOP	MDP0040
EL5304IUZ (Note)	5304IUZ	-	16 Ld QSOP (Pb-Free)	MDP0040
EL5304IUZ-T7 (Note)	5304IUZ	7"	16 Ld QSOP (Pb-Free)	MDP0040
EL5304IUZ-T13 (Note)	5304IUZ	13"	16 Ld QSOP (Pb-Free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# EL5104, EL5105, EL5204, EL5205, EL5304

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Supply Voltage between $V_{S+}$ and GND. . . . .	13.2V	Storage Temperature Range . . . . .	-65°C to +150°C
Input Voltage . . . . .	$\pm V_S$	Ambient Operating Temperature Range . . . . .	-40°C to +85°C
Differential Input Voltage . . . . .	$\pm 4\text{V}$	Operating Junction Temperature . . . . .	150°C
Maximum Output Current. . . . .	80mA		
$V_{S+}$ to $V_{S-}$ Maximum Slew Rate . . . . .	1V/ $\mu\text{s}$		

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

## DC Electrical Specifications $V_S = \pm 5\text{V}$ , $\text{GND} = 0\text{V}$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 0\text{V}$ , $V_{OUT} = 0\text{V}$ , $V_{ENABLE} = \text{GND or OPEN}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Offset Voltage	EL5104, EL5105, EL5204, EL5205	-10	3	10	mV
		EL5304	-18	5	18	mV
TCV <sub>OS</sub>	Offset Voltage Temperature Coefficient	Measured from T <sub>MIN</sub> to T <sub>MAX</sub>		10		$\mu\text{V}/^\circ\text{C}$
I <sub>B</sub>	Input Bias Current	$V_{IN} = 0\text{V}$		8	30	$\mu\text{A}$
I <sub>OS</sub>	Input Offset Current	$V_{IN} = 0\text{V}$		4	15	$\mu\text{A}$
TCI <sub>OS</sub>	Input Bias Current Temperature Coefficient	Measured from T <sub>MIN</sub> to T <sub>MAX</sub>		50		$\text{nA}/^\circ\text{C}$
PSRR	Power Supply Rejection Ratio		60	70		dB
CMRR	Common Mode Rejection Ratio	$V_{CM}$ from -3V to +3V	56	62		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3		+3	V
R <sub>IN</sub>	Input Resistance	Common mode	50	120		k $\Omega$
C <sub>IN</sub>	Input Capacitance	SO package		1		pF
I <sub>S,ON</sub>	Supply Current - Enabled	Per amplifier	8.5	9.5	11	mA
I <sub>S,OFF</sub>	Supply Current - Shut Down	$V_{S+}$ , per amplifier	+1	0	+25	$\mu\text{A}$
		$V_{S-}$ , per amplifier	-25	17	-1	$\mu\text{A}$
PSOR	Power Supply Operating Range		4		13.2	V
AVOL	Open Loop Gain	$R_L = 1\text{k}\Omega$ to GND	55	65		dB
		$R_L = 150\Omega$ to GND		60		dB
V <sub>OP</sub>	Positive Output Voltage Swing	$R_L = 150\Omega$ to 0V	3.6	3.8		V
V <sub>ON</sub>	Negative Output Voltage Swing	$R_L = 150\Omega$ to 0V		-3.8	-3.6	V
I <sub>OUT</sub>	Output Current	$R_L = 10\Omega$ to 0V	$\pm 90$	$\pm 160$		mA
V <sub>IH-EN</sub>	ENABLE Pin Voltage for Power Up		$(V_{S+})$ -5		$(V_{S+})$ -3	V
V <sub>IL-EN</sub>	ENABLE Pin Voltage for Shut Down		$(V_{S+})$ -1		$V_{S+}$	V

**EL5104, EL5105, EL5204, EL5205, EL5304**

**Closed Loop AC Electrical Specifications**  $V_S = +5V$ ,  $GND = 0V$ ,  $T_A = 25^\circ C$ ,  $V_{CM} = +1.5V$ ,  $V_{OUT} = +1.5V$ ,  $V_{CLAMP} = +5V$ ,  
 $V_{ENABLE} = 0V$ ,  $A_V = +1$ ,  $R_F = 0\Omega$ ,  $R_L = 150\Omega$  to GND pin, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth ( $V_{OUT} = 200mV_{P-P}$ )	$V_S = \pm 5V$ , $A_V = 1$ , $R_F = 0\Omega$		700		MHz
SR	Slew Rate	$R_L = 100\Omega$ , $V_{OUT} = -3V$ to $+3V$	2000	3000	7000	V/ $\mu s$
$t_R$ , $t_F$	Rise Time, Fall Time	$\pm 0.1V$ step		0.4		ns
OS	Overshoot	$\pm 0.1V$ step		10		%
$t_{PD}$	Propagation Delay	$\pm 0.1V$ step		0.4		ns
$t_S$	0.1% Settling Time	$V_S = \pm 5V$ , $R_L = 500\Omega$ , $A_V = 1$ , $V_{OUT} = \pm 2.5V$		7		ns
dG	Differential Gain	$A_V = 2$ , $R_L = 150\Omega$ , $V_{INDC} = -1$ to $+1V$		0.01		%
dP	Differential Phase	$A_V = 2$ , $R_L = 150\Omega$ , $V_{INDC} = -1$ to $+1V$		0.02		$^\circ$
$e_N$	Input Noise Voltage	$f = 10kHz$		10		nV/ $\sqrt{Hz}$
$i_N$	Input Noise Current	$f = 10kHz$		54		pA/ $\sqrt{Hz}$
$t_{DIS}$	Disable Time			180		ns
$t_{EN}$	Enable Time			650		ns
$I_{EN}$	Enable Pin Current	Enabled, $V_{EN} = 0V$	-1		1	$\mu A$
		Disabled, $V_{EN} = 5V$	1		25	$\mu A$

Typical Performance Curves

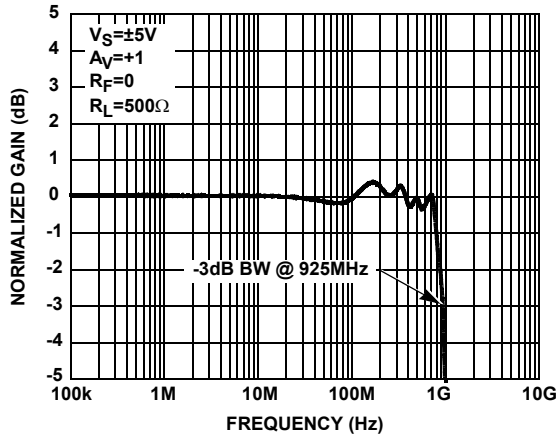


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

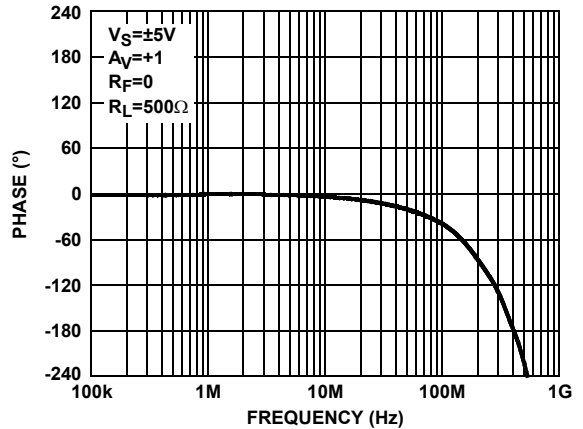


FIGURE 2. PHASE vs FREQUENCY

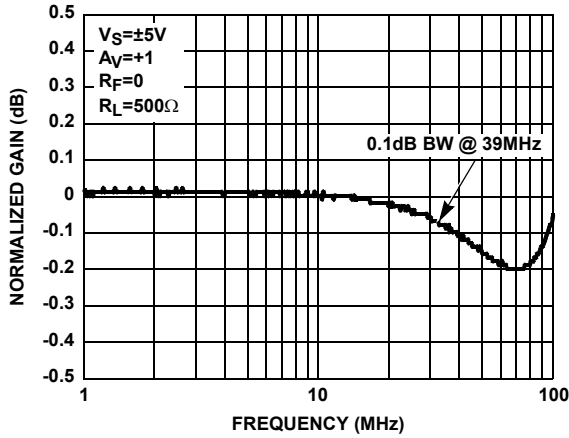


FIGURE 3. 0.1dB BANDWIDTH

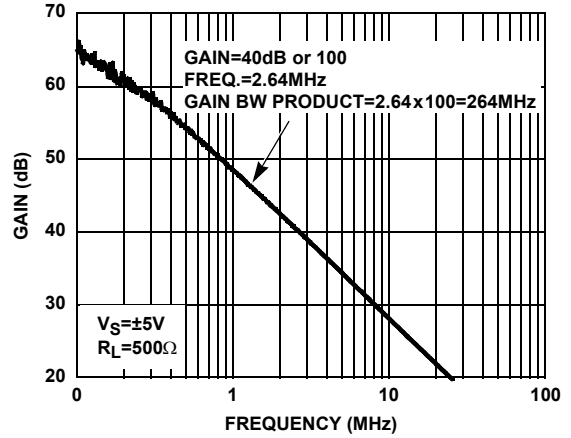


FIGURE 4. GAIN BANDWIDTH PRODUCT

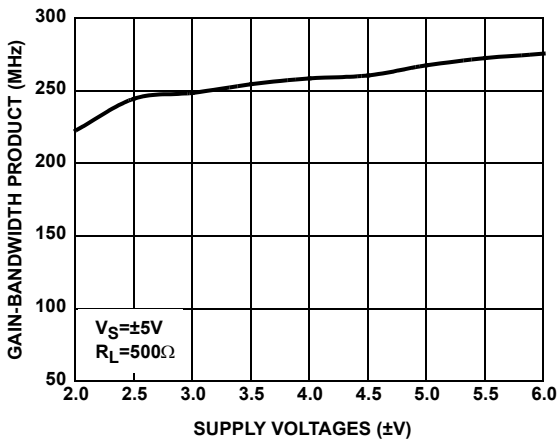


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

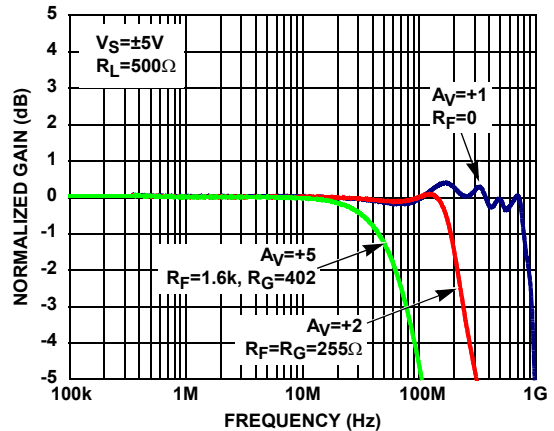


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS +AV

Typical Performance Curves (Continued)

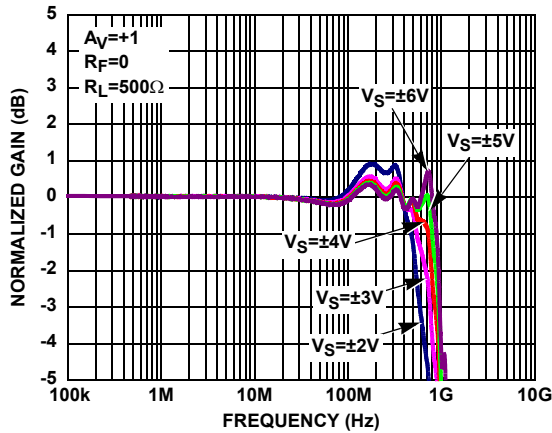


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS  $\pm V_S$

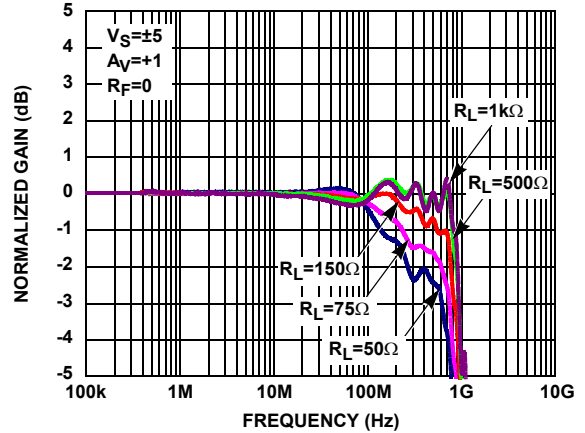


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS  $R_L$  ( $A_V=+1$ )

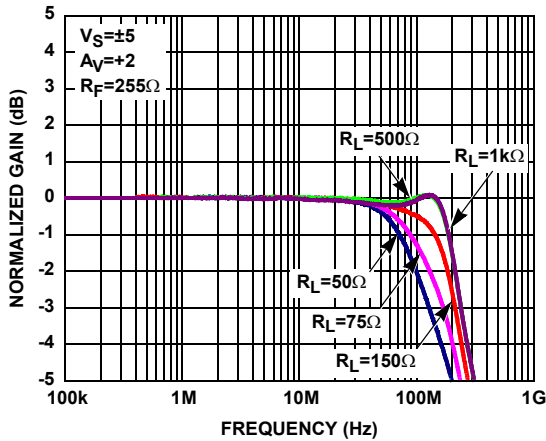


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS  $R_L$  ( $A_V=+2$ )

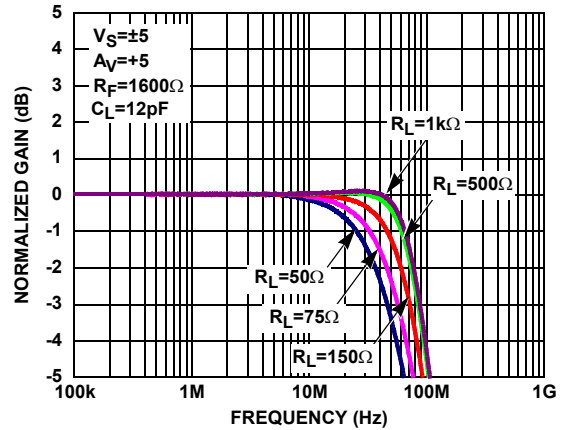


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS  $R_L$  ( $A_V=+5$ )

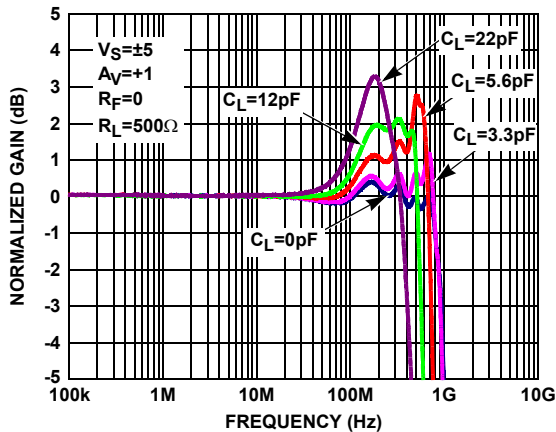


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS  $C_L$  ( $A_V=+1$ )

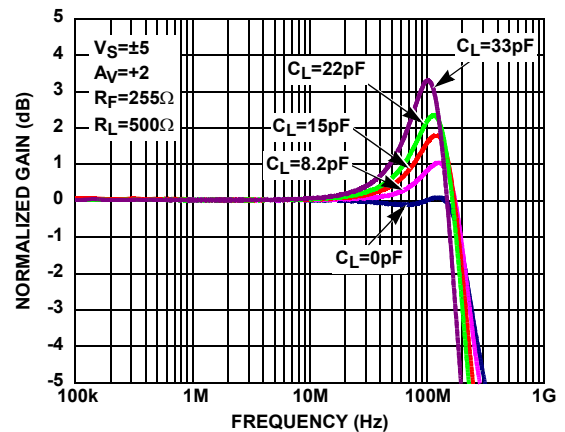


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS  $C_L$  ( $A_V=+2$ )

Typical Performance Curves (Continued)

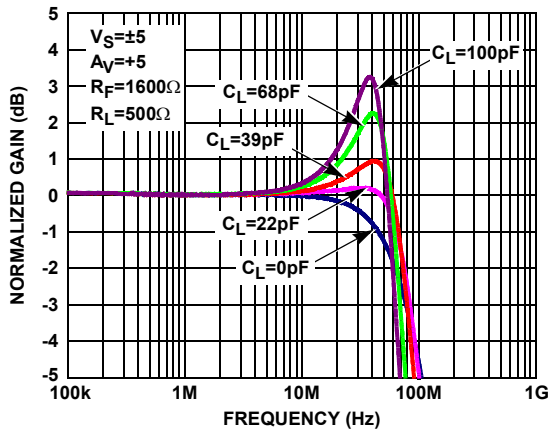


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS  $C_L$  ( $A_V = +5$ )

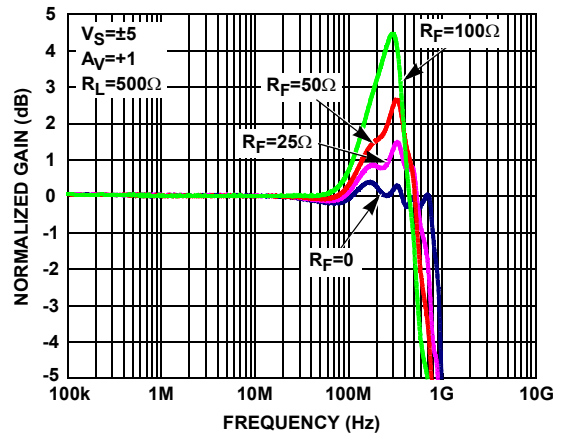


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS  $R_F$  ( $A_V = +1$ )

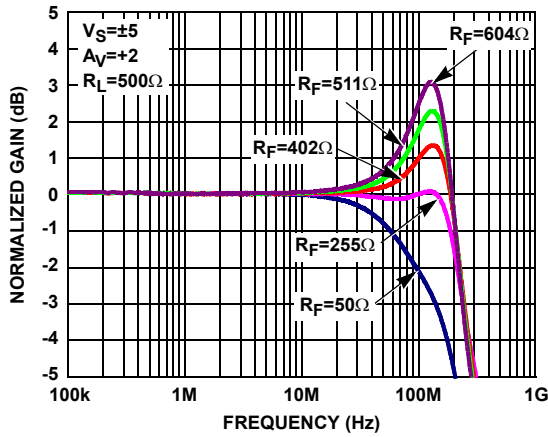


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS  $R_F$  ( $A_V = +2$ )

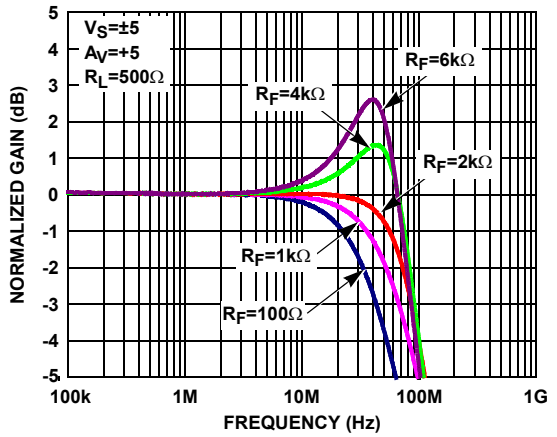


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS  $R_F$  ( $A_V = +5$ )

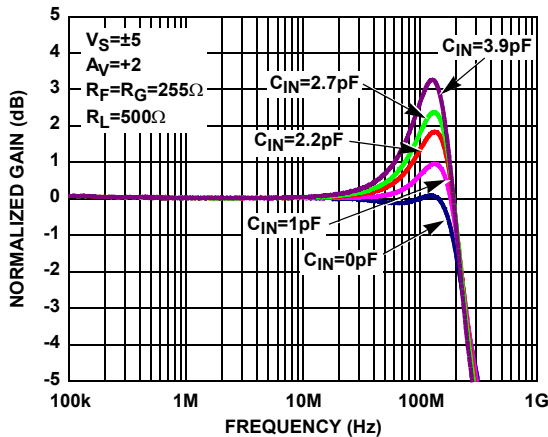


FIGURE 17. GAIN vs FREQUENCY FOR VARIOUS  $C_{IN(-)}$  ( $A_V = +2$ )

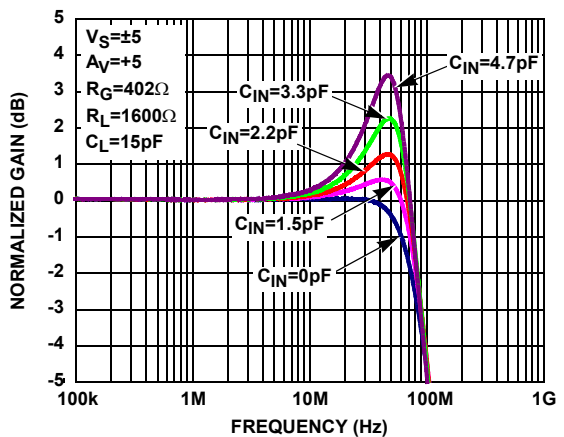


FIGURE 18. GAIN vs FREQUENCY FOR VARIOUS  $C_{IN(-)}$  ( $A_V = +5$ )



Typical Performance Curves (Continued)

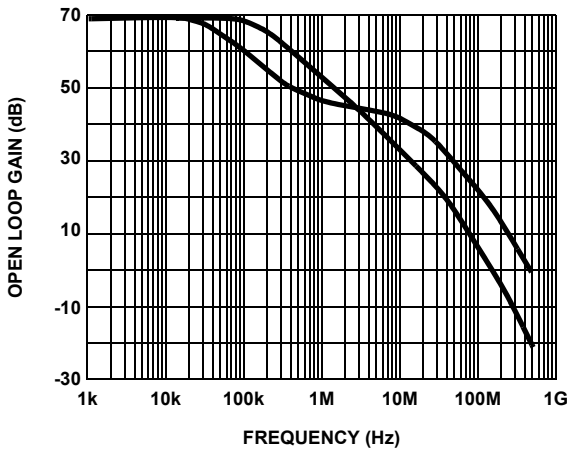


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

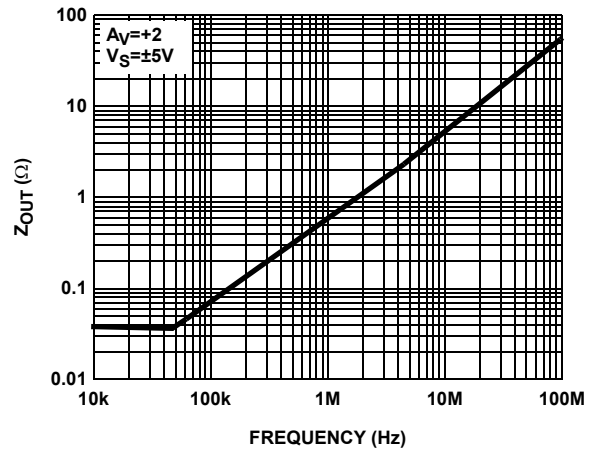


FIGURE 20.  $Z_{OUT}$  vs FREQUENCY

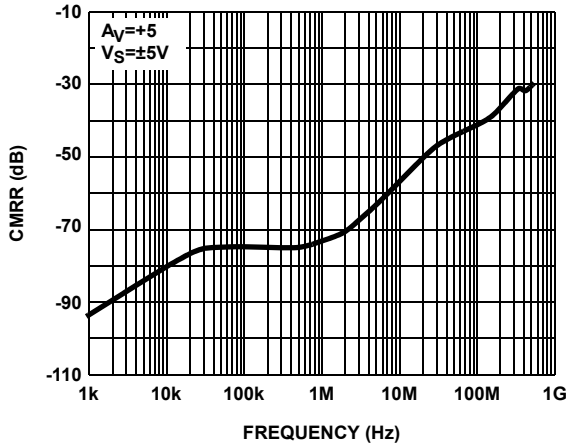


FIGURE 21. CMRR vs FREQUENCY

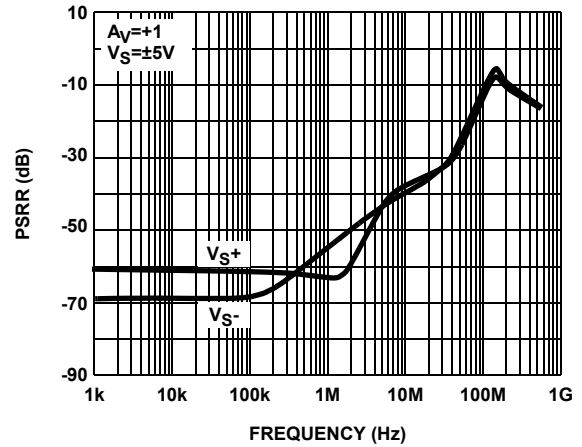


FIGURE 22. PSRR vs FREQUENCY

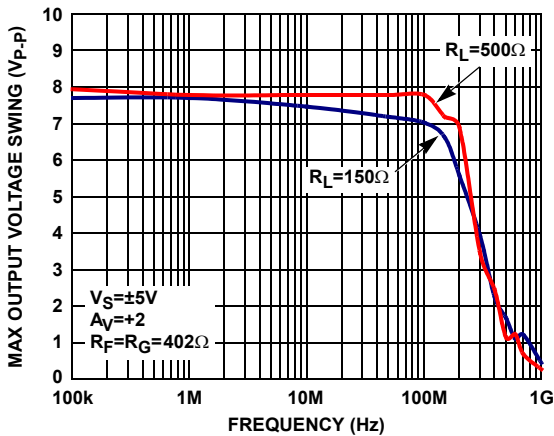


FIGURE 23. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

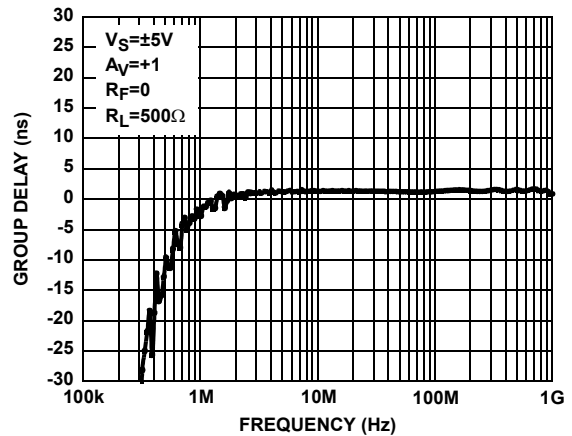


FIGURE 24. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

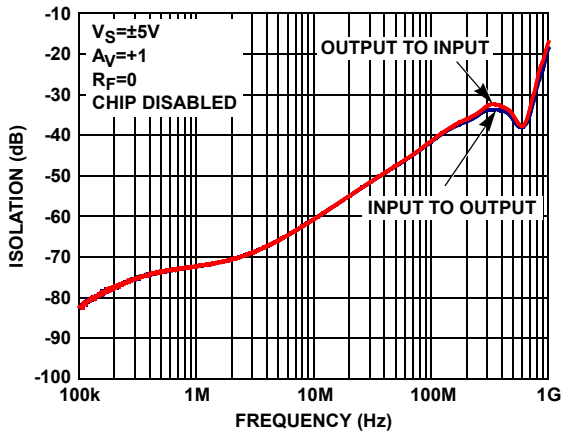


FIGURE 25. INPUT AND OUTPUT ISOLATION

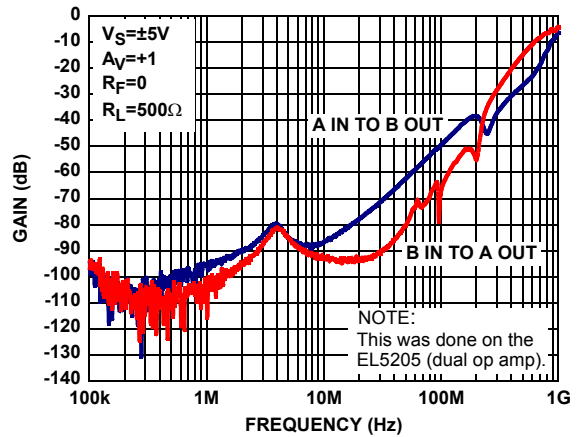


FIGURE 26. CHANNEL TO CHANNEL ISOLATION

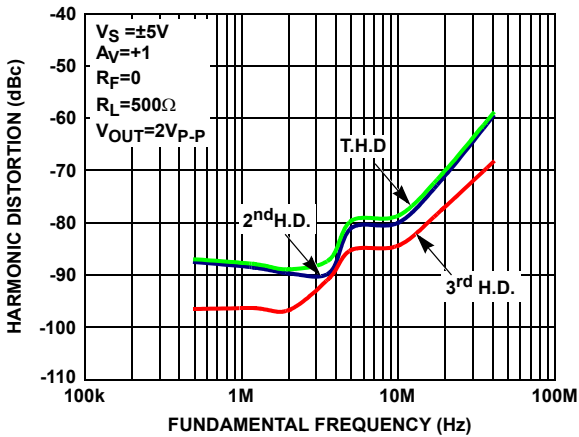


FIGURE 27. HARMONIC DISTORTION vs FREQUENCY

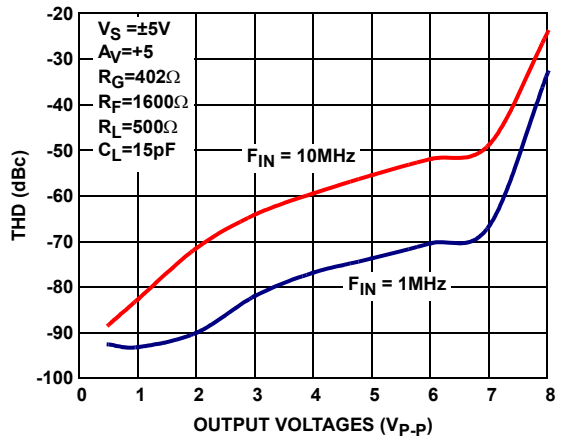


FIGURE 28. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

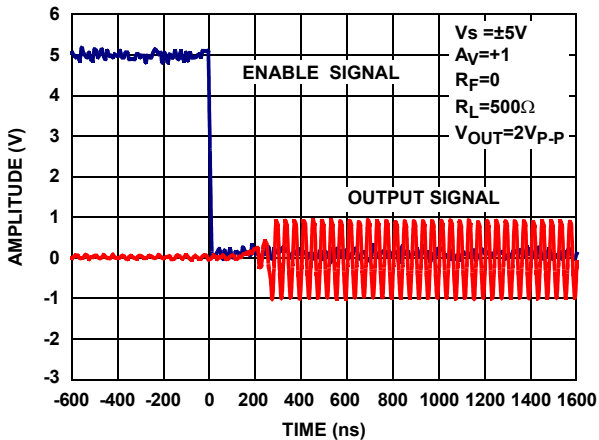


FIGURE 29. TURN-ON TIME

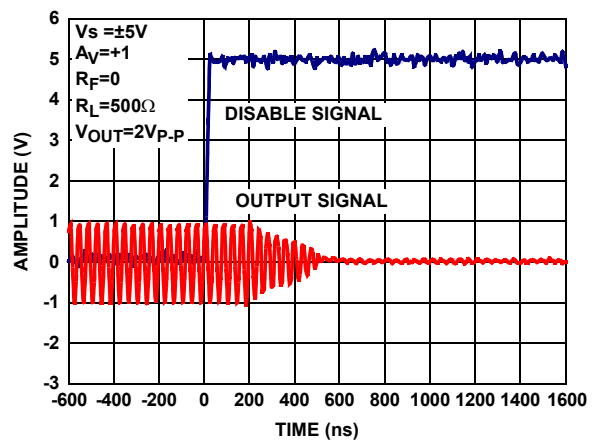


FIGURE 30. TURN-OFF TIME

Typical Performance Curves (Continued)

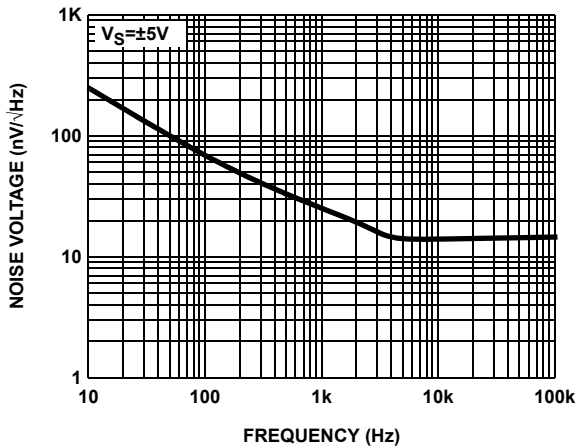


FIGURE 31. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

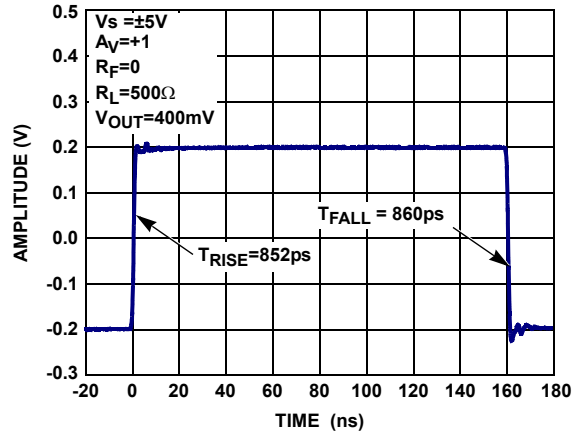


FIGURE 32. SMALL SIGNAL STEP RESPONSE\_RISE & FALL TIME

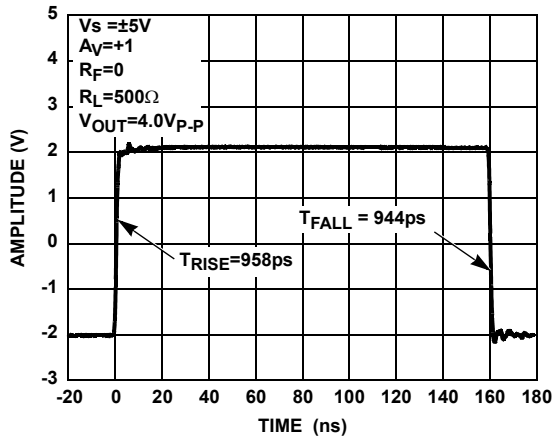


FIGURE 33. LARGE SIGNAL STEP RESPONSE\_RISE & FALL TIME

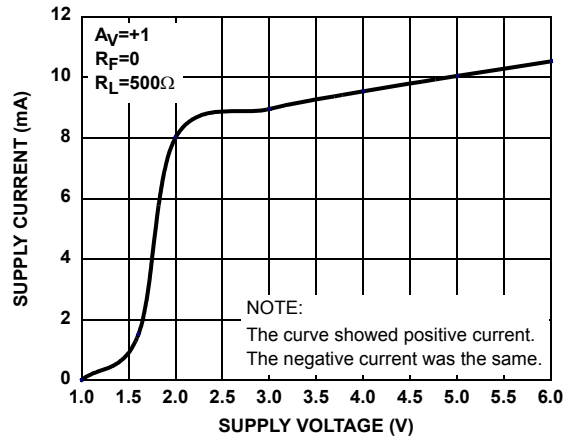


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

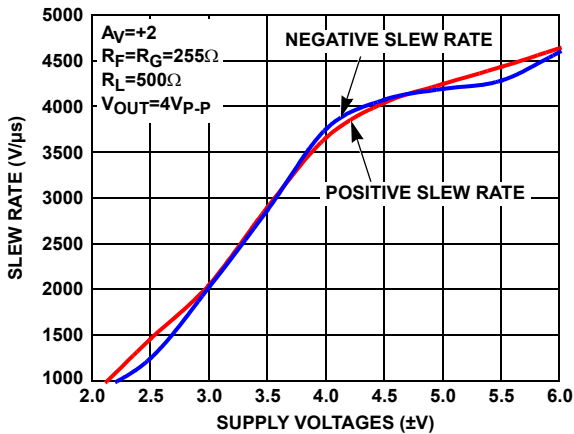


FIGURE 35. SLEW RATE vs SUPPLY VOLTAGES

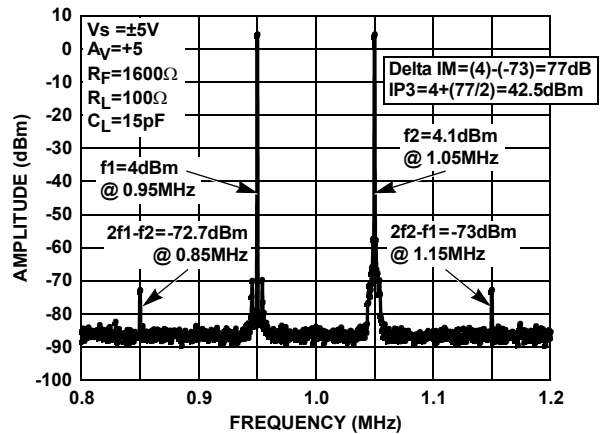


FIGURE 36. THIRD ORDER IMD INTERCEPT (IP3)

Typical Performance Curves (Continued)

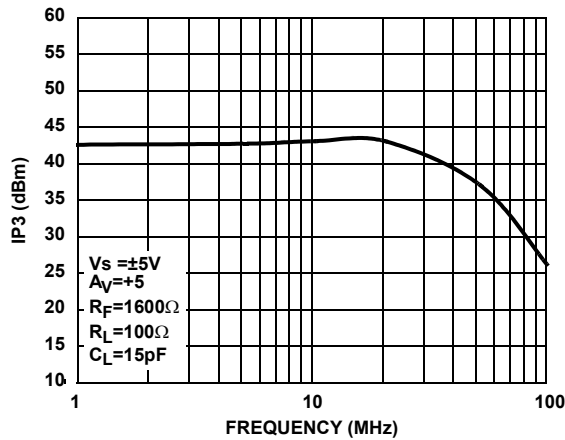


FIGURE 37. THIRD ORDER IMD INTERCEPT vs FREQUENCY

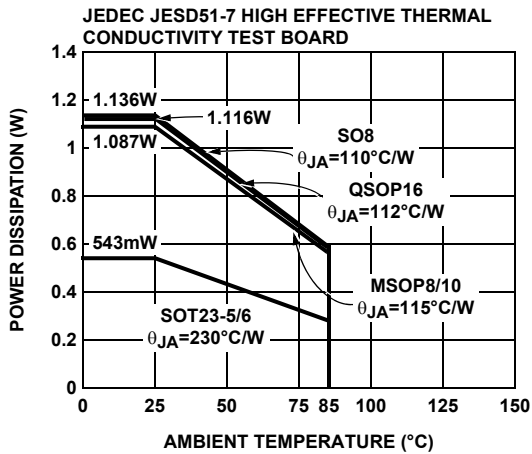


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

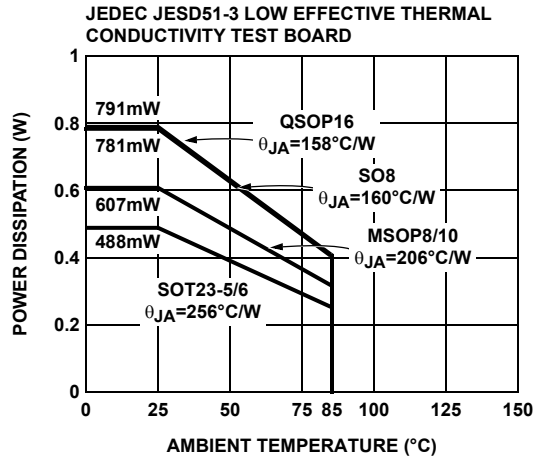
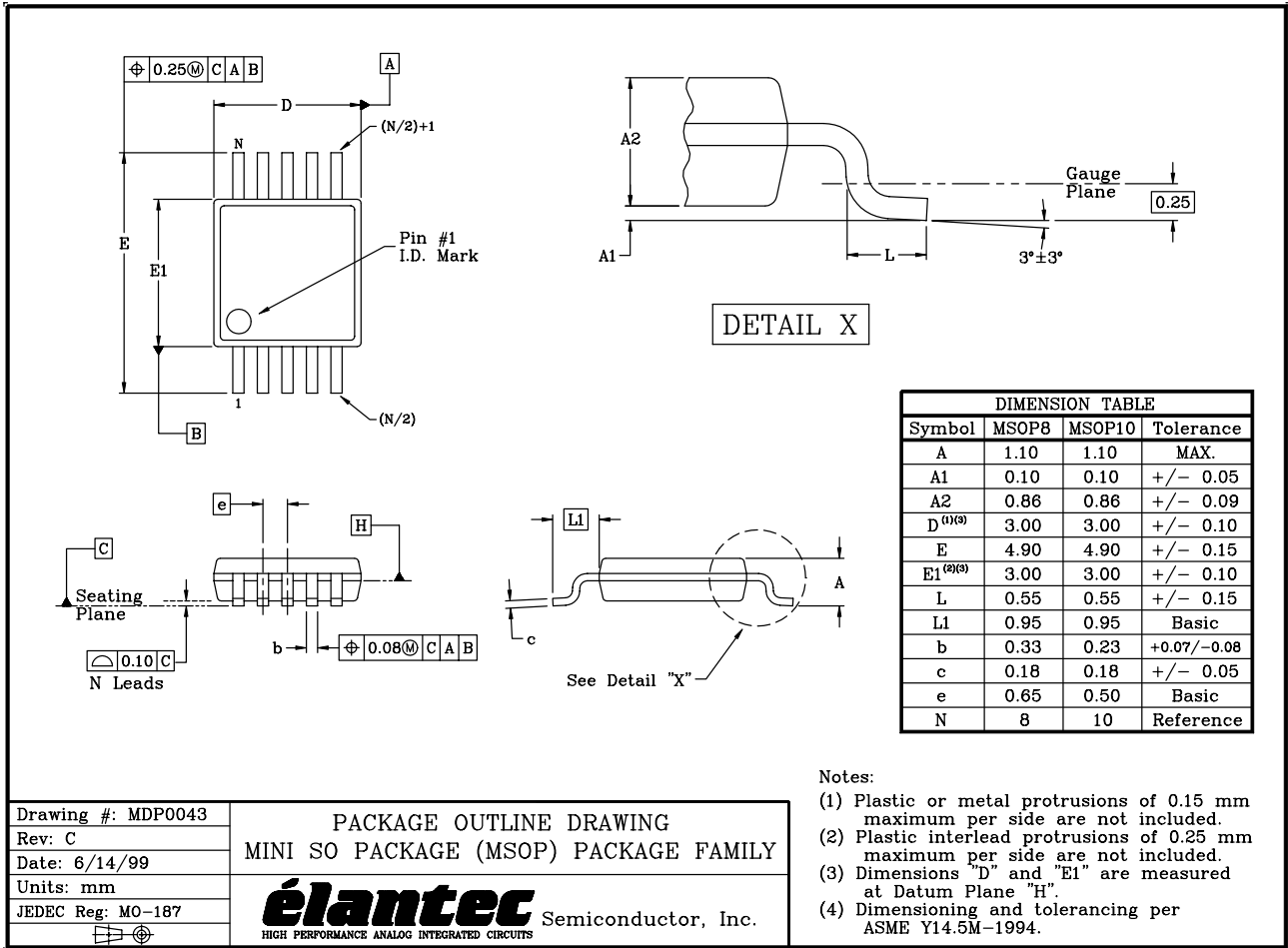


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

MSOP Package Outline Drawing

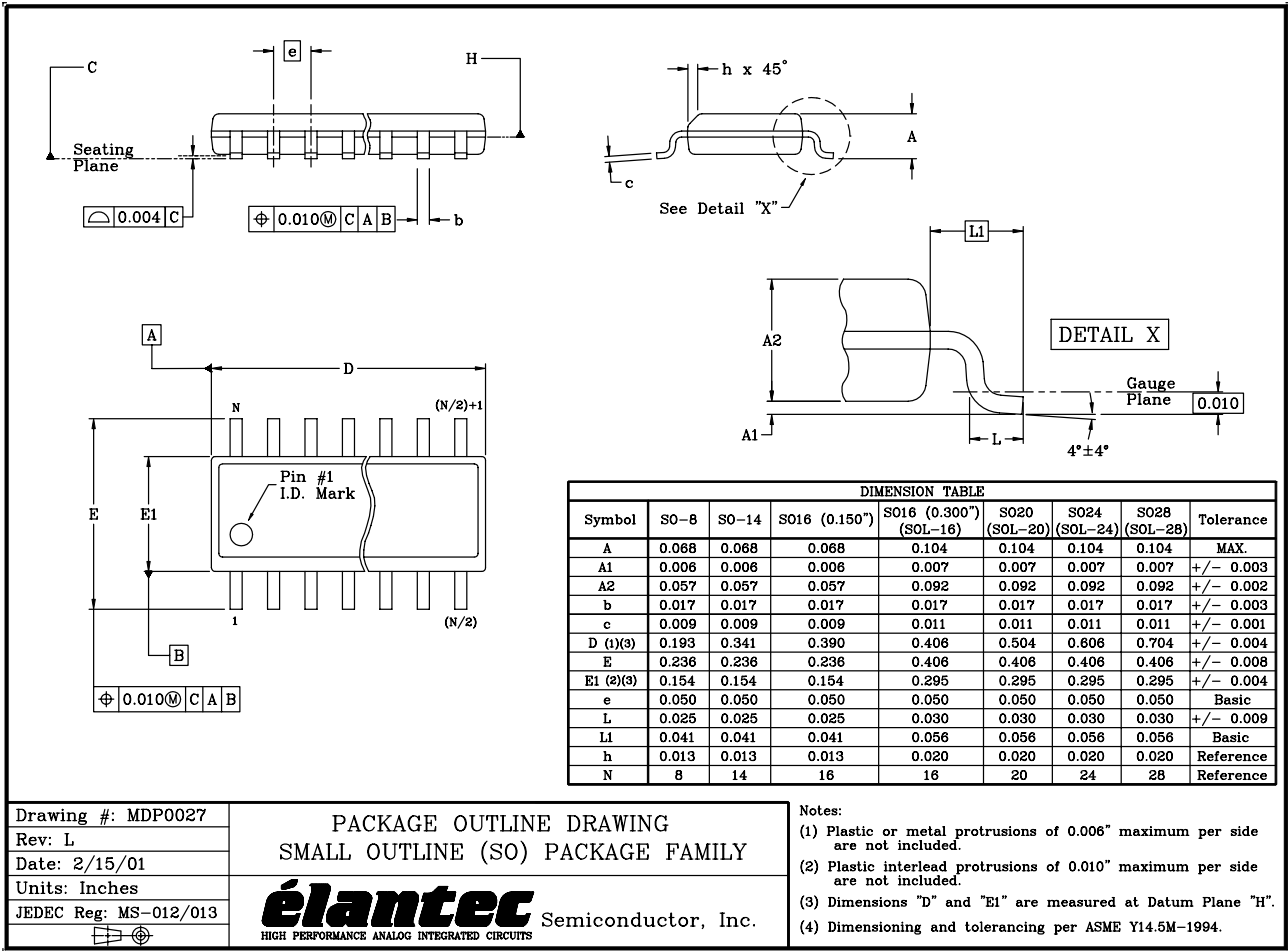


Notes:

- (1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- (2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
- (3) Dimensions "D" and "E1" are measured at Datum Plane "H".
- (4) Dimensioning and tolerancing per ASME Y14.5M-1994.

Drawing #: MDP0043	PACKAGE OUTLINE DRAWING MINI SO PACKAGE (MSOP) PACKAGE FAMILY  Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Rev: C	
Date: 6/14/99	
Units: mm	
JEDEC Reg: MO-187	

SO Package Outline Drawing

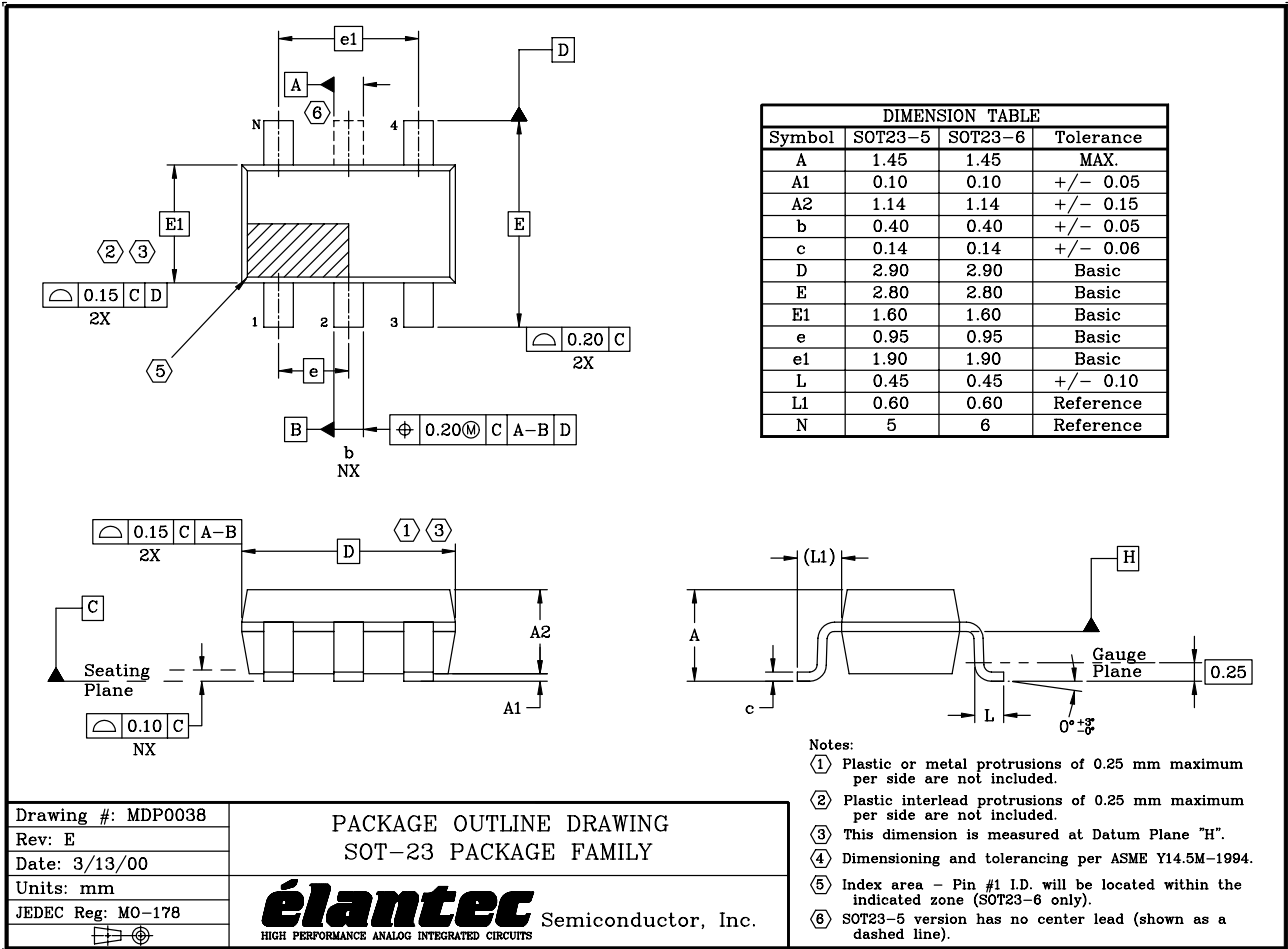


Drawing #: MDP0027  
 Rev: L  
 Date: 2/15/01  
 Units: Inches  
 JEDEC Reg: MS-012/013

PACKAGE OUTLINE DRAWING  
 SMALL OUTLINE (SO) PACKAGE FAMILY

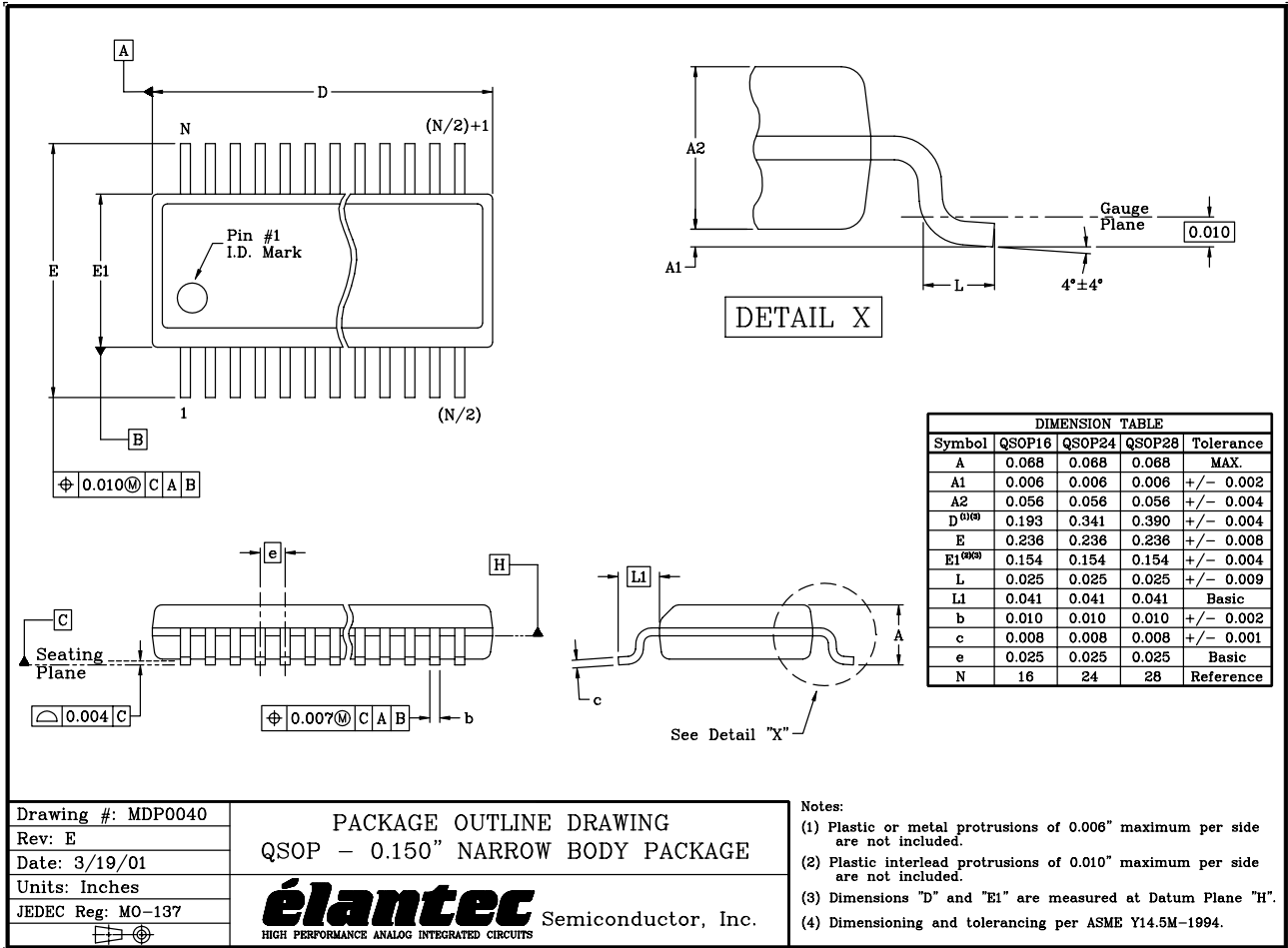


SOT-23 Package Outline Drawing



Drawing #: MDP0038	<p>PACKAGE OUTLINE DRAWING SOT-23 PACKAGE FAMILY</p> <p>Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS</p>
Rev: E	
Date: 3/13/00	
Units: mm	
JEDEC Reg: MO-178	

QSOP Package Outline Drawing

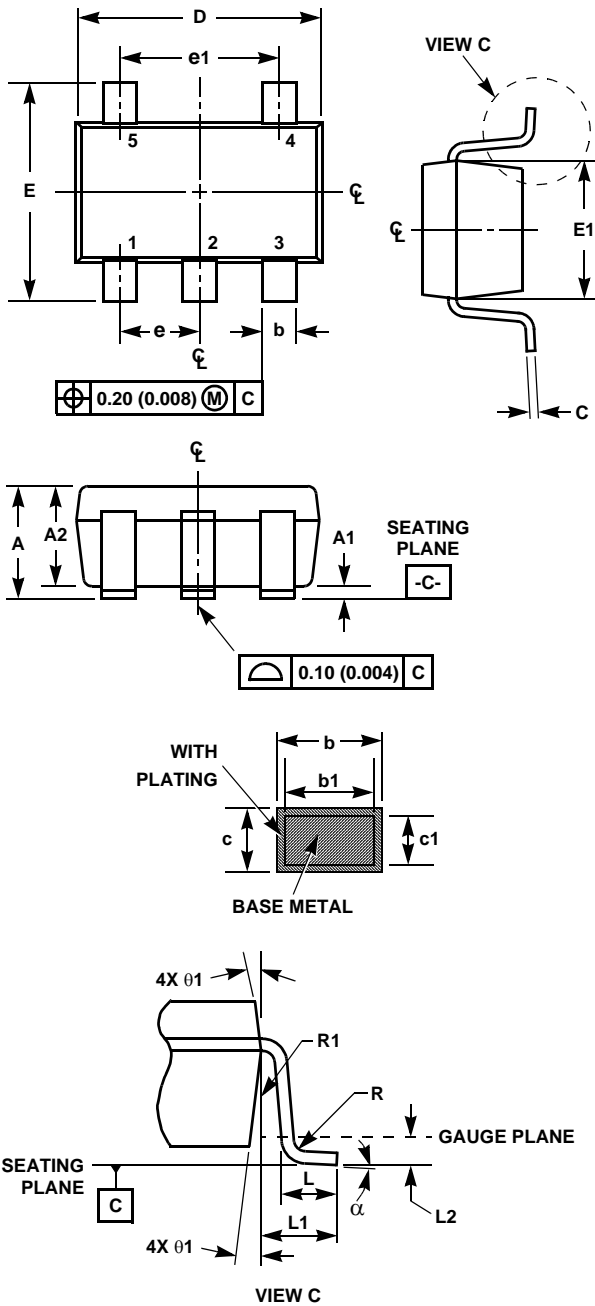


Drawing #: MDP0040	PACKAGE OUTLINE DRAWING QSOP - 0.150" NARROW BODY PACKAGE Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Rev: E	
Date: 3/19/01	
Units: Inches	
JEDEC Reg: MO-137	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>



Small Outline Transistor Plastic Packages (SC70-5)



P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		-
$\alpha$	0°	8°	0°	8°	-
N	5		5		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.15	0.25	-

Rev. 2 9/03

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)