

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby 275 μ W Max
- Low Power Operation55mW/MHz Max
- Fast Access Time 120/200ns Max
- Industry Standard Pinout
- Single Supply 5.0V VCC
- TTL Compatible
- Static Memory Cells
- High Output Drive
- On-Chip Address Latches
- Easy Microprocessor Interfacing

Description

The HM-6516/883 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, which also gives fast access times. The pinout of the HM-6516/883 is the popular 24 pin, 8-bit wide JEDEC Standard which allows easy memory board layouts, flexible enough to accommodate a variety of PROMs, RAMS, EPROMs, and ROMs.

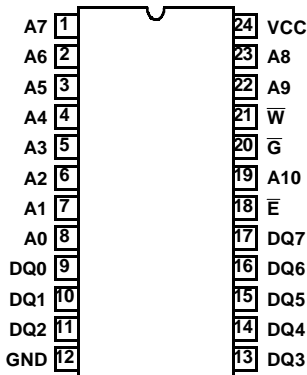
The HM-6516/883 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Ordering Information

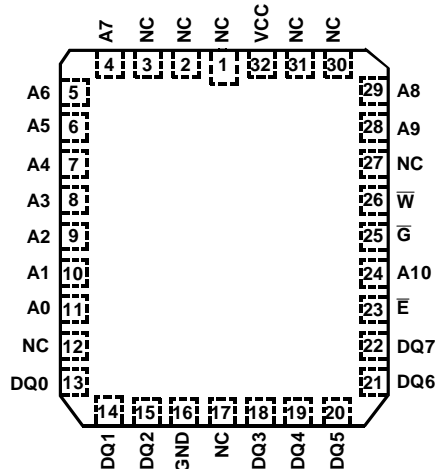
120ns	200ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HM1-6516B/883	HM1-6516/883	-55 $^{\circ}$ C to 125 $^{\circ}$ C	CERDIP	F24.6
HM4-6516B/883	-	-55 $^{\circ}$ C to +125 $^{\circ}$ C	CLCC	J32.A

Pinouts

HM-6516/883
(CERDIP)
TOP VIEW

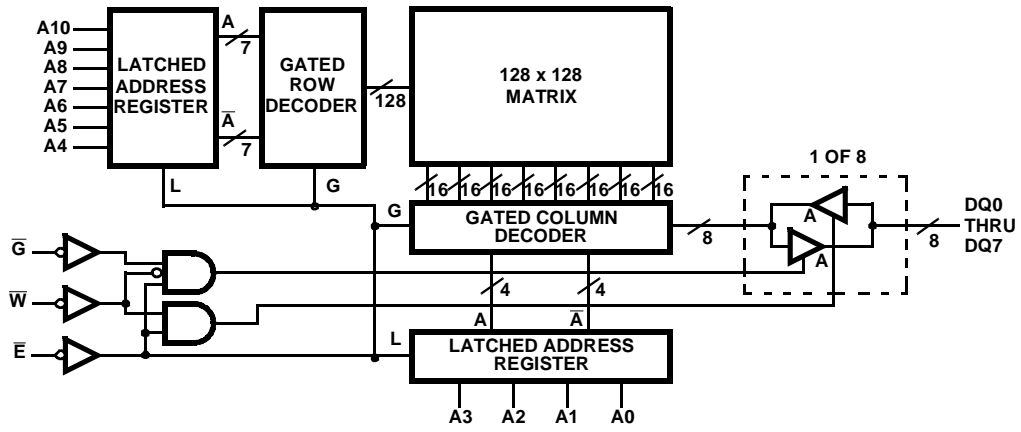


HM-6516/883
(CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Inputs
\bar{E}	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
\bar{W}	Write Enable
\bar{G}	Output Enable

Functional Diagram



HM-6516/883

Absolute Maximum Ratings

Supply Voltage +7.0V
 Input or Output Voltage Applied for all Grades. GND -0.3V to VCC +0.3V
 ESD Classification Class 1

Thermal Information

Thermal Resistance θ_{JA} θ_{JC}
 CERDIP Package 48°C/W 8°C/W
 CLCC Package 66°C/W 12°C/W
 Maximum Storage Temperature Range -65°C to +150°C
 Maximum Junction Temperature. +175°C
 Maximum Lead Temperature (Soldering 10s). +300°C

Die Characteristics

Gate Count 25953 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range. +4.5V to +5.5V Input High Voltage. +2.4V to VCC
 Operating Temperature Range. -55°C to +125°C Data Retention Supply Voltage. 2.0V to 4.5V
 Input Low Voltage. 0V to +0.8V Input Rise and Fall Time 40ns Max

TABLE 1. HM-6516/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH	VCC = 4.5V IO = -1.0mA	1, 2, 3	-55°C ≤ T _A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V IO = 3.2mA	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = \bar{G} = 5.5 V, VIO = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-1.0	1.0	μA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-1.0	1.0	μA
Operating Supply Current	ICCOP	VCC = \bar{G} = 5.5V, (Note 2) f = 1MHz, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	10	mA
Standby Supply Current	ICCSB1	VCC = 5.5V, HM-6516/883 \bar{E} = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	100	μA
		VCC = 5.5V, HM-6516B/883 \bar{E} = VCC -0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	50	μA
Data Retention Supply Current	ICCDR	VCC = 2.0V, HM-6516/883 \bar{E} = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	50	μA
		VCC = 2.0V, HM-6516B/883 \bar{E} = VCC-0.3V, IO = 0mA, VI = GND or VCC	1, 2, 3	-55°C ≤ T _A ≤ +125°C	-	25	μA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T _A ≤ +125°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

HM-6516/883

TABLE 2. HM-6514/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6516B/883		HM-6516/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	120	-	200	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, (Note 3)	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	120	-	200	ns
Chip Enable Pulse Negative Width	(9) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	120	-	200	-	ns
Chip Enable Pulse Positive Width	(10) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	50	-	80	-	ns
Address Set-up Time	(11) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0	-	0	-	ns
Address Hold Time	(12) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	30	-	50	-	ns
Write Enable Pulse Width	(13) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	120	-	200	-	ns
Write Enable Pulse Set-up Time	(14) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	120	-	200	-	ns
Chip Selection to End of Write	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	120	-	200	-	ns
Data Set-up Time	(16) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	50	-	80	-	ns
Data Hold Time	(17) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	10	-	10	-	ns
Read or Write Cycle Time	(18) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	170	-	280	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

HM-6516/883

TABLE 3. HM-6516/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	T _A = +25°C	-	8	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	T _A = +25°C	-	12	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	T _A = +25°C	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	T _A = +25°C	-	14	pF
Chip Enable to Output Valid Time	(3) TELQX	VCC = 4.5 and 5.5V	1	-55°C ≤ T _A ≤ +125°C	10	-	ns
Write Enable Output Disable Time	(4) TWLQZ	VCC = 4.5 and 5.5V HM-6516/883	1	-55°C ≤ T _A ≤ +125°C	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	-55°C ≤ T _A ≤ +125°C	-	50	ns
Chip Enable Output Disable Time	(5) TEHQZ	VCC = 4.5 and 5.5V HM-6516/883	1	-55°C ≤ T _A ≤ +125°C	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	-55°C ≤ T _A ≤ +125°C	-	50	ns
Output Enable Access Time	(6) TGLQV	VCC = 4.5 and 5.5V	1	-55°C ≤ T _A ≤ +125°C	-	80	ns
Output Enable to Output Valid Time	(7) TGLQX	VCC = 4.5 and 5.5V	1	-55°C ≤ T _A ≤ +125°C	10	-	ns
Output Disable Time	(8) TGHQZ	VCC = 4.5 and 5.5V HM-6516/883	1	-55°C ≤ T _A ≤ +125°C	-	80	ns
		VCC = 4.5 and 5.5V HM-6516B/883	1	-55°C ≤ T _A ≤ +125°C	-	50	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to LCC device types only.
3. Applies to DIP device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

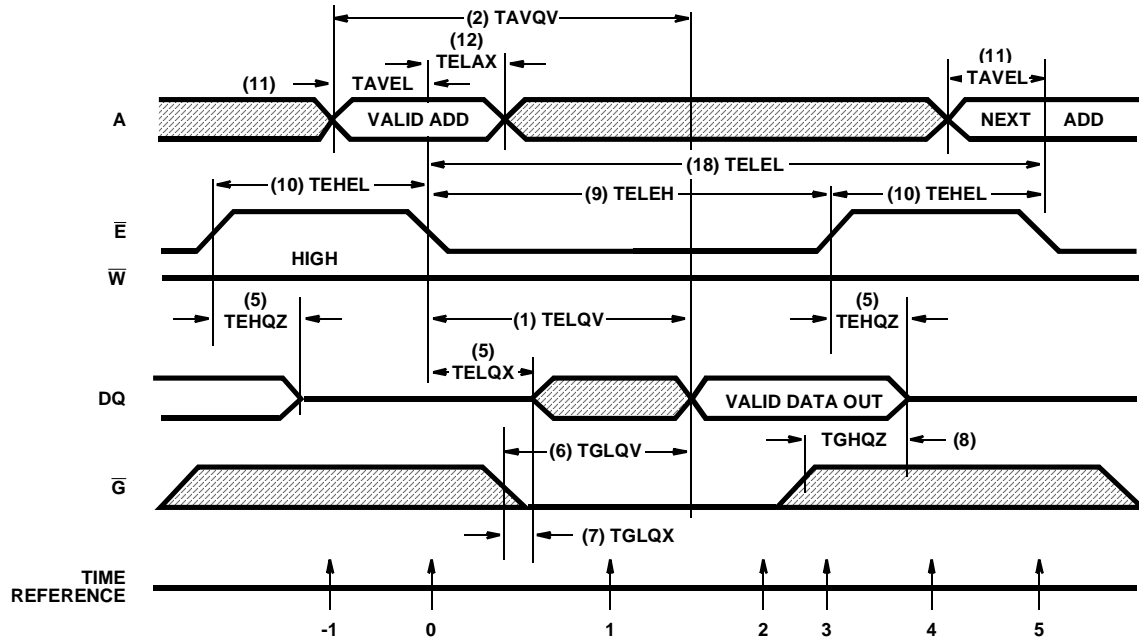


FIGURE 1. READ CYCLE

The address information is latched in the on-chip registers on the falling edge of \bar{E} ($T = 0$), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time ($T = 1$), the outputs become enabled but data is not valid until time ($T = 2$), \bar{W} must remain high throughout

the read cycle. After the data has been read, \bar{E} may return high ($T = 3$). This will force the output buffers into a high impedance mode at time ($T = 4$). \bar{G} is used to disable the output buffers when in a logical "1" state ($T = -1, 0, 3, 4, 5$). After ($T = 4$) time, the memory is ready for the next cycle.

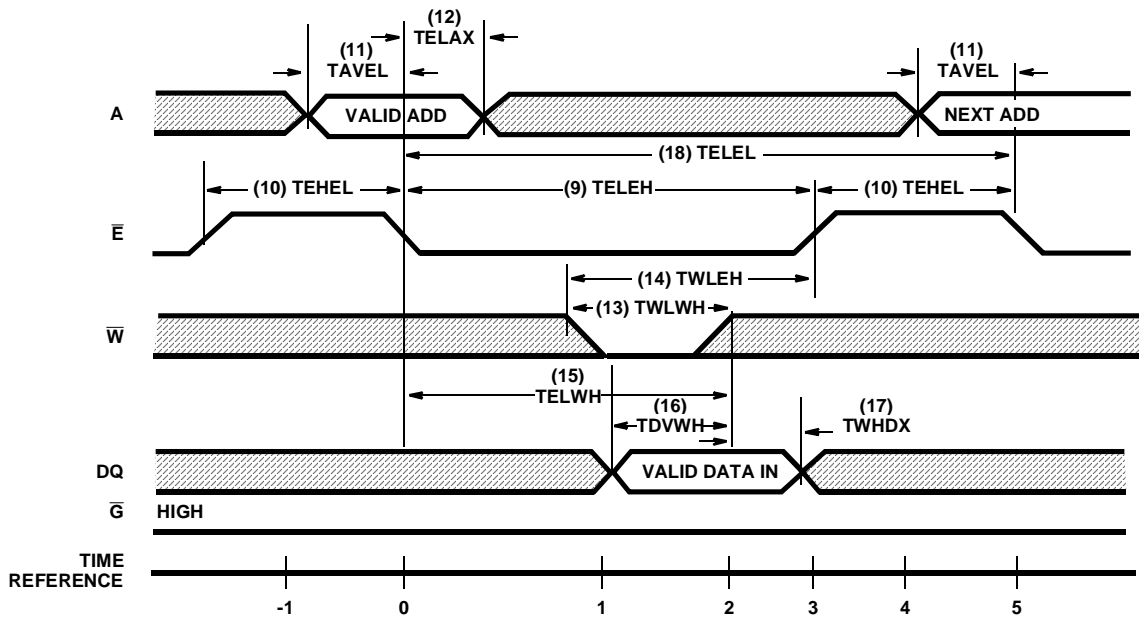


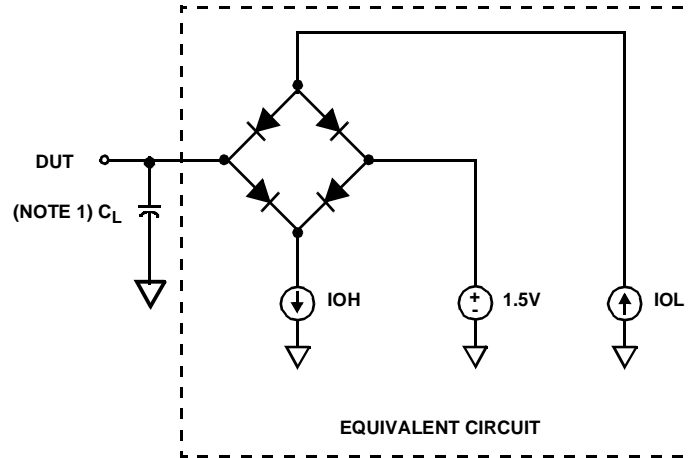
FIGURE 2. WRITE CYCLE

The write cycle is initiated on the falling edge of \bar{E} ($T = 0$), which latches the address information in the on-chip registers. If a write cycle is to be performed where the output is not to become active, \bar{G} can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of \bar{G} . If \bar{E} and \bar{G} fall before \bar{W} falls (read mode), a possible bus conflict may exist. If \bar{E} rises before \bar{W} rises, reference data

setup and hold times to the \bar{E} rising edge. The write operation is terminated by the first rising edge of \bar{W} ($T = 2$) or \bar{E} ($T = 3$). After the minimum \bar{E} high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the \bar{W} line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of \bar{E} .

HM-6516/883

Test Circuit

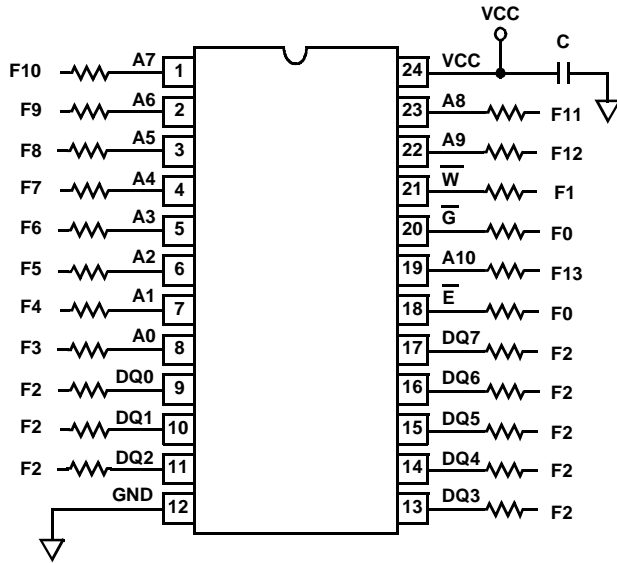


NOTE:

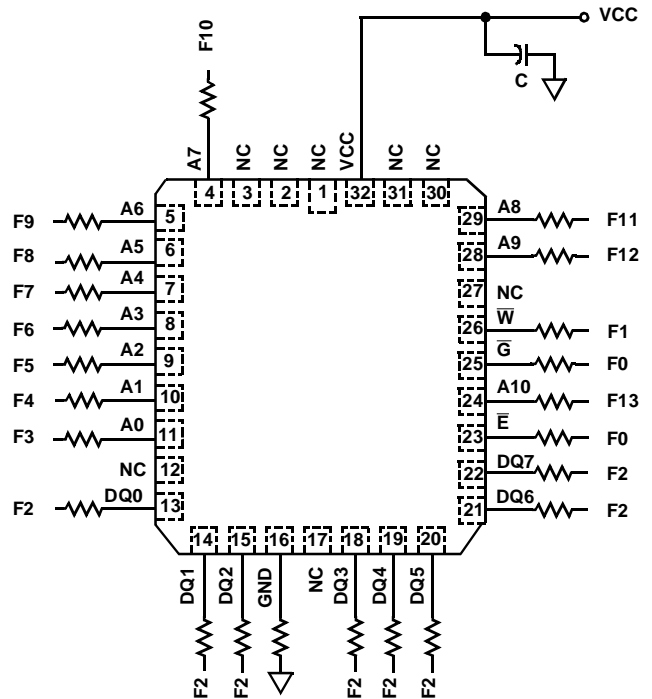
1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuits

HM-6516/883
CERDIP
TOP VIEW



HM-6516/883
CLCC
TOP VIEW



NOTES:

- All resistors $47k\Omega \pm 5\%$.
- $F0 = 100kHz \pm 10\%$.
- $VCC = 5.5V \pm 0.5V$.
- $V_{IH} = 4.5V \pm 10\%$.
- $V_{IL} = -0.2V$ to $+0.4V$.
- $C1 = 0.01\mu F$ Min.

HM-6516/883

Die Characteristics

DIE DIMENSIONS:
186.6 x 199.6 x 19 ±1mils

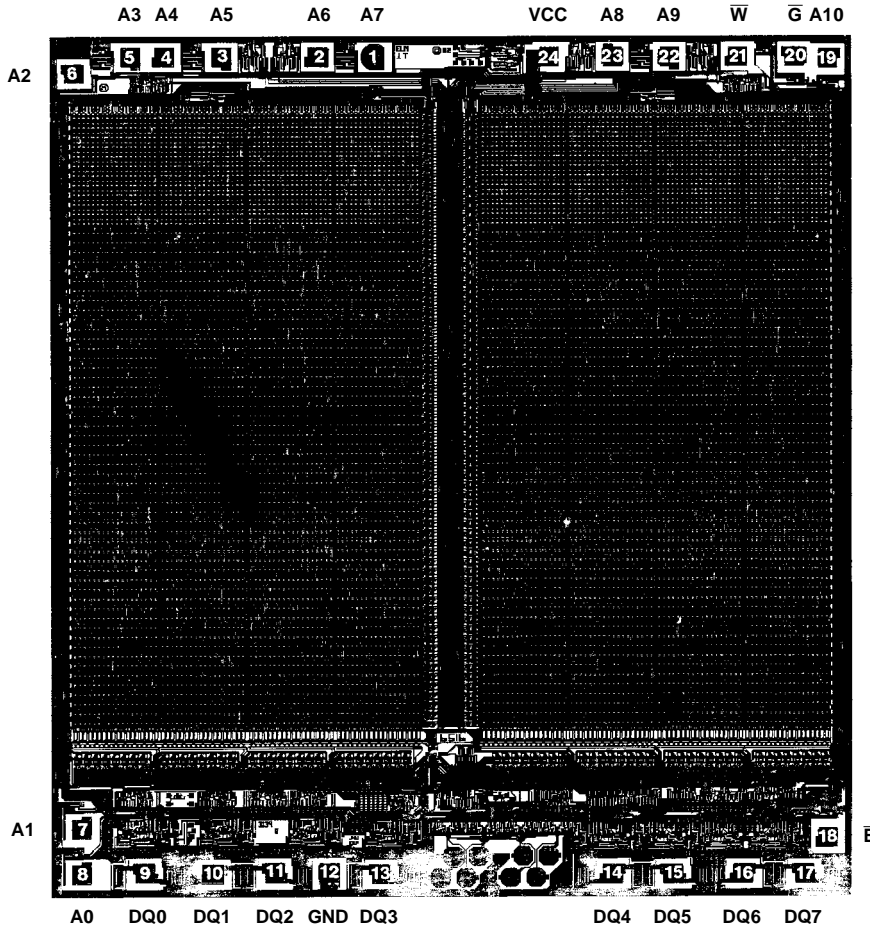
METALLIZATION:
Type: Si - Al
Thickness: 9kÅ - 13kÅ

GLASSIVATION:
Type: SiO₂
Thickness: 7kÅ ±9kÅ

WORST CASE CURRENT DENSITY:
0.5 x 10⁵ A/cm²

Metallization Mask Layout

HM-6516/883



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com