HM101510 Series

1,048,576-word × 1-bit Random Access Memory

The Hitachi HM101510 is ECL 100 K compatible, 1,048,576 words by 1 bits read/write random access memory developed for high speed systems.

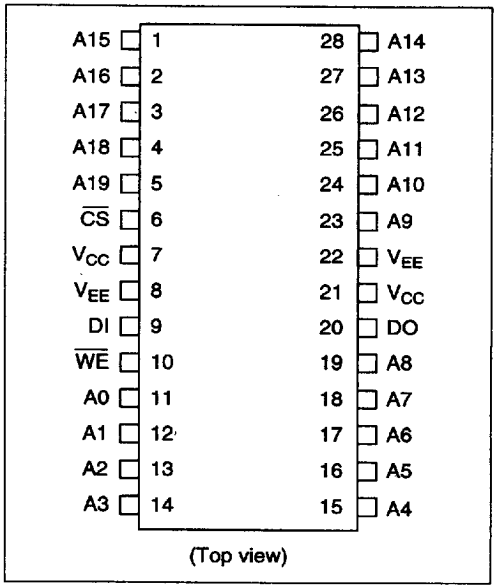
Features

- 1,048,576-words × 1 bit organization
- Fully compatible with 100 K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access Time: 15 ns max
- Write pulse width: 9 ns min
- Low power dissipation: 700 mW typ
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101510F-15	15 ns	28 pin ceramic flat (30 mil lead pitch) (FG-28DB)

Pin Arrangement



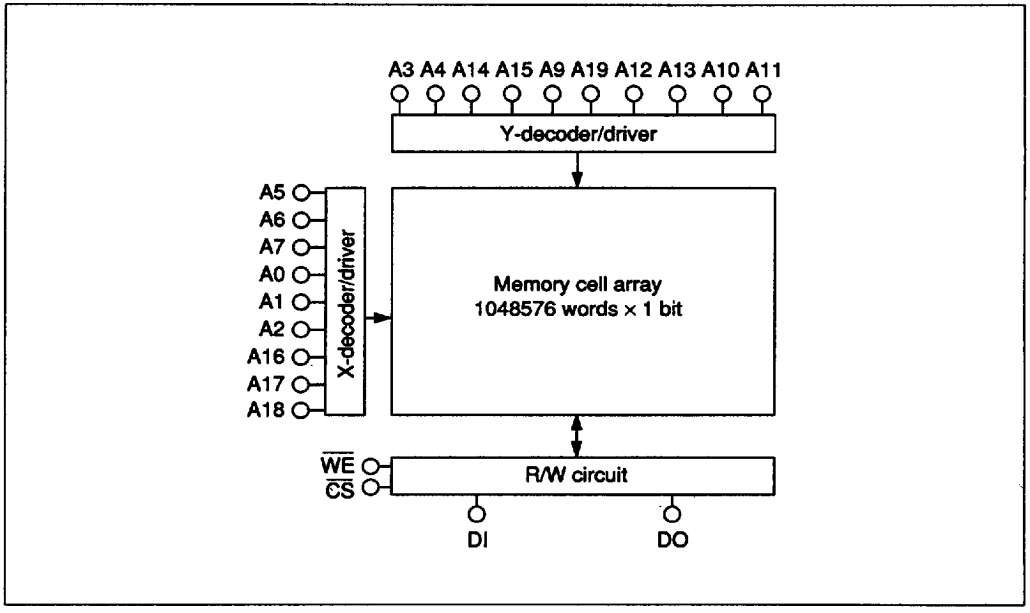
(Top view)

Pin Description

Pin name	Function
A0 – A19	Address input
DI	Data input
DO	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

2

Block Diagram



Function Table

Input				
$\overline{CS}$	$\overline{WE}$	DIn	Output	Mode
H	X*1	X*1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X*1	Dout*2	Read

Notes: 1. Irrelevant
2. Read out noninvert

Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: 1. Under bias (V_{EE} = –6.0 V min)

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +75°C)

Parameter	Symbol	Min (B)	Typ	Max (A)	Unit	Test condition
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/low for all input
	V_{IL}	–1810	—	–1475	mV	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—	µA	Others
Supply current	I_{EE}	–180	—	—	mA	All outputs open

AC Characteristics (V_{EE} = –5.2 V ± 5%, Tc = 0 to +75°C)

Read Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Chip select access time	t_{ACS}	—	—	10	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Write pulse width	t_W	9	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	3	—	—	ns	
Data hold	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	3	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	3	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

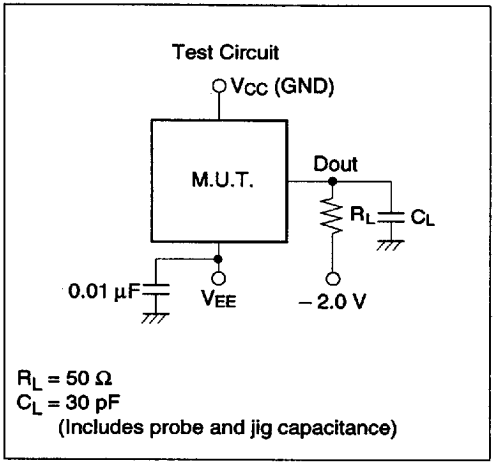
Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Output rise time	t_r	—	1.5	—	ns	
Output fall time	t_f	—	1.5	—	ns	

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

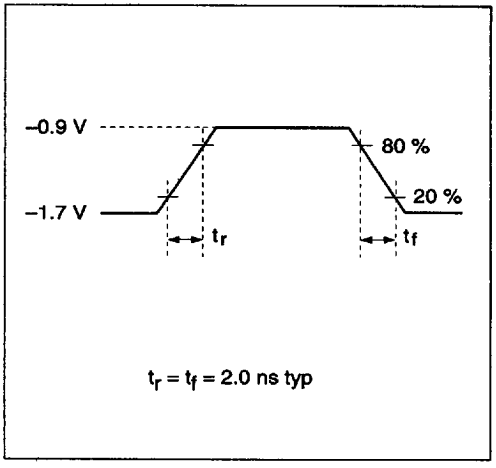
Test Circuit and Waveforms

Loading Condition



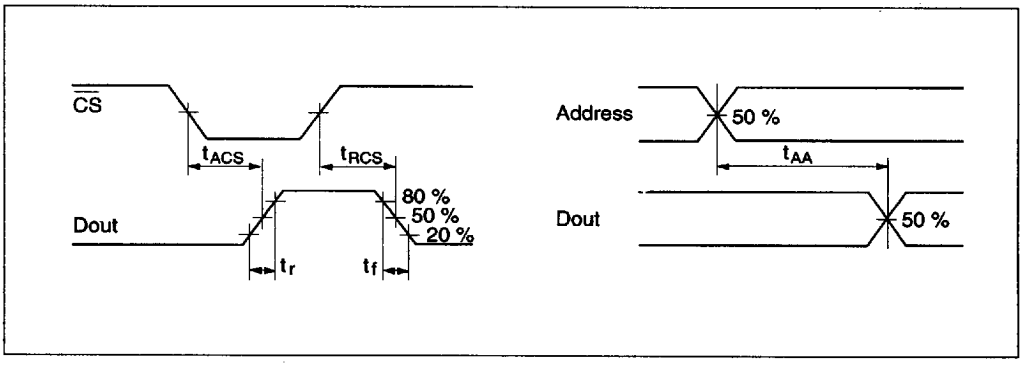
R_L = 50 Ω
C_L = 30 pF
(Includes probe and jig capacitance)

Input Pulse



$t_r = t_f$ = 2.0 ns typ

Read Mode



Write Mode