FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20913-2E

BURST MODE FLASH MEMORY

CMOS

32M (2M × 16) BIT

MBM29BS/BT32LF 18/25

■ GENERAL DESCRIPTION

The MBM29BS/BT32LF is a 32M bit, 1.8 Volt-only, Burst mode and dual operation Flash memory organized as 2M words of 16 bits each. The device offered in a 60-ball FBGA package. This device is designed to be programmed in-system with the standard system 1.8V V_{CC} supply.

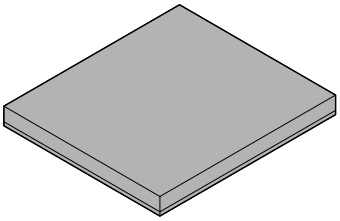
(Continued)

■ PRODUCT LINE UP

Part No.		MBM29BS/ BT32LF-25	MBM29BT32LF-18	MBM29BS32LF-18
V_{CC}		1.8 V $^{+0.15\ V}_{-0.15\ V}$	1.8 V $^{+0.15\ V}_{-0.15\ V}$	1.8 V $^{+0.15\ V}_{-0.15\ V}$
V_{CCQ}		1.8 V/3.0 V	3.0 V $^{+0.15\ V}_{-0.30\ V}$	1.8 V $^{+0.15\ V}_{-0.15\ V}$
Clock Rate		40 MHz (– 25)	54 MHz (– 18)	54 MHz (– 18)
Synchronous/Burst	Max Latency Time (ns)	120	106.5	106
	Max Burst Access Time (ns)	20	14	13.5
	Max $\overline{OE}$ Access Time (ns)	20	14	13.5
Asynchronous	Max Address Access Time (ns)	70	70	70
	Max $\overline{CE}$ Access Time (ns)	70	70	70
	Max $\overline{OE}$ Access Time (ns)	20.5	20	20

■ PACKAGE

60-ball plastic FBGA



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The device supports Enhanced V_{CCQ} to offer up to 3 V compatible inputs and outputs(MBM29BS32LF:1.8V V_{CCQ}, MBM29BT32LF:3.0V V_{CCQ}). 12.0V V_{PP} and 5.0V V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device provides truly high performance non-volatile memory solution. The device offers fast burst access frequency of 54MHz with initial access times of 106ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus connection the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), address valid ($\overline{AVD}$) and output enable ($\overline{OE}$) controls. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/ microcontrollers for high performance read operations. The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and wrap through the same memory space. At 54 MHz, the device provides a burst access of 13.5 ns with a latency of 106 ns at 30 pF.

The dual operation function provides simultaneous operation by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0V and 12.0V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each 32K words sector can be programmed and verified in about 0.3 second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 0.2 second. (If already preprogrammed.)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The Enhanced $V_{I/O}$ (V_{CCQ}) feature allows the output voltage generated on the device to be determined based on the $V_{I/O}$ level. This feature allows this device to operate in the 1.8 V and 3.0 V I/O environment, driving and receiving signals to and from other 1.8 V and 3.0 V devices on the same bus.

The device features single 1.8 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, output pin. Once the end of a program or erase cycle has been comleted, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

■ FEATURES

- **0.17 µm process technology**
- **Single 1.8 volt read, program and erase (1.65 V to 1.95 V)**
- **Simultaneous Read/Write operation (Dual Bank)**
- **All Sectors Being Protected Upon Power-up**
  The device aims for high-speed read of stored codes, thus to fully prevent it from much anticipated wrong operational procedures, programming and erasure, it adopts All-Sectors Lock for ultimate all sector protection by default upon power-up.
- **FlexBank™ *1**
  Bank A: 8M bit (8K words × 4 and 32K words × 15)
  Bank B: 8M bit (32K words × 16)
  Bank C: 8M bit (32K words × 16)
  Bank D: 8M bit (8K words × 4 and 32K words × 15)
- **Enhanced I/O™ *2 (V_{CCQ}) Feature**
  Input/ Output voltage generated on the device is determined based on the $V_{I/O}$ level
  (MBM29BS32LF: 1.8V V_{CCQ} and MBM29BT32LF: 3.0V V_{CCQ})
- **High Performance Burst frequency reach at 54MHz**
  Burst access times of 13.5 ns @ 30 pF at industrial temperature range
  Asynchronous random access times of 70 ns (at 30 pF)
  Synchronous latency of 106 ns with 1.8 V V_{CCQ}, and 106.5 ns with 3.0 V V_{CCQ} (at 30 pF)
- **Programmable Burst Read Interface**
  Linear Burst: 8, 16, and 32 words with wrap-around
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Minimum 100,000 program/erase cycles**
- **Sector Erase Architecture**
  Eight 8K words, sixty-two 32K words sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Write Protect Pin ($\overline{WP}$)**
  At V_{IL}, allows protection of "outermost" 2 × 8K words on low end of boot sectors(SA0 and SA1), regardless of sector protection/unprotection status
- **Accelerate Pin (ACC)**
  At V_{ACC}, increases program performance.
  At V_{IL}, hardware protect method to lock all sectors.
- **Embedded Erase™ *2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{Data}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Automatic sleep mode**
  When address remain stable, the device automatically switches itself to low power mode
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **In accordance with CFI (Common Flash Interface)**
- **Hardware reset pin ($\overline{RESET}$)**
  Hardware method to reset the device for reading array data
  To avoid initiation of a write cycle during Vcc power-up/down, $\overline{Reset}$ must be V_{IL} for defined time.

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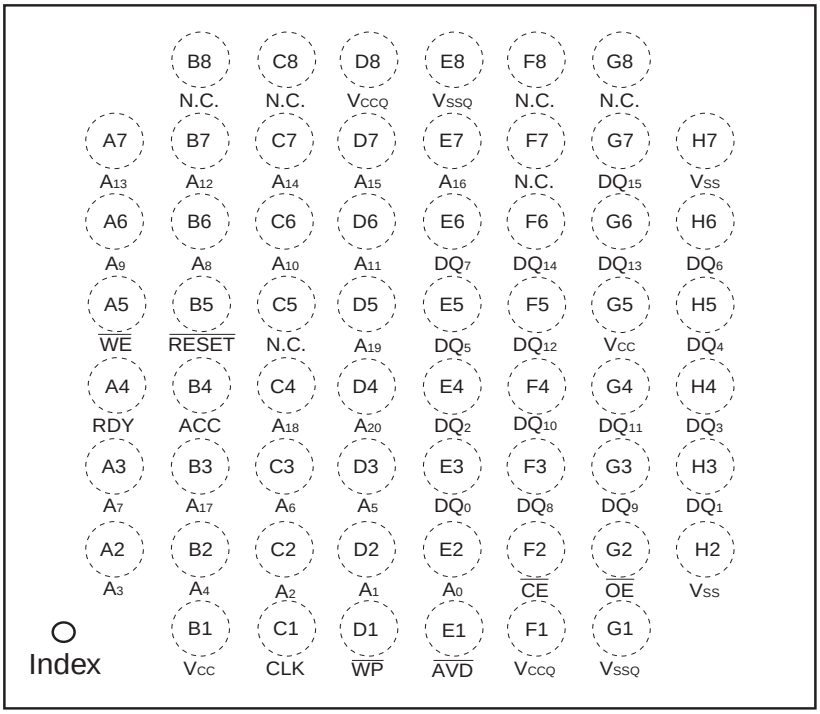
- **Protection**
  Software command sector locking
  WP protects the outermost two boot sectors(SA0 and SA1)
  ACC protects all sector at VIL. Should be at VIH for all other conditions.
- **CMOS compatible inputs, CMOS compatible outputs**

*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2: Embedded Erase™, Embedded Program™ and Enhanced $V_{I/O}$™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENT

FBGA
(TOP VIEW)
Marking Side

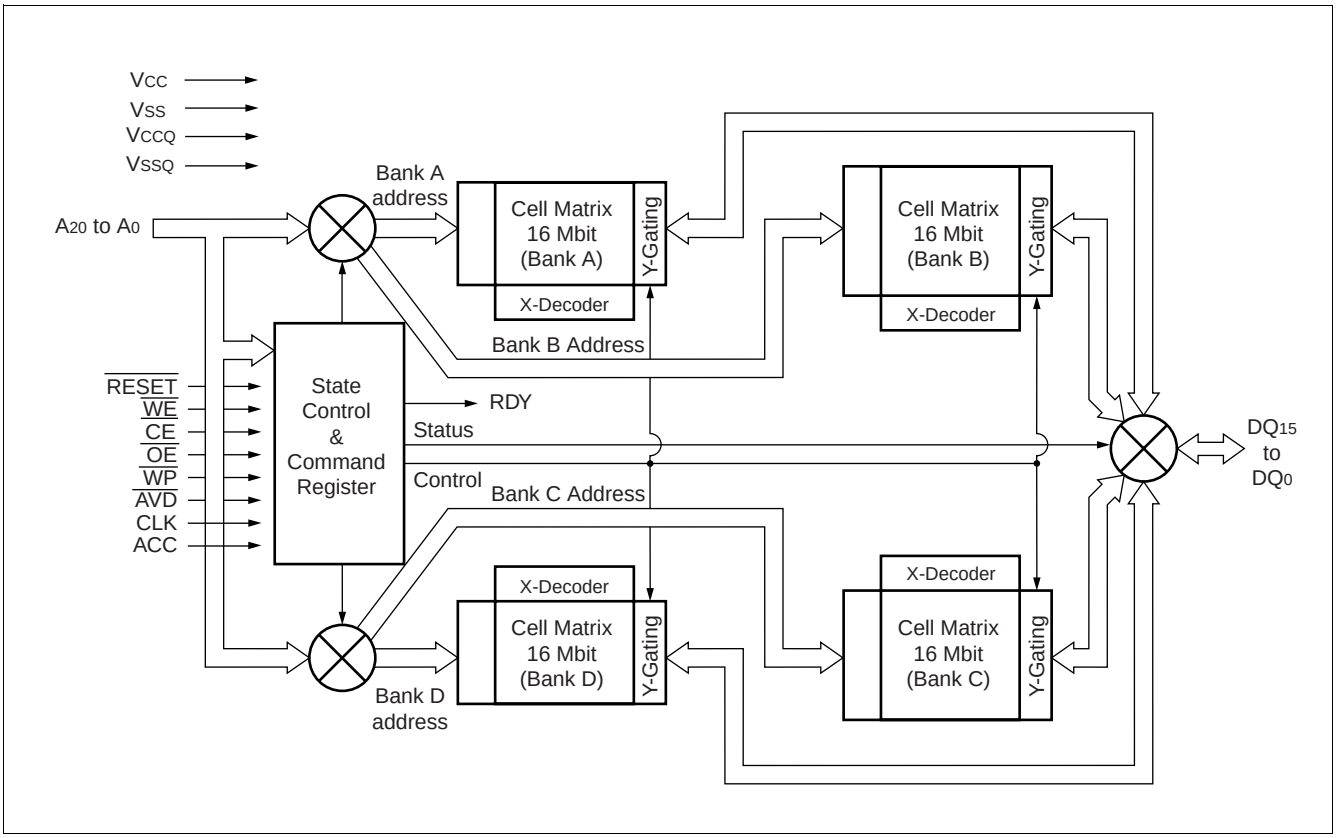


(BGA-60P-M05)

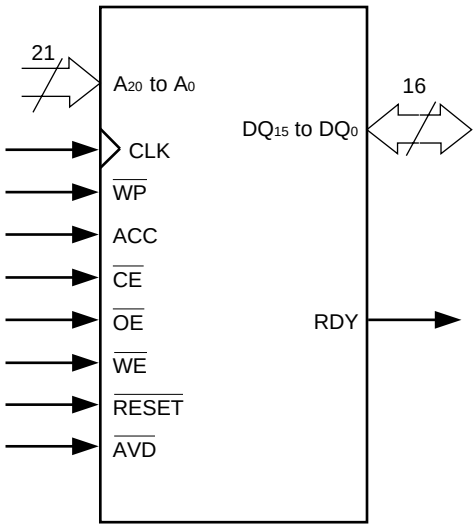
■ PIN DESCRIPTIONS

Pin	Function
A_{20} to A_0	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
CLK	CLK Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{AVD}$	Address Valid Input
RDY	Ready Output
$\overline{RESET}$	Hardware Reset
$\overline{WP}$	Hardware Write Protection
ACC	Program Acceleration
N.C.	Pin Not Connected Internally
V_{SS}	Device Ground
V_{CC}	Device Power Supply
V_{SSQ}	Input & Output Buffer Ground
V_{CCQ}	Input & Output Buffer Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATIONS

MBM29BS/BT32LF User Bus Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	DQ_{15} to DQ_0	CLK *1	$\overline{AVD}$	$\overline{RESET}$	$\overline{ACC}$
Auto-Select Manufacturer Code *2	L	L	H	X	L	H	L	L	L	L	L	L	Code	X	⌐↑	H	H
Auto-Select Device Code *2	L	L	H	X	H	L	L	L	L	L	L	L	Code	X	⌐↑	H	H
Extended Auto-Select Device Code *2	L	L	H	X	L	H	H	H	L	L	L	L	Code	X	⌐↑	H	H
	L	L	H	X	H	H	H	H	L	L	L	L	Code	X	⌐↑	H	H
Asynchronous Read - Addresses Latched *3	L	L	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{OUT}	X	⌐↑	H	H
Asynchronous Read - Addresses Steady State *3	L	L	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{OUT}	X	L	H	H
Load Starting Burst Address (CLK latch) *3	L	X	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	X	⌐↑	⌐⌐	H	H
Load Starting Burst Address ($\overline{AVD}$ latch) *3	L	X	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	X	H/L	⌐↑	H	H
Advance Burst to next address *3	L	L	H	X	X	X	X	X	X	X	X	X	D_{OUT}	⌐↑	H	H	H
Terminate Burst read	H	X	H	X	X	X	X	X	X	X	X	X	High-Z	⌐↑	X	H	H
Terminate Burst read and start new Burst read	L	X	H	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{OUT}	⌐↑	⌐⌐	H	H
Terminate Burst read via $\overline{RESET}$	X	X	H	X	X	X	X	X	X	X	X	X	High-Z	X	X	L	H
Standby	H	X	X	X	X	X	X	X	X	X	X	X	High-Z	X	X	H	H
Output Disable	L	H	H	X	X	X	X	X	X	X	X	X	High-Z	X	X	H	H
Program 1 - Addresses Latched ($\overline{WE}$) *4	L	H	L	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{IN}	L	L	H	H
Program 1 - Addresses Latched (CLK) *4	L	H	L	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{IN}	⌐↑	L	H	H
Program 2 - Addresses Latched (CLK) *4	L	H	L	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{IN}	⌐↑	⌐⌐	H	H
Program 2 - Addresses Latched ($\overline{AVD}$) *4	L	H	L	X	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_{IN}	H/L	⌐↑	H	H
Boot Block Sector Write Protection *5	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H	H
All Sector Lock	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L
$\overline{RESET}$	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	X	X	L	H

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⌐⌐ = Pulse input. See DC Characteristics for voltage levels.

*1: Default active edge of CLK is the rising edge.

*2: Autoselect code can be read both Asynchronous and Synchronous Read operation

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: For four program operations, enable to input the same program command.

*5: Protect “outermost” 2 × 8K words on low end of the boot block sectors.(SA0 and SA1)

MBM29BS/BT32LF Command Definitions Table

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Write Cycle		Third Write Cycle		Fourth Write Cycle		Fifth Write Cycle		Sixth Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Asynchronous Read / Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—
Asynchronous Read / Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0	PA	PD								
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	F0h*2	—	—	—	—	—	—	—	—
Sector Lock/Unlock (Sector Command Locking)	3	XXXh	60h	XXXh	60h	SLA	60h	—	—	—	—	—	—
Set Burst Mode Configuration Register	3	555h	AAh	2AAh	55h	(CR) 555h	C0h	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—

Legend:

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed. Address latches on the rising edge of $\overline{AVD}$ pulse or active CLK edge while $\overline{AVD}=V_{IL}$ or falling edge of write pulse while $\overline{AVD}=V_{IL}$

SA = Address of the sector to be erased. The combination of A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14} and A_{13} will uniquely select any sector.

BA = Bank Address. Address setted by A_{20}, A_{19} will select Bank A, Bank B, Bank C and Bank D.

SLA = Address of the sector to be locked. Set sector address (SA) and either A_6 = 1 for unlocked or A_6 = 0 for locked.

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data latches on the rising edge of write pulse.

CR = Configuration Register address bits A_{19} to A_{12}.

*1: This command is valid during Fast Mode.

*2: The data "00h" is also acceptable.

Notes:
- Address bits A_{20} to A_{11} = X = "H" or "L" for all address commands except for PA, SA, BA.
- Bus operations are defined in "MBM29BS/BT32LF User Bus Operations Table" (in ■DEVICE BUS OPERATIONS).
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

MBM29BS/BT32LF Sector Protection Verify Autoselect Codes Table

Type	A_{20}, A_{19}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA*2	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	BA*2	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Extended Device Code*1	BA	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2223h*2
										2234h*2
	BA	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	2200h
Sector lock/ unlock	Sector Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	01h*3

*1: A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA)0Eh, as well as at (BA)0Fh.

*2: 2223h for V_{CCQ}: 1.8 V(MBM29BS32LF), 2234h for V_{CCQ}: 3.0 V(MBM29BT32LF).

*3: Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

Expanded Autoselect Code Table

Type	Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code	04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	227Eh	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	0
Extended Device Code	2223h	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1
	2234h	0	0	1	0	0	0	1	0	0	0	1	1	0	1	0	0
	2200h	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Sector Lock/ Unlock	00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	01h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

■ FLEXIBLE SECTOR ERASE ARCHITECTURE

Sector Address Table (Bank A, B)

Bank	Sector	Sector Address								Sector Size (Kwords)	Address Range
		Bank Address		A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}		
		A_{20}	A_{19}								
Bank A	SA0	0	0	0	0	0	0	0	0	8	000000h to 001FFFh
	SA1	0	0	0	0	0	0	0	1	8	002000h to 003FFFh
	SA2	0	0	0	0	0	0	1	0	8	004000h to 005FFFh
	SA3	0	0	0	0	0	0	1	1	8	006000h to 007FFFh
	SA4	0	0	0	0	0	1	X	X	32	008000h to 00FFFFh
	SA5	0	0	0	0	1	0	X	X	32	010000h to 017FFFh
	SA6	0	0	0	0	1	1	X	X	32	018000h to 01FFFFh
	SA7	0	0	0	1	0	0	X	X	32	020000h to 027FFFh
	SA8	0	0	0	1	0	1	X	X	32	028000h to 02FFFFh
	SA9	0	0	0	1	1	0	X	X	32	030000h to 037FFFh
	SA10	0	0	0	1	1	1	X	X	32	038000h to 03FFFFh
	SA11	0	0	1	0	0	0	X	X	32	040000h to 047FFFh
	SA12	0	0	1	0	0	1	X	X	32	048000h to 04FFFFh
	SA13	0	0	1	0	1	0	X	X	32	050000h to 057FFFh
	SA14	0	0	1	0	1	1	X	X	32	058000h to 05FFFFh
	SA15	0	0	1	1	0	0	X	X	32	060000h to 067FFFh
	SA16	0	0	1	1	0	1	X	X	32	068000h to 06FFFFh
	SA17	0	0	1	1	1	0	X	X	32	070000h to 077FFFh
	SA18	0	0	1	1	1	1	X	X	32	078000h to 07FFFFh
Bank B	SA19	0	1	0	0	0	0	X	X	32	080000h to 087FFFh
	SA20	0	1	0	0	0	1	X	X	32	088000h to 08FFFFh
	SA21	0	1	0	0	1	0	X	X	32	090000h to 097FFFh
	SA22	0	1	0	0	1	1	X	X	32	098000h to 09FFFFh
	SA23	0	1	0	1	0	0	X	X	32	0A0000h to 0A7FFFh
	SA24	0	1	0	1	0	1	X	X	32	0A8000h to 0AFFFFh
	SA25	0	1	0	1	1	0	X	X	32	0B0000h to 0B7FFFh
	SA26	0	1	0	1	1	1	X	X	32	0B8000h to 0BFFFFh
	SA27	0	1	1	0	0	0	X	X	32	0C0000h to 0C7FFFh
	SA28	0	1	1	0	0	1	X	X	32	0C8000h to 0CFFFFh
	SA29	0	1	1	0	1	0	X	X	32	0D0000h to 0D7FFFh
	SA30	0	1	1	0	1	1	X	X	32	0D8000h to 0DFFFFh
	SA31	0	1	1	1	0	0	X	X	32	0E0000h to 0E7FFFh
	SA32	0	1	1	1	0	1	X	X	32	0E8000h to 0EFFFFh
	SA33	0	1	1	1	1	0	X	X	32	0F0000h to 0F7FFFh
	SA34	0	1	1	1	1	1	X	X	32	0F8000h to 0FFFFFh

Sector Address Table (Bank C, D)

Bank	Sector	Sector Address								Sector Size (Kwords)	Address Range
		Bank Address		A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}		
		A_{20}	A_{19}								
Bank C	SA35	1	0	0	0	0	0	X	X	32	100000h to 107FFFh
	SA36	1	0	0	0	0	1	X	X	32	108000h to 10FFFFh
	SA37	1	0	0	0	1	0	X	X	32	110000h to 117FFFh
	SA38	1	0	0	0	1	1	X	X	32	118000h to 11FFFFh
	SA39	1	0	0	1	0	0	X	X	32	120000h to 127FFFh
	SA40	1	0	0	1	0	1	X	X	32	128000h to 12FFFFh
	SA41	1	0	0	1	1	0	X	X	32	130000h to 137FFFh
	SA42	1	0	0	1	1	1	X	X	32	138000h to 13FFFFh
	SA43	1	0	1	0	0	0	X	X	32	140000h to 147FFFh
	SA44	1	0	1	0	0	1	X	X	32	148000h to 14FFFFh
	SA45	1	0	1	0	1	0	X	X	32	150000h to 157FFFh
	SA46	1	0	1	0	1	1	X	X	32	158000h to 15FFFFh
	SA47	1	0	1	1	0	0	X	X	32	160000h to 167FFFh
	SA48	1	0	1	1	0	1	X	X	32	168000h to 16FFFFh
	SA49	1	0	1	1	1	0	X	X	32	170000h to 177FFFh
	SA50	1	0	1	1	1	1	X	X	32	178000h to 17FFFFh
Bank D	SA51	1	1	0	0	0	0	X	X	32	180000h to 187FFFh
	SA52	1	1	0	0	0	1	X	X	32	188000h to 18FFFFh
	SA53	1	1	0	0	1	0	X	X	32	190000h to 197FFFh
	SA54	1	1	0	0	1	1	X	X	32	198000h to 19FFFFh
	SA55	1	1	0	1	0	0	X	X	32	1A0000h to 1A7FFFh
	SA56	1	1	0	1	0	1	X	X	32	1A8000h to 1AFFFFh
	SA57	1	1	0	1	1	0	X	X	32	1B0000h to 1B7FFFh
	SA58	1	1	0	1	1	1	X	X	32	1B8000h to 1BFFFFh
	SA59	1	1	1	0	0	0	X	X	32	1C0000h to 1C7FFFh
	SA60	1	1	1	0	0	1	X	X	32	1C8000h to 1CFFFFh
	SA61	1	1	1	0	1	0	X	X	32	1D0000h to 1D7FFFh
	SA62	1	1	1	0	1	1	X	X	32	1D8000h to 1DFFFFh
	SA63	1	1	1	1	0	0	X	X	32	1E0000h to 1E7FFFh
	SA64	1	1	1	1	0	1	X	X	32	1E8000h to 1EFFFFh
	SA65	1	1	1	1	1	0	X	X	32	1F0000h to 1F7FFFh
	SA66	1	1	1	1	1	1	0	0	8	1F8000h to 1F9FFFh
	SA67	1	1	1	1	1	1	0	1	8	1FA000h to 1FBFFFh
	SA68	1	1	1	1	1	1	1	0	8	1FC000h to 1FDFFFh
	SA69	1	1	1	1	1	1	1	1	8	1FE000h to 1FFFFFh

Common Flash Memory Interface Code Table (CFI)

Description	A_6 to A_0	DQ_{15} to DQ_0
Query-unique ASCII string “QRY”	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min (write/erase) DQ_7 to DQ_4 : 1 V/bit, DQ_3 to DQ_0 : 100 mV/bit	1Bh	0017h
V_{CC} Max (write/erase) DQ_7 to DQ_4 : 1 V/bit, DQ_3 to DQ_0 : 100 mV/bit	1Ch	0019h
V_{PP} Min voltage	1Dh	0000h
V_{PP} Max voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	0009h
Typical timeout for full chip erase 2^N ms	22h	0000h
Max timeout for byte/word write 2^N times typical	23h	0004h
Max timeout for buffer write 2^N times typical	24h	0000h
Max timeout per individual block erase 2^N times typical	25h	0004h
Max timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0016h
Flash Device Interface description	28h 29h	0001h 0000h
Max number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0003h
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0003h 0000h 0040h 0000h
Erase Block Region 2 Information	31h 32h 33h 34h	003Dh 0000h 0000h 0001h
Erase Block Region 3 Information	35h 36h 37h 38h	0003h 0000h 0040h 0000h

(Continued)

(Continued)

Description	A_6 to A_0	DQ_{15} to DQ_0
Erase Block Region 4 Information	39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h
Query-unique ASCII string “PRI”	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0033h
Address Sensitive Unlock 0h = Required 1h = Not Required	45h	0004h
Erase Suspend 0h = Not Supported 1h = To Read Only 2h = To Read & Write	46h	0002h
Sector Protection 0h = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotection 00h = Not Supported 01h = Supported	48h	0000h
Sector Protection Algorithm	49h	0005h
Simultaneous Operation 00h = Not Supported, X = Total number of sectors in all Banks except Bank A	4Ah	0033h
Burst Mode Type 00h = Not Supported	4Bh	0001h
Page Mode Type 00h = Not Supported	4Ch	0000h
ACC (Acceleration) Supply Minimum 00h = Not Supported, DQ_7 to DQ_4 : 1 V/bit, DQ_3 to DQ_0 : 100 mV/bit	4Dh	00B5h
ACC (Acceleration) Supply Maximum 00h = Not Supported, DQ_7 to DQ_4 : 1 V/bit, DQ_3 to DQ_0 : 100 mV/bit	4Eh	00C5h
Boot Type 02h = Bottom Boot 03h = Top Boot	4Fh	0002h
Program Suspend 00h = Not Supported, 01h = Supported	50h	0000h
Bank Organization	57h	0004h
Bank A Region Information	58h	0013h
Bank B Region Information	59h	0010h
Bank C Region Information	5Ah	0010h
Bank D Region Information	5Bh	0013h

■ FUNCTIONAL DESCRIPTION

Asynchronous Read Operation (Non-Burst) Mode

When the device first powers up, it is enabled for asynchronous read operation. CLK is ignored in this operation.

To read data from the memory array, the system must first assert a valid address on A_{20} to A_0, while driving $\overline{AVD}$ and $\overline{CE}$ to V_{IL}. $\overline{WE}$ should remain at V_{IH}. The rising edge of $\overline{AVD}$ latches the address or while $\overline{AVD}$=V_{IL}, address is latched by address change timing. The data will appear on DQ_{15} to DQ_0. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable $\overline{CE}$ to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. During power transition, $\overline{RESET}$ must be held low(Refer to "Power On/Off Timing Diagram").This ensures that no spurious alteration of the memory content occurs during the power transition.

Synchronous (Burst) Read Operation Mode

The device is capable of continuous sequential burst operation and linear burst operation of a preset length.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, which edge of the clock will be the active clock edge, and how the RDY signal will transition with valid data. The system would then write the configuration register set command sequence. See "Configuration Register Set Command" and "Command Definitions" for further details.

Once the system has written the "Configuration Register Set" command sequence, the device Read mode is enabled for synchronous reads only. However Program operation is independent of the Configuration Register status.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle, which automatically increments the internal address counter.

The device will continue to output sequential burst data, wrapping around to address after it reaches the highest addressable memory location in group address range, until the system drives $\overline{CE}$ to V_{IH}, $\overline{RESET}$ to V_{IL}, or $\overline{AVD}$ to V_{IL} in conjunction with a new address. See “MBM29BS/BT32LF User Bus Operations Table” in ■DEVICE BUS OPERATIONS.

If the clock frequency is less than 6 MHz during a burst mode operation, additional latencies will occur. RDY indicates the length of the latency by pulsing low.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see “MBM29BS/BT32LF User Bus Operations Table” in ■DEVICE BUS OPERATIONS).

As an example: if the starting address in the 8-word with wrap-around mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h-etc. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group.

In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group.

The RDY pin indicates when data is valid on the bus in both asnchronous and synchronous read mode. The devices can wrap through a maximum of 128 words of data (8 words up to 16 times, 16 words up to 8 times, or 32 words up to 4 times) before requiring a new synchronous access (latching of a new address).

Burst Address Groups Table

Mode	Group Size	Group Address Ranges
8-word with wrap-around	8 words	0-7h, 8-Fh, 10-17h, ...
16-word with wrap-around	16 words	0-Fh, 10-1Fh, 20-2Fh, ...
32-word with wrap-around	32 words	00-1Fh, 20-3Fh, 40-5Fh, ...

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active.

Simultaneous Operation

The device features functions that enable reading of data from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation) , in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank can be selected by bank address (A_{20}, A_{19})with zero latency. The device consists of the following four banks :

Bank A : 4 X 8K word and 15 X 32K word; Bank B : 16 X 32K word; Bank C : 16 X 32K word; Bank D : 4 X 8K word and 15 X 32K word. The device can execute simultaneous operations between Bank 1, a bank chosen from among the four banks, and Bank 2, a bank consisting of the three remaining banks. (See “FlexBank™ Architecture Table”.) This is what we call a “FlexBank”, for example, the rest of banks B, C and D to let the system read while Bank A is in the process of program (or erase) operation. However, the different types of operations for the three banks are impossible, e.g. Bank A writing, Bank B erasing, and Bank C reading out. With this “FlexBank”, as described in “Example of Virtual Banks Combination Table”, the system gets to select from four combinations of data volume for Bank 1 and Bank 2, which works well to meet the system requirement. The simultaneous operation cannot execute multi-function mode in the same bank. “Simultaneous Operation Table” shows the possible combinations for simultaneous operation. (Refer to “(20) Bank-to-Bank Read/Write Cycle Timings” in ■TIMING DIAGRAMS.)

FlexBank™ Architecture Table

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	8M bit	Bank A	24M bit	Remainder (Bank B, C, D)
2	16M bit	Bank A, B	16M bit	Remainder (Bank C, D)

Example of Virtual Banks Combination Table

Bank Splits	Bank 1			Bank 2		
	Megabits	Combination of Memory Bank	Sector Sizes	Megabits	Combination of Memory Bank	Sector Sizes
1	8M bit	Bank A	Four 8K word, fifteen 32K word	24M bit	Bank B + Bank C + Bank D	Four 8K word, forty-seven 32K word
2	16M bit	Bank A + Bank D	Eight 8K word, thirty 32K word	16M bit	Bank B + Bank C	thirty-two 32K word

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Simultaneous Operation Table

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode	Read mode

Note : Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C and Bank D. Bank Address (BA) meant to specify each of the Banks.

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins, and the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ input held at V_{CC}±0.2 V. Under this condition the current consumed is less than 5µA Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even if $\overline{CE}$="H". The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS}±0.3 V ($\overline{CE}$="H" or "L") . Under this condition the current consumed is less than 5µA Max. Once the $\overline{RESET}$ pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state, regardless of $\overline{OE}$ input.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of the device data. This mode can be useful in the application such as a handy terminal which requires low power consumption.

While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} +60 ns. While in synchronous mode, the device automatically enables this mode when either the first active CLK level is greater than t_{ACC} or the CLK runs slower than 5 MHz. A new burst operations is required to provid new data. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on this mode. Under the mode, the current consumed is typically 0.2 µA (CMOS Level)(I_{CC5}).

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device reads the data for changed addresses.

Output Disable

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

Autoselect Mode

The Autoselect mode allows the reading out of a binary code and identifies its manufacturer and type.It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device. Autoselect may only be entered and used when in the asynchronous mode.

The manufacturer and device codes can be read via the command register, Three identifier bytes may then be sequenced from the device outputs by toggling addresses. All addresses are DON'T CARES except A_7 to A_0. (See "MBM29BS/BT32LF User Bus Operations Table" in ■DEVICE BUS OPERATIONS.)

The command sequence is illustrated in "MBM29BS/BT32LF Command Definitions Table" (in ■DEVICE BUS OPERATIONS). (Refer to Autoselect Command section.)

In the command Autoselect mode, the bank addresses BA; (A_{20}, A_{19})must point to a specific bank during the third write bus cycle of the Autoselect command. Then the Autoselect data will be read from that bank while array data can be read from the other bank.

A read cycle from address 00h returns the manufacturer's code (Fujitsu=04h) . A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. (Refer to "MBM29BS/BT32LF Sector Protection Verify Autoselect Codes Table" and "Expanded Autoselect Code Table" in ■DEVICE BUS OPERATIONS.)

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine output dictates the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command.

The device has the capability of performing programming operations. It has inputs/outputs that accept both address and data information. During a program operation($\overline{AVD}$ latched address)(Program2), the command register is written by bringing active CLK edge while $\overline{AVD}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH} when providing an address to the device, addresses are latched on the CLK active edge or $\overline{AVD}$ rising edge(when CLK active edge doesn't appear while AVD=V_{IL}) and drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}, data is latched on the rising edge of $\overline{WE}$. During a program operation($\overline{WE}$ latched address)(Program1), the command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever

happens later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$(whichever happensfirst). Standard microprocessor write timings are used. The programming operations are independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

$\overline{RESET}$ (Hardware Reset)

The $\overline{RESET}$ input provides a hardware method of re-setting the device to reading array data. When $\overline{RESET}$ is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current (I_{CC4}). If $\overline{RESET}$ is held at V_{IL} but not within $V_{SS} \pm 0.2$ V, the standby current will be greater.

$\overline{RESET}$ may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If $\overline{RESET}$ is asserted during a program or erase operation, the device requires a time of t_{READY} (during Embedded Algorithms) before the device is ready to read data again. If $\overline{RESET}$ is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after $\overline{RESET}$ returns to V_{IH}.

Refer to the AC Characteristics tables for $\overline{RESET}$ parameters.

Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. Note that sectors must be unlocked by sector unlock command sequence(xxxh/60h, xxxh/60h, SLA/60h), prior to raising ACC to V_{ACC}.

When at V_{IL}, ACC locks all sectors. Should be at V_{IH} for all other conditions.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the pressent sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the ACC pin returns the device to normal operation. Do not remove V_{ACC} from ACC pin while programming. See “(15) Accelerated Fast mode Programming Timing” in ■TIMING DIAGRAMS.

<Protection>

The MBM29BS/BT32LF features several levels of sector protection, which can disable both the program and erase operations

(1) Write Protect ($\overline{WP}$) [Hardware Protection]

The device features a hardware protection option using a write protect pin that prevents programming or erasing. The $\overline{WP}$ pin is associated with the “outermost” 2×8K words on low end of boot sectors. The $\overline{WP}$ pin has no effect on any other sector. When $\overline{WP}$ is taken to V_{IL}, programming and erase operations of the “outermost” 2×8K words sectors are disabled. By taking $\overline{WP}$ back to V_{IH}, the “outermost” 2×8K words sectors are enabled for program and erase operations, The user must hold the $\overline{WP}$ pin at either V_{IH} or V_{IL} during the entire program or erase operation of the “outermost” two sectors on low end of boot sectors(SA0 and SA1).

(2) ACC Protect (ACC) [Hardware Protection2]

The device has also hardware protect feature by ACC pin. When ACC is V_{IL}, all sectors are locked. Should be at V_{IH} for all other condition

(3) Software Command Locking(SCL) [Software Protection]

The sector lock/unlock feature allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command.

Enhanced I/O (V_{CCQ}) Control

The Enhanced I/O (V_{CCQ}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin. This allows the device to operate in 1.8 V and 3 V system environments as required.

For example, a V_{CCQ} of 2.70 V to 3.15 V allows for I/O at the 3-volt level, driving and receiving signals to and from other 3 V devices on the same bus.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Some commands require Bank Address (BA) input. When command sequences are input into a bank reading, the commands have priority over the reading. “MBM29BS/BT32LF Command Definitions Table” in ■DEVICE BUS OPERATIONS shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover, Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Asynchronous Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, verify mode of secter protect commands the Reset operation is initiated by writing the Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Asynchronous Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. While $\overline{AVD}$ = V_{IL}, asynchronous read operation is same as conventional Fujitsu Flash memory. Addresses are latched by the rising edge of $\overline{AVD}$ or address change timing. t_{ACC} defined from address change timing or $\overline{AVD}$ falling edge, because addresses are input to internal circuit while $\overline{AVD}$ = V_{IL}. If the device is used by $\overline{AVD}$ ratch asynchronous read operation, addresses should be kept from $\overline{AVD}$ falling edge to $\overline{AVD}$ rising edge or t_{ACC} defined by address change timing, not $\overline{AVD}$ falling edge. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Synchronous (Burst) Read Command

This operation is enable after configuratrion register command is issued (A_{19} = 0). Addresses are latched by the $\overline{AVD}$ rising edge or CLK active edge while $\overline{AVD}$ = V_{IL}.

Configuration Register Set Command

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode(burst length), active clock edge, RDY configuration, and synchronous Read mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a three-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C0h, address bits A_{11} to A_0 should be 555h, address bits A_{19} to A_{12} set the code to be latched, and address bit A_{20} is Don’t care. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. Address A_{19} determines this setting: "1’ for asynchronous mode, "0" for synchronous mode.

Programmable Wait State Configuration Setting

The programmable wait state feature informs the device of the number of clock cycles that must elapse after $\overline{AVD}$ is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A_{14} to A_{12} determine the setting (see “Third Cycle Address/Data Table”).The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Third Cycle Address/Data Table

A_{14}	A_{13}	A_{12}	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. “Wait State Table” describes the typical number of clock cycles (wait states) for conditions.The host system must set the appropriate number of wait states in the flash device depending on the clock frequency and the presence of a boundary crossing.

Wait State Table

Conditions at Address	Typical No. of Clock Cycles after $\overline{AVD}$ Low	
	40 MHz	54 MHz
Wait state for initial access	5	6

Burst Read Mode Configuration Setting(Burst Length)

The device supports three different burst read modes: 8, 16, and 32 word linear wrap around modes. A continuous sequence begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear burst with wrap around begins on the starting burst address written to the device and then advances to the next 8-word boundary. The address pointer then returns to the 1st word after the previous eight-word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

“Burst Read Mode Settings Table” shows the address bits and settings for the three burst read modes.

Burst Read Mode Settings Table

Burst Modes	Address Bits	
	A_{16}	A_{15}
8-word linear wrap around	0	1
16-word linear wrap around	1	0
32-word linear wrap around	1	1

Active Clock Edge Configuration Setting

By default, the device will deliver data on the rising edge of the clock after the initial synchronous access time. Subsequent outputs will also be on the following rising edges, barring any delays. The device can be set so that the falling clock edge is active for all synchronous accesses. Address bit A_{17} determines this setting; "1" for rising active, "0" for falling active.

RDY Configuration Setting

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. Address bit A_{18} determines this setting; "1" for RDY active with data, "0" for RDY active one clock cycle before valid data. “Hardware Sequence Flags Table” shows the address bits that determine the configuration register settings for various device functions.

Configuration Register Table

Address BIt	Function	Settings (Binary)
A_{19}	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
A_{18}	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data
A_{17}	Clock	0 = Burst starts and data is output on the falling edge of CLK 1 = Burst starts and data is output on the rising edge of CLK
A_{16}	Burst Read Mode	00 = Reserved 01 = 8-word linear with wrap around 10 = 16-word linear with wrap around 11 = 32-word linear with wrap around
A_{15}		
A_{14}	Programmable Wait State	000 = Data is valid on the 2th active CLK edge after $\overline{AVD}$ transition to V_{IH} 001 = Data is valid on the 3th active CLK edge after $\overline{AVD}$ transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after $\overline{AVD}$ transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after $\overline{AVD}$ transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after $\overline{AVD}$ transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after $\overline{AVD}$ transition to V_{IH} 110 = Reserved 111 = Reserved
A_{13}		
A_{12}		

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a higher voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data from the memory cell can be read from another bank. The higher order address (A_{20}, A_{19}) required for reading out the manufacture and device codes demands the bank address (BA) set at the third write cycle.

Following the command write, a read cycle from address (BA)00h returns the manufacturer’s code (Fujitsu=04h). And a read cycle at address (BA)01h outputs device code. When 227Eh was output, this indicates that two

additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh. (Refer to “MBM29BS/BT32LF Sector Protection Verify Autoselect Codes Table” and “Expanded Autoselect Code Table” in ■DEVICE BUS OPERATIONS.)

The sector state will be informed by address (SA)02h. Scanning the sector addresses (A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) while(A_7,A_6, A_5, A_4, A_3, A_2, A_1,A_0) = (0, 0, 0, 0, 0, 0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector group. The programming verification should be performed by verifying sector group protection on the protected sector. (See “MBM29BS/BT32LF User Bus Operations Table” in ■DEVICE BUS OPERATIONS.)

The manufacture and device codes can be read from the selected bank. To read the manufacture and device codes and sector protection status from a non-selected bank, it is necessary to write the Read/Reset command sequence into the register. Autoselect command should then be written into the bank to be read.

If the software (program code) for Autoselect command is stored in the Flash memory, the device and manufacture codes should be read from the other bank, which does not contain the software. No subsequent data will be made available if the autoselect data is read in synchronous mode.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, Read/Reset command sequence must be written before the Autoselect command.

Word Programming Command

The device is programmed on word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. During a programming operation($\overline{AVD}$ latched address)(Program2), the command register is written by bringing active CLK edge while $\overline{AVD}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH} when providing an address to the device, addresses are latched on the CLK active edge or $\overline{AVD}$ rising edge(when CLK active edge doesn’t appear while AVD=V_{IL}). and drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}, data is latched on the rising edge of $\overline{WE}$. During a programming operation($\overline{WE}$ latched address)(Program1), the command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$(whichever happens first). Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit). The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see “Hardware Sequence Flags Table”). Therefore, the device requires that a valid address to the device be supplied by the system in this particular instance. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert from “0”s to “1”s.

“(2) Embedded Program™ Algorithm” in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase Command

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit). The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

"(3) Embedded Erase™ Algorithm" in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of "t_{TOW}" from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on "MBM29BS/BT32LF Command Definitions Table" (in ■DEVICE BUS OPERATIONS). This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of "t_{TOW}" from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the "t_{TOW}" time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit).

The sector erase begins after the "t_{TOW}" time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase.

In case of multiple sector erase across bank boundaries, a read from the bank (read-while-erase) to which sectors being erased belong cannot be performed.

"(3) Embedded Erase™ Algorithm" in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume Command

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The addresses are "DON'T CARES" when writting the Erase Suspend or Erase Resume command.When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the $\overline{\text{Data}}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Sector Lock/Unlock Command(Software Command Locking(SCL))

The sector lock/unlock command sequence allows the system to determine which sectors are protected from accidental writes. When the device is first powered up, all sectors are locked. To unlock a sector, the system must write the sector lock/unlock command sequence. Two cycles are first written: addresses are don't care and data is 60h. During the third cycle, the sector address (SLA) and unlock command (60h) is written, while specifying with address A_6 whether that sector should be locked ($A_6 = V_{IL}$) or unlocked ($A_6 = V_{IH}$). After the third cycle, the system can continue to lock or unlock additional cycles, or exit the sequence by writing F0h (reset command).

Note that the last two outermost boot sectors can be locked by taking the $\overline{\text{WP}}$ signal to V_{IL}.

Extended Command

(1) Fast Mode

The device has Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to "(6) Embedded Programming Algorithm for Fast Mode" in ■FLOW CHART.) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). (Refer to "(6) Embedded Programming Algorithm for Fast Mode" in ■FLOW CHART.)

(3) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of device. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrives device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is "0" in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the Read/Reset command sequence into the register.

WRITE OPERATION STATUS

Detailed in "Hardware Sequence Flags Table" are all the status flags which can determine the status of the bank for the current mode operation. The read operation from the bank which doesn't operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether an Embedded Algorithm is properly completed. The information on DQ_2 is address-sensitive. This means that if an address from an erasing sector is consecutively read, the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

The status flag is not output from banks (non-busy banks) which do not execute Embedded Algorithms.
For example, a bank (busy bank) is executing an Embedded Algorithm. When the read sequence is [1] < busy bank >, [2] < non-busy bank >, [3] < busy bank >, the DQ_6 toggles in the case of [1] and [3]. In case of [2], the data of memory cells are output. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in [1] and [3].

Hardware Sequence Flags Table

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	No toggle *3
	Embedded Erase Algorithm	Erase Sector	0	Toggle	0	1	Toggle *1
		Non-Erase Sector					No toggle *3
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No toggle *3	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1 *2,*3
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	No toggle *3
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2: Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

*3: When the device is set to Asynchronus mode, these status flags should be read by CE toggle.

Notes: • DQ_0 and DQ_1 are reserve pins for future use.
• DQ_4 is limited to Fujitsu internal use.

DQ_7

$\overline{Data}$ Polling

The device features $\overline{Data}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” on DQ_7. The flowchart for $\overline{Data}$ Polling (DQ_7) is shown in “(4) $\overline{Data}$ Polling Algorithm” (in ■FLOW CHART).

For programming, the $\overline{Data}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences.

For chip erase and sector erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequences. $\overline{Data}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise the status may become invalid.

If a program address falls within a protected sector, $\overline{Data}$ Polling on DQ_7 is active for approximately 1 μs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{Data}$ Polling on DQ_7 is active for approximately 400 μs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that device is driving status information

on DQ_7 at one instant, and then that byte's valid data at the next instant. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ_7 has a valid data, data outputs on DQ_0 to DQ_6 may still be invalid. The valid data on DQ_0 to DQ_7 will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See "Toggle Bit Status Table".)

See "(14) Chip/Sector Erase Command Sequence", "(16) $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithm)" in ■TIMING DIAGRAMS for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the busy bank will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, the device will erase all selected sectors except for protected ones. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data kept remained.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

The system can use DQ_6 to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress) , DQ_6 toggles. When a bank enters the Erase Suspend mode, DQ_6 stops toggling. Successive read cycles during erase-suspend-program cause DQ_6 to toggle.

To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

See "(15) Accelerated Fast mode Programming Timing", "(16) $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithm)" in ■TIMING DIAGRAMS for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ_5 will produce "1". This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down device under these conditions (to approximately 2 mA) . The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in "MBM29BS/BT32LF User Bus Operations Table" in ■DEVICE BUS OPERATIONS.

The DQ_5 failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ_7 bit and DQ_6 never stop toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset device with the command sequence.

DQ_3

Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out begins. DQ_3 will remain low until the time-out is completed. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit I indicates that a valid erase command has been written, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun. If DQ_3 is low ("0") , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags Table"

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also "Toggle Bit Status Table".

Furthermore DQ_2 can also be used to determine which sector is being erased. At the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5) . If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to "(5) Toggle Bit Algorithm" in ■FLOW CHART.)

Toggle Bit Status Table

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle *
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1 *

*: Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

RDY: Ready

The RDY is a dedicated output that, by default, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

RDY functions only while reading data in burst mode. The following condition causes the RDY output to be low: during the initial access (in burst mode).

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state machine to Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequence.

Device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All inputs and I/Os pins except as noted below *1	V_{IN}, V_{OUT}	–0.5	V_{CCQ}+0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+2.5	V
I/O's Power Supply Voltage	V_{CCQ}	–0.5	+3.5	V
ACC *2	V_{ACC}	–0.5	+10.5	V

*1: Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may underrshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on ACC pin is –0.5 V. During voltage transitions, ACC pin may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on ACC pin is +10.5 V which may overshoot to +12.5 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} - V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T_A	MBM29BS/BT32LF 18/25	–40	+85	°C
Power Supply Voltage	V_{CC}	MBM29BS/BT32LF 18/25	+1.65	+1.95	V
V_{CCQ} Supply Voltage	V_{CCQ}	MBM29BS32LF 18/25	+1.65	Vcc	V
		MBM29BT32LF 18/25	+2.70	+3.15	V

Note: Operating ranges define those limits between which the functionality of the device is quaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT

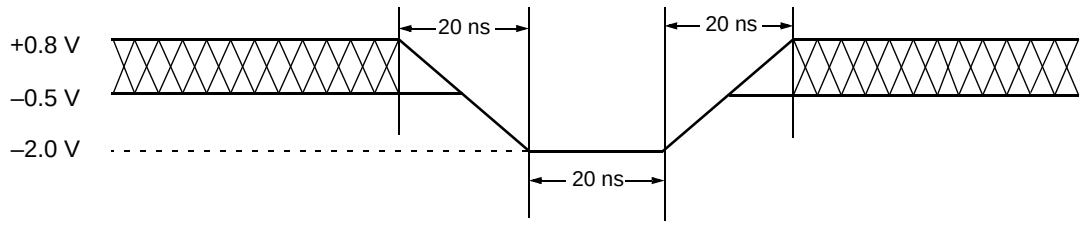


Figure 1 Maximum Undershoot Waveform

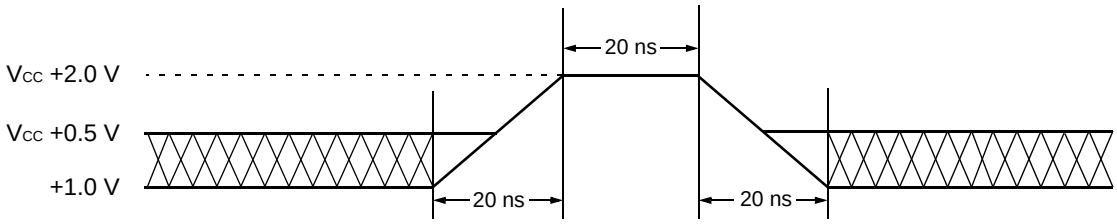


Figure 2 Maximum Overshoot Waveform 1

■ DC CHARACTERISTICS

Parameter Description	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to Vcc, V_{CC} = Vcc Max		—	—	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to Vcc, V_{CC} = Vcc Max		—	—	±1.0	µA
V_{CC} Active Burst Read Current	I_{CCB}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{WE}$ =V_{IH} (54MHz)		—	—	25	mA
V_{CC} Active Asynchronous Read Current*1	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IH}	5 MHz	—	8	12	mA
			1 MHz		3.3	5	
V_{CC} Active Current*2	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{PP} = V_{IH}		—	15	40	mA
V_{CC} Current (Standby)	I_{CC3}	$\overline{CE}$ = $\overline{RESET}$ = V_{CC} ±0.2 V, V_{IN} ≤0.2V	V_{CCQ} = 1.8 V	—	0.2	10	µA
			V_{CCQ} = 3.0 V	—	0.2	10	µA
V_{CC} Current (Standby, Reset)*3	I_{CC4}	$\overline{RESET}$ = V_{IL}, CLK = V_{IL}	V_{CCQ} = 1.8 V	—	0.2	10	µA
			V_{CCQ} = 3.0 V	—	0.2	10	µA
V_{CC} Current (Automatic Sleep Mode)*3	I_{CC5}	Vcc=Vcc Max, $\overline{CE}$ = V_{SSQ} ± 0.2 V, $\overline{RESET}$ = V_{CCQ} ± 0.2 V, V_{IN} = V_{CCQ} ± 0.2 V or V_{SSQ} ± 0.2 V	V_{CCQ} = 1.8 V	—	0.2	10	µA
			V_{CCQ} = 3.0 V	—	0.2	10	µA
V_{CC} Active Current (Read-While-Program)*4	I_{CC6}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	25	60	mA
V_{CC} Active Current (Read-While-Erase)*4	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	25	60	mA
Input Low Level	V_{IL}	—	V_{CCQ} = 1.8 V	–0.5	—	0.2	V
			V_{CCQ} = 3.0 V	–0.5	—	0.4	V
Input High Level	V_{IH}	—	V_{CCQ} = 1.8 V	V_{CCQ} –0.2	—	V_{CCQ}+0.2	V
			V_{CCQ} = 3.0 V	V_{CCQ} –0.4	—	V_{CCQ}+0.4	V
Output Low Voltage Level	V_{OL}	I_{OL} = 100 µA, V_{CC} = V_{CC} Min = V_{CCQ}		—	—	0.1	V
Output High Voltage Level	V_{OH}	I_{OH} = –100 µA, V_{CC} = V_{CC} Min = V_{CCQ}		V_{CCQ} –0.1	—	—	V
Voltage for ACC Program Acceleration*5	V_{ACC}	—		8.5	—	9.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (Program or Erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remain stable for t_{ACC} + 60 ns.

*4: Embedded Algorithm (Program or Erase) is in progress.(@5 MHz)

*5: Applicable for only Vcc.

■ AC CHARACTERISTICS

- **Synchronous/Burst Read**

Parameter	Symbol		BS32LF				BT32LF				Unit
			-25 (40 MHz)		-18 (54 MHz)		-25 (40 MHz)		-18 (54 MHz)		
	JEDEC	Standard	Min	Max	Min	Max	Min	Max	Min	Max	
Latency	—	t_{IACC}	—	120	—	106	—	120	—	106.5	ns
Burst Access Time Valid Clock to Output Delay	—	t_{BACC}	—	20	—	13.5	—	20	—	14	ns
$\overline{AVD}$ Setup Time to CLK	—	t_{AVDS}	5	—	5	—	5	—	5	—	ns
Address Setup Time to CLK *	—	t_{ACS}	5	—	5	—	5	—	5	—	ns
Address Hold Time from CLK *	—	t_{ACH}	7	—	7	—	7	—	7	—	ns
Data Hold Time from Next Clock Cycle	—	t_{BDH}	—	4	—	4	—	4	—	4	ns
Output Enable to Output Valid	—	t_{OE}	—	20	—	13.5	—	20	—	14	ns
Chip Enable to High-Z	—	t_{CEZ}	—	10	—	10	—	10.5	—	10.5	ns
Output Enable to High-Z	—	t_{OEZ}	—	10	—	10	—	10.5	—	10.5	ns
$\overline{CE}$ Setup Time to CLK	—	t_{CES}	5	—	5	—	5	—	5	—	ns
RDY Setup Time to CLK	—	t_{RDYS}	5	—	5	—	4.5	—	4.5	—	ns
Ready Access Time from CLK	—	t_{RACC}	—	20	—	13.5	—	20	—	14	ns
Address Setup Time to $\overline{AVD}$ *	—	t_{AAS}	5	—	5	—	5	—	5	—	ns
Address Hold Time to $\overline{AVD}$ *	—	t_{AAH}	7	—	7	—	7	—	7	—	ns
$\overline{CE}$ Setup Time to $\overline{AVD}$	—	t_{CAS}	0	—	0	—	0	—	0	—	ns
$\overline{AVD}$ Low to CLK	—	t_{AVC}	5	—	5	—	5	—	5	—	ns
$\overline{AVD}$ Pulse	—	t_{AVD}	12	—	12	—	12	—	12	—	ns
Access Time	—	t_{ACC}	—	70	—	70	—	70	—	70	ns

*: Addresses are latched on the first of either the active edge of CLK or the rising edge of $\overline{AVD}$.

Note: Test Conditions:

Output Load: V_{CCQ} =1.65 V to 1.95 V :30 pF(MBM29BS32LF)

V_{CCQ} =2.7 V to 3.15 V : 30 pF(MBM29BT32LF)

Input rise and fall times: 5 ns

Input pulse levels: 0.0 V to V_{CCQ}

Timing measurement reference level

Input: $0.5 \times V_{CCQ}$ Output: $0.5 \times V_{CCQ}$

- **Asynchronous Read**

Parameter		Symbol		BS32LF		BT32LF		Unit
		JEDEC	Standard	Min	Max	Min	Max	
Access Time from $\overline{CE}$ Low		—	t_{CE}	—	70	—	70	ns
Asynchronous Access Time *1		—	t_{ACC}	—	70	—	70	ns
$\overline{AVD}$ Low Time		—	t_{AVDP}	12	—	12	—	ns
Address Setup Time to Rising Edge of AVD		—	t_{AAVDS}	5	—	5	—	ns
Address Hold Time from Rising Edge of AVD		—	t_{AAVDH}	7	—	7	—	ns
Output Enable to Output Valid		—	t_{OE}	—	20	—	20.5	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	0	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	10	—	ns
Output Enable to High-Z *2		—	t_{OEZ}	—	10	—	10.5	ns
$\overline{CE}$ Setup Time to $\overline{AVD}$		—	t_{CAS}	0	—	0	—	ns

*1: Asynchronous Access Time is from the last of either stable addresses or the falling edge of $\overline{AVD}$.

*2: Addresses are latched on the rising edge of $\overline{AVD}$ or Address change timing.

- **Hardware Reset ($\overline{RESET}$)**

Parameter	Symbol		All Speed Options		Unit
	JEDEC	Standard	Min	Max	
$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read Mode	—	t_{READY}	—	20	µs
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	ns
Reset High Time Before Read	—	t_{RH}	200	—	ns
Power On/Off Time	—	t_{PS}	0	—	ns

- **Write (Erase/Program) Operations**

Parameter		Symbol		All Speed Options		Unit
		JEDEC	Standard	Min	Typ	
Write Cycle Time		t_{AVAV}	t_{WC}	80	—	ns
Address Setup Time *1	Program 1($\overline{WE}$ or CLK)	t_{AVWL}	t_{AS}	0	—	ns
	Program 2($\overline{AVD}$ or CLK)			5	—	
Address Hold Time *1	Program 1($\overline{WE}$ or CLK)	t_{WLAX}	t_{AH}	45	—	ns
	Program 2($\overline{AVD}$ or CLK)			7	—	
$\overline{AVD}$ Low Time		—	t_{AVDP}	12	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	45	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	ns
Read Recovery Time Before Write		t_{GHWL}	t_{GHWL}	0	—	ns
$\overline{CE}$ Setup Time to $\overline{AVD}$		—	t_{CAS}	0	—	ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	ns
Write Pulse Width		t_{EHWH}	t_{WP}	50	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	30	—	ns
Latency Between Read and Write Operations		—	$t_{SR/W}$	0	—	ns
Programming Operation *2		t_{WHWH1}	t_{WHWH1}	—	8	µs
Accelerated Programming Operation *2		t_{WHWH1}	t_{WHWH1}	—	2.5	µs
Sector Erase Operation *2, *3		t_{WHWH2}	t_{WHWH2}	—	0.5	s
Chip Erase Operation *2, *3				—	35.0	
V_{ACC} Rise and Fall Time		—	t_{VID}	500	—	ns
V_{ACC} Setup Time (During Accelerated Programming)		—	t_{VIDS}	1	—	µs
V_{CC} Setup Time		—	t_{VCS}	50	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$		t_{ELWL}	t_{CS}	0	—	ns
$\overline{AVD}$ Setup Time to $\overline{WE}$		—	t_{ASW}	5	—	ns
$\overline{AVD}$ Hold Time to $\overline{WE}$		—	t_{AHW}	5	—	ns
Address Setup Time to CLK *1		—	t_{ACS}	5	—	ns
Address Hold Time to CLK *1		—	t_{ACH}	7	—	ns
$\overline{AVD}$ Hold Time to CLK		—	t_{AVCH}	5	—	ns
$\overline{WE}$ Low to CLK		—	t_{WLC}	0	—	ns
CLK to $\overline{WE}$ Low		—	t_{CWL}	5	—	ns

*1: In Program 1 timing, addresses are latched on the falling edge of $\overline{WE}$. In Program 2 timing, addresses are latched on the first of either the rising edge of $\overline{AVD}$ or the active edge of CLK.

*2: See the "Erase and Programming Performance" section for more information.

*3: Does not include the preprogramming time.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limit			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	0.5	2.0	s	Excludes programming prior to erasure
Word Programming Time	—	6	100	µs	Excludes system level overhead
Chip Programming Time	—	25.2	95	s	Excludes system level overhead
Erase/Program Cycle	100,000			cycle	—

Note : Test conditions T_A = +25°C, Typical Erase conditions T_A = +25°C, V_{CC} = 1.8 V
Typical Program conditions T_A = +25°C, V_{CC} = 1.8 V, Data = checker

■ FBGA PIN CAPACITANCE

Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0	TBD	TBD	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	TBD	TBD	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	TBD	TBD	pF

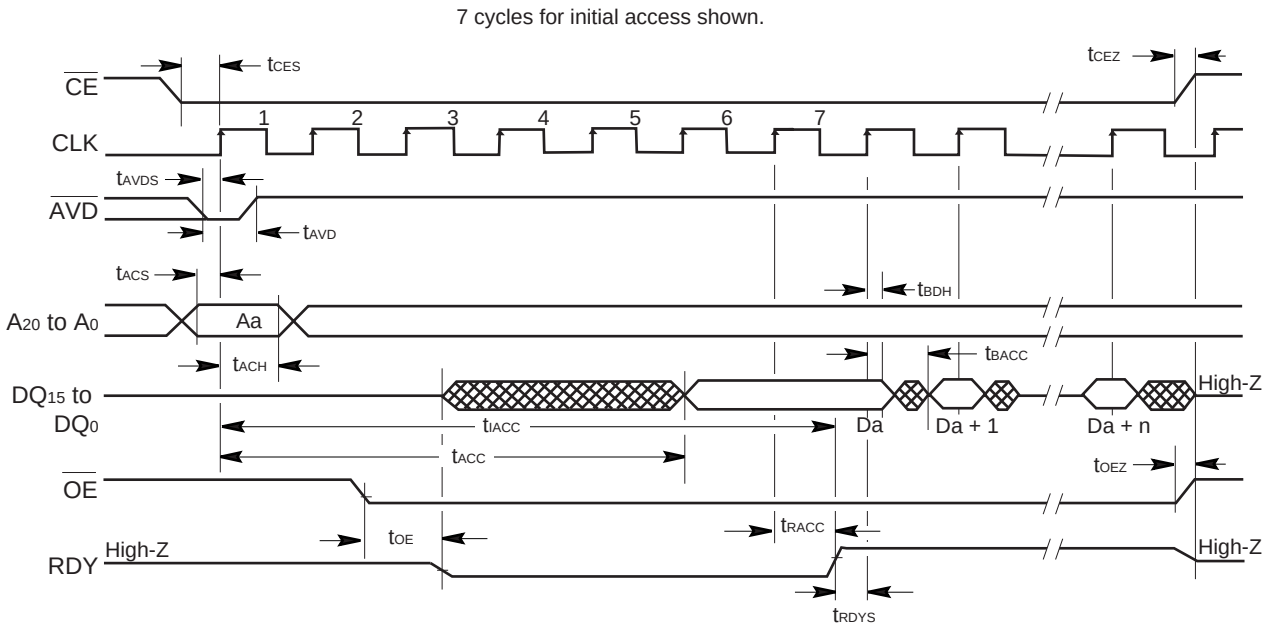
Note : Test conditions T_A = +25°C, f = 1.0 MHz

■ TIMING DIAGRAMS

- **Key to Switching Wavwforms**

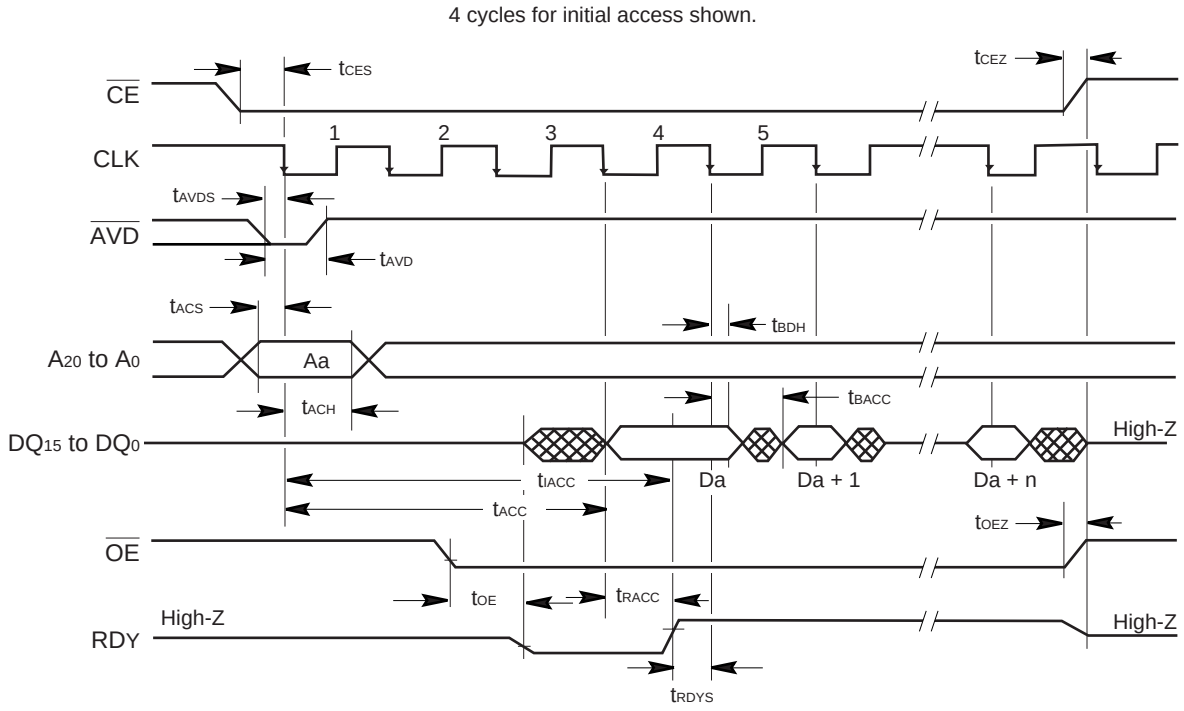
Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High-Z)

(1) Synchronous Burst Mode Read (Latched By Rising Active CLK)



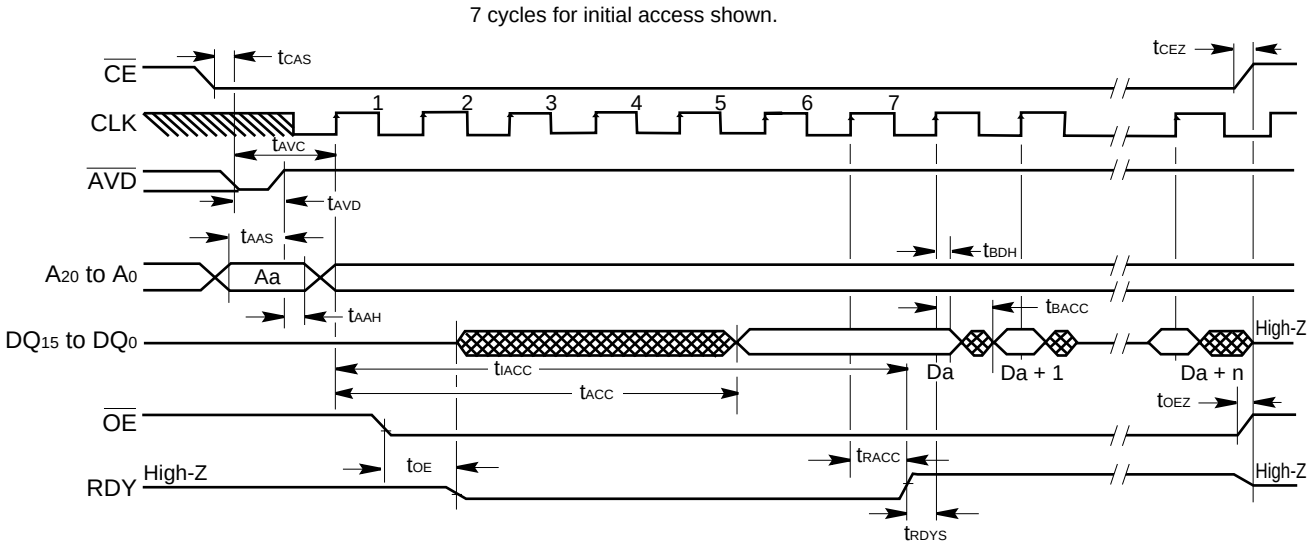
Notes: • Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.
• The device is in synchronous mode.

(2) Synchronous Burst Mode Read (Latched By Falling Active CLK)



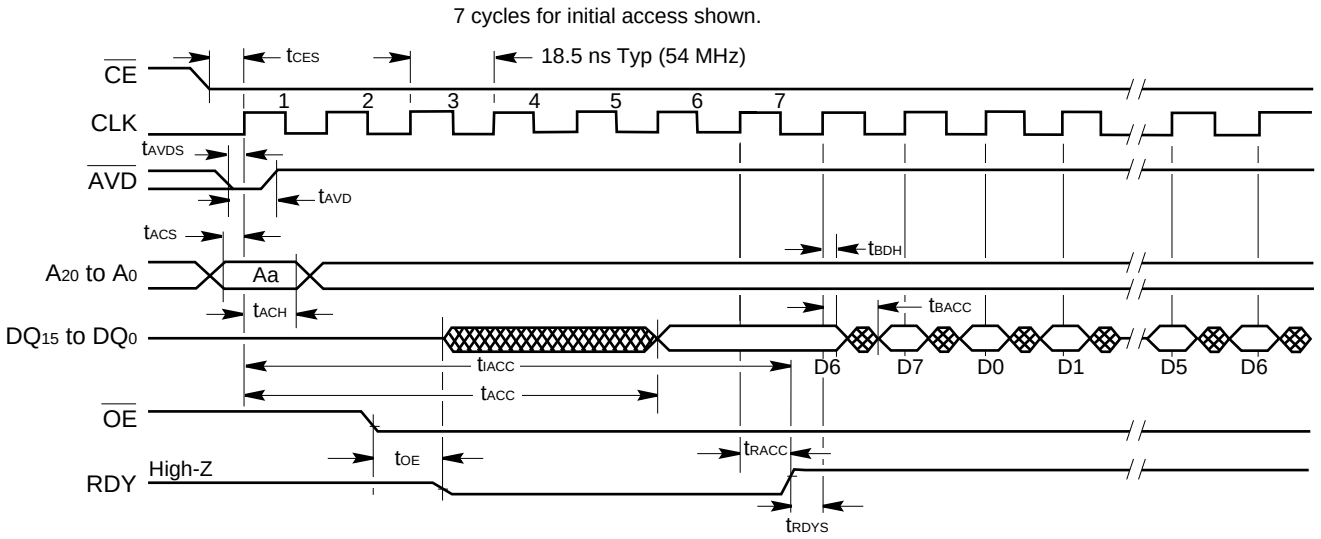
Notes: • Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.
• The device is in synchronous mode.

(3) Synchronous Burst Mode Read(Latched By $\overline{\text{AVD}}$ Active Edge)



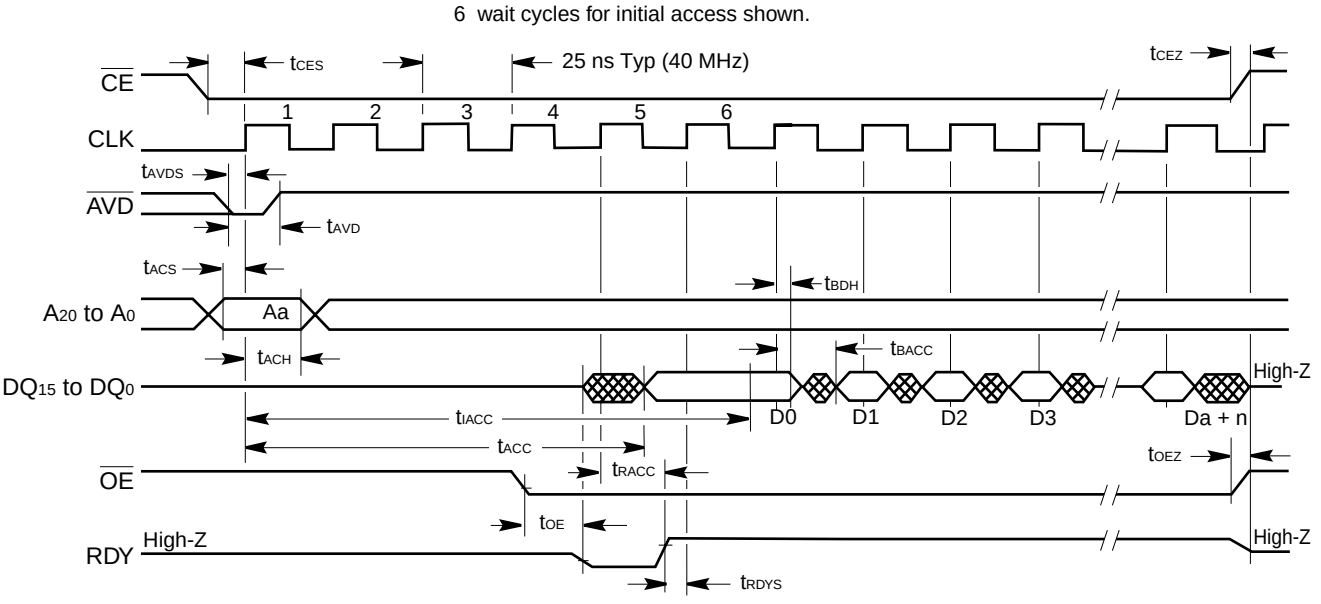
Notes: • Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.
• The device is in synchronous mode.

(4) 8-word Linear Burst With Wrap Around



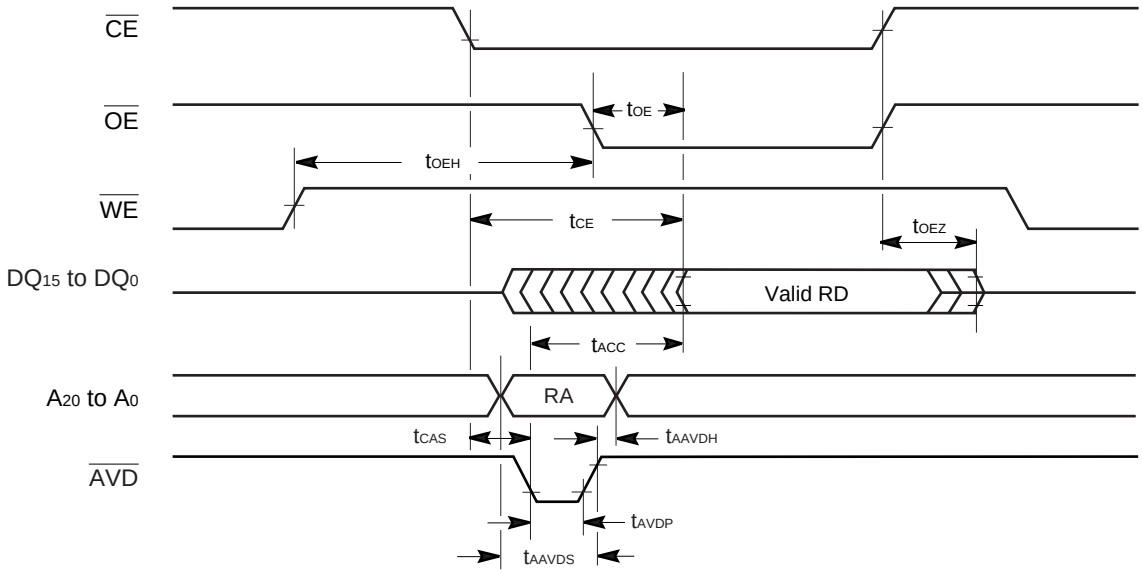
Note: Figure assumes 7 wait states for initial access, 54 MHz clock, synchronous read. D0 to D7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 7th address in range (A_6). See “Requirements for Synchronous (Burst) Read Operation”. The Set Configuration Register command sequence has been written with A_{18} = 1; device will output RDY with valid data.

(5) Burst with RDY Set One Cycle Before Data



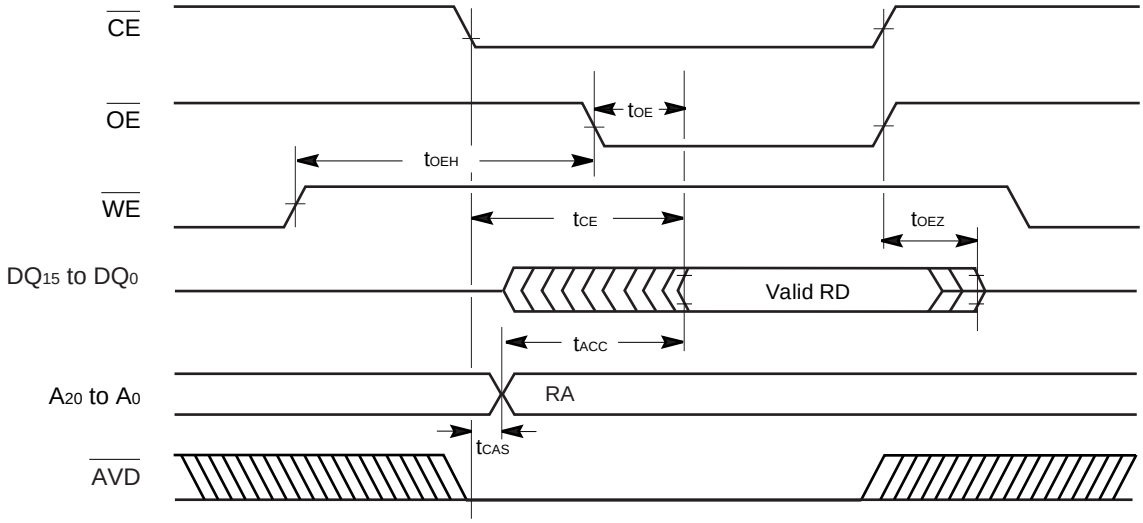
Note: Figure assumes 6 wait states for initial access, 40 MHz clock, and synchronous read. The Set Configuration Register command sequence has been written with A_{18} = 0; device will output RDY one cycle before valid data.

(6) Asynchronous Mode Read With $\overline{AVD}$ Latched



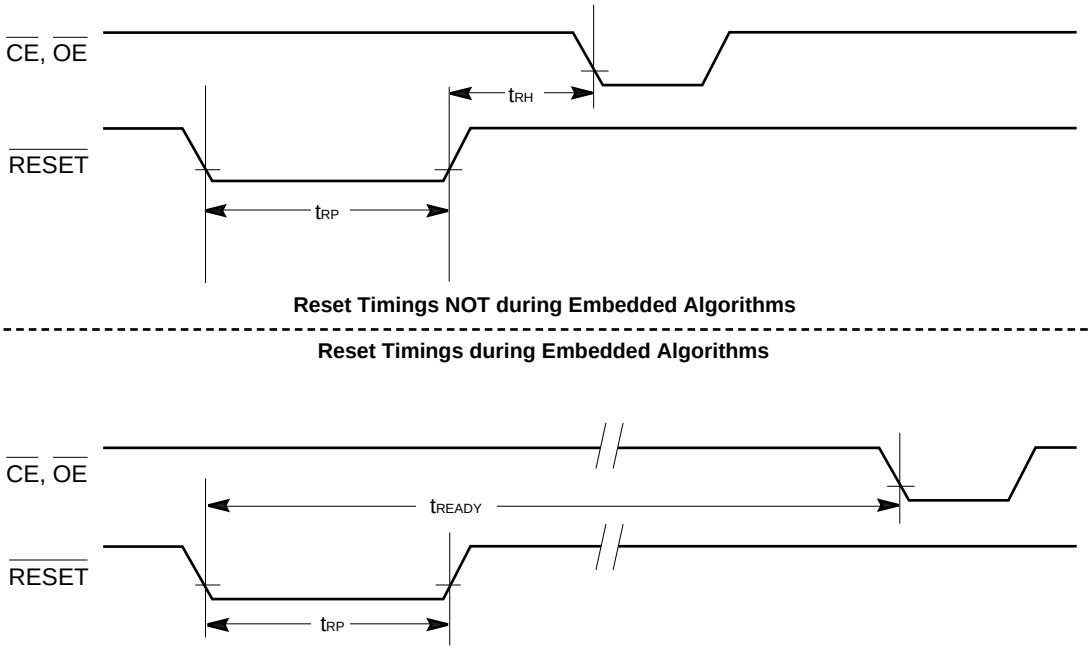
Note: RA = Read Address, RD = Read Data.

(7) Asynchronous Mode Read With $\overline{AVD}$ Stable Low

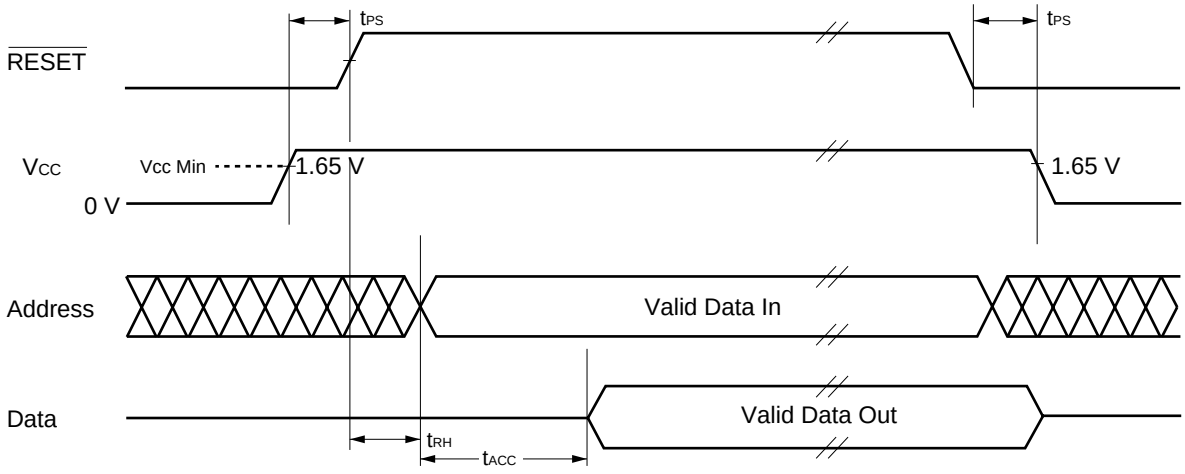


Note: RA = Read Address, RD = Read Data.

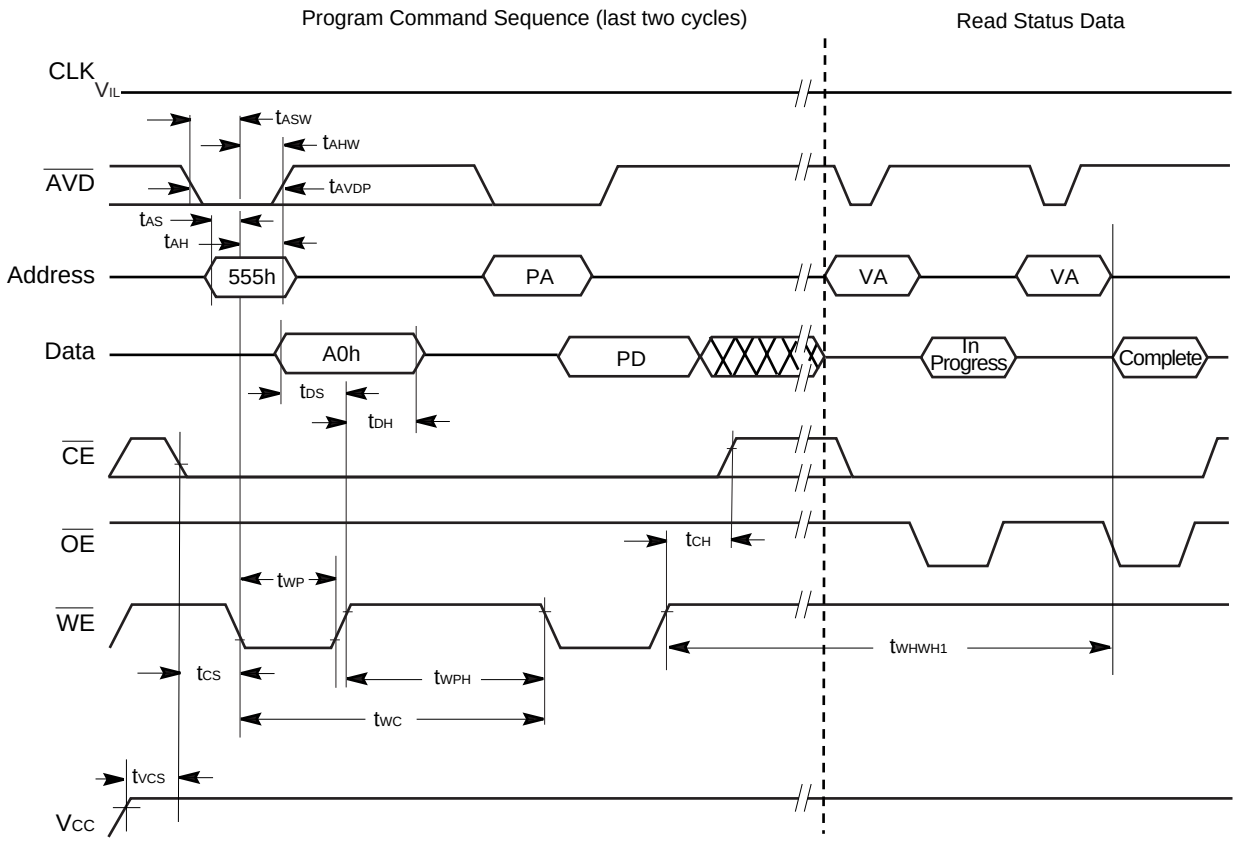
(8) Reset Timings



(9) Power On/Off Timings

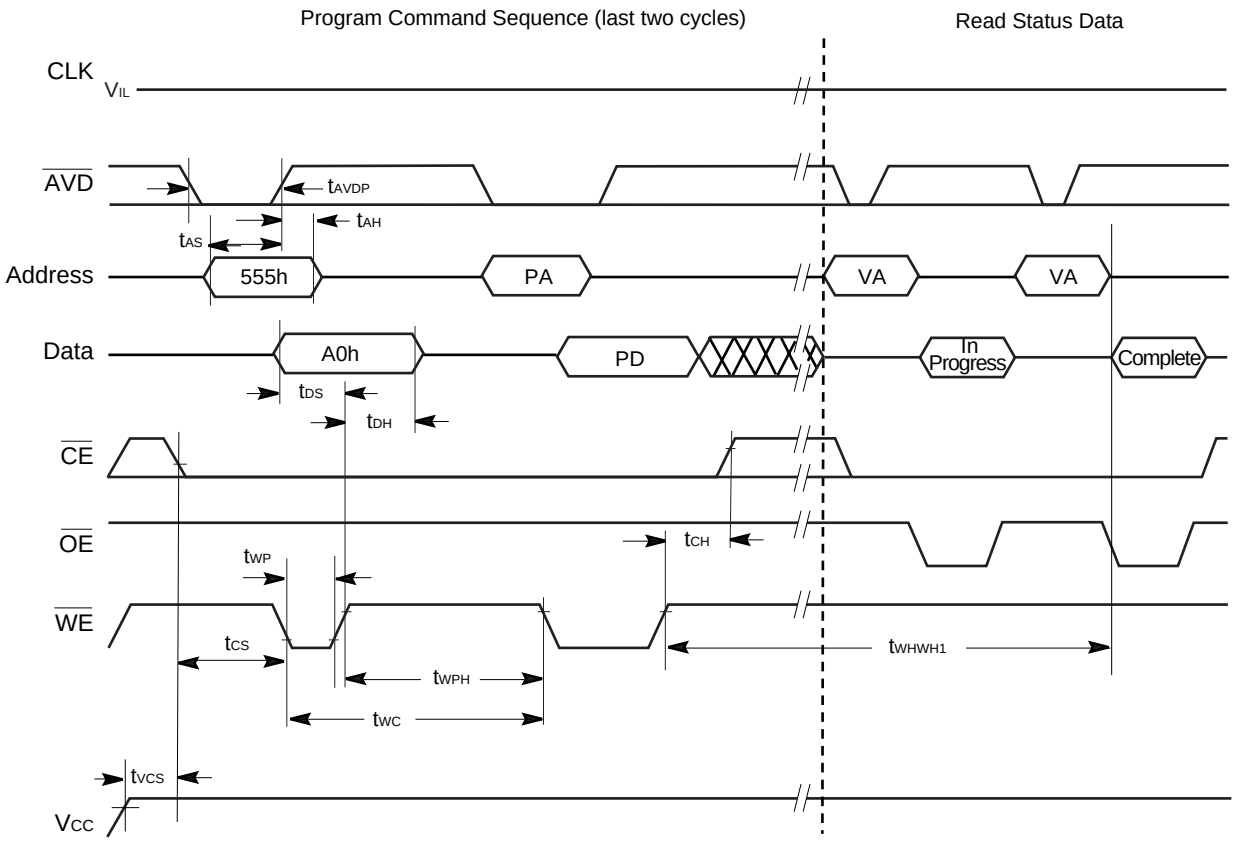


(10) Programming Operation Timings ($\overline{WE}$ latched address at CLK=V_{IL}) (Program1 $\overline{WE}$)



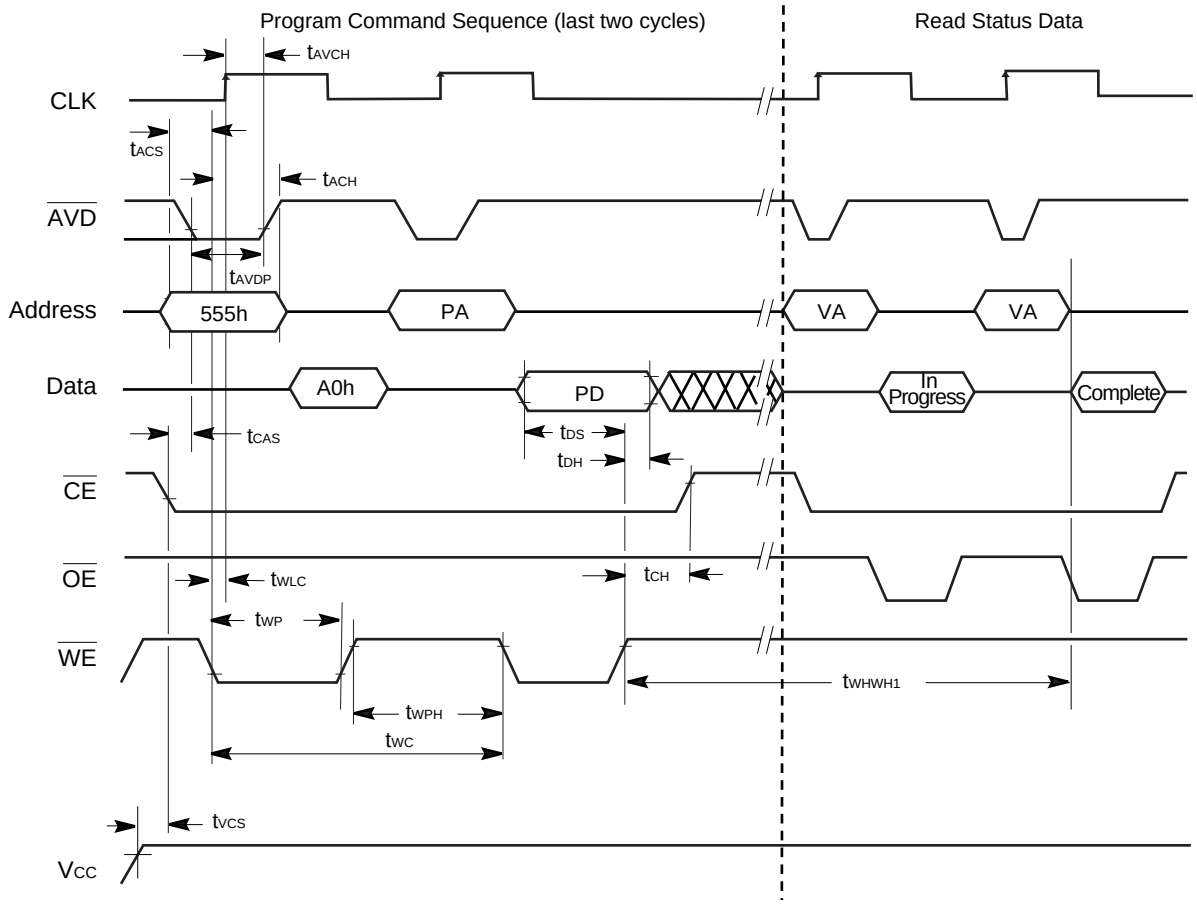
Notes:
- PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
- “In progress” and “complete” refer to status of program operation.
- A_{20} to A_{12} are don’t care during command sequence unlock cycles.
- CLK must be fixed at V_{IL}.(Don’t be fixed at V_{IH})
- Either CE or AVD is required to go from low to high in between programming command sequences.
- The Programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

(11) Programming Operation Timings ($\overline{AVD}$ latched address at CLK=V_{IL}) (Program1 $\overline{AVD}$)



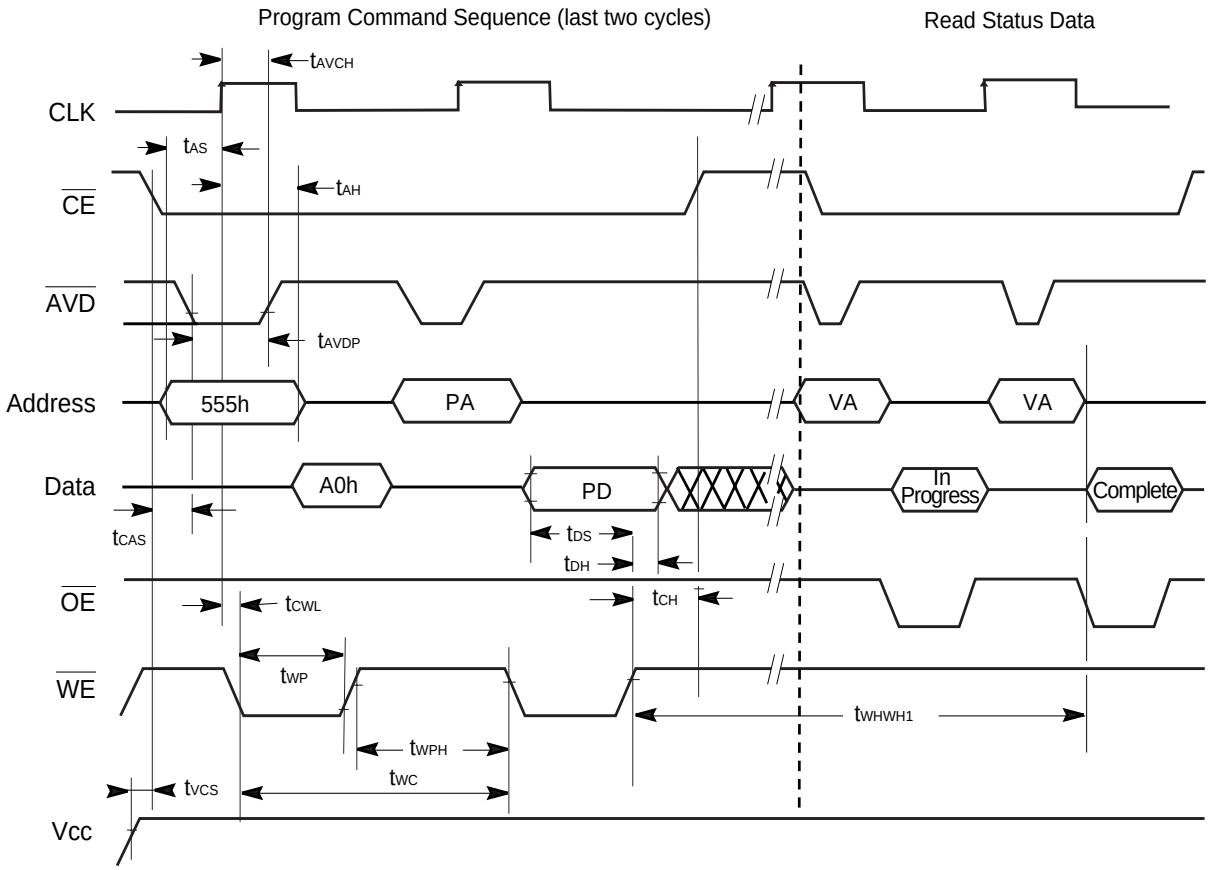
Notes:
- PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
- “In progress” and “complete” refer to status of program operation.
- A_{20} to A_{12} are don’t care during command sequence unlock cycles.
- CLK must be fixed at V_{IL}.(Don’t be fixed at V_{IH})
- Either CE or AVD is required to go from low to high in between programming command sequences.
- The programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

(12) Programming Operation Timings ($\overline{WE}$ or CLK latched address) (Program1 $\overline{WE}$ or CLK)



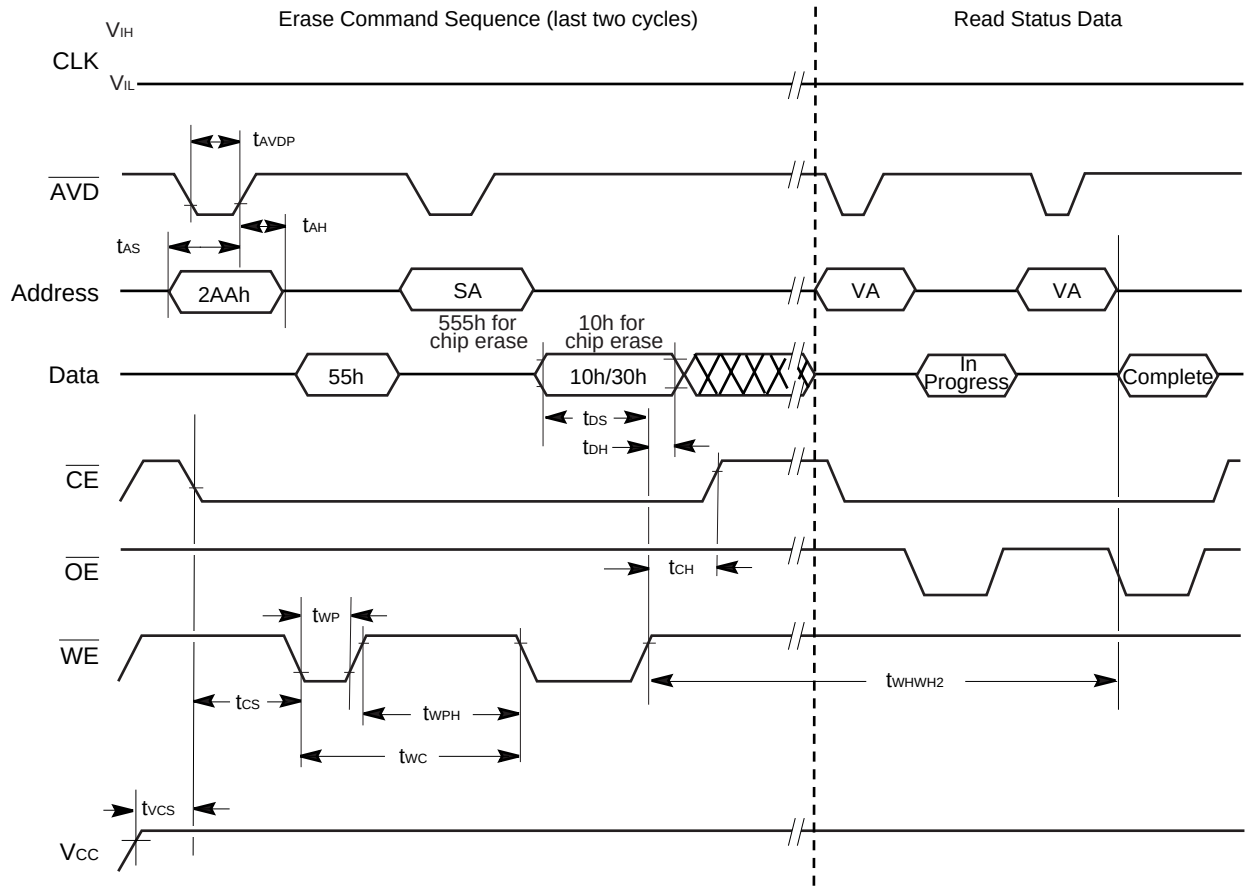
Notes:
- PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
- "In progress" and "complete" refer to status of program operation.
- A_{20} to A_{12} are don't care during command sequence unlock cycles.
- Addresses are latched on the first of either the rising edge of $\overline{WE}$ or the active edge of CLK. If CLK active edge will not appear until $\overline{WE}$ falling edge, program timing become programming operation ($\overline{WE}$ latched address).
- Either $\overline{CS}$ or $\overline{AVD}$ is required to go from low to high inbetween programming command sequences.
- The programming operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

(13) Programming Operation Timings ($\overline{AVD}$ or CLK latched address) (Program2 $\overline{AVD}$ or CLK)



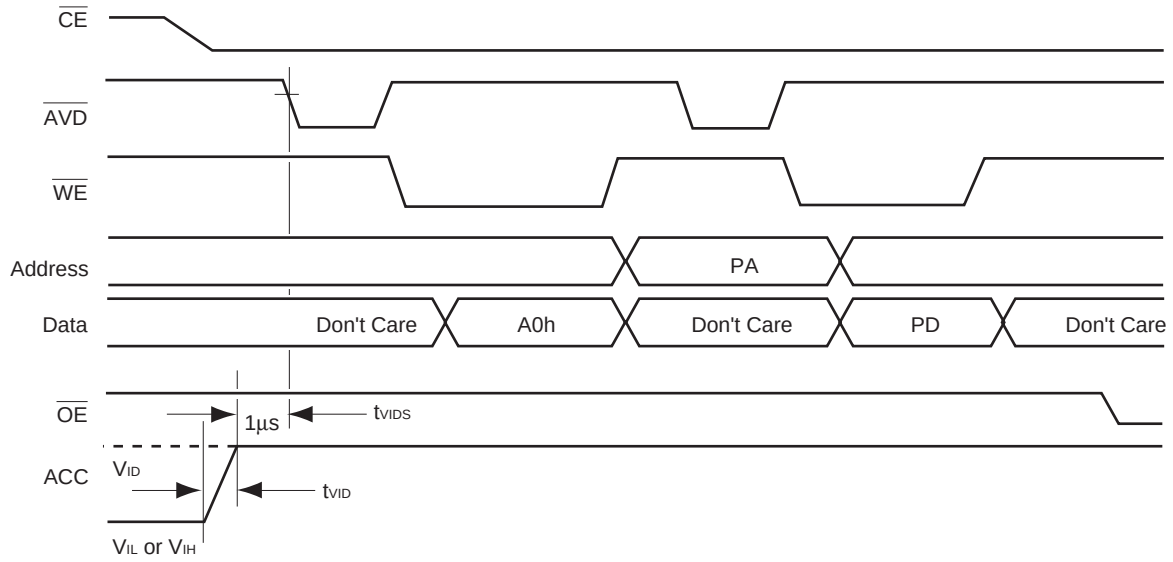
Notes:
- PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
- "In progress" and "complete" refer to status of program operation.
- A_{20} to A_{12} are don't care during command sequence unlock cycles.
- Addresses are latched on the first of either the rising edge of $\overline{AVD}$ or the active edge of CLK. If CLK active edge will appear while $\overline{AVD}$=V_{IL}, program timing become Program operation (CLK latched address).
- Either $\overline{CS}$ or $\overline{AVD}$ is required to go from low to high inbetween programming command sequences.
- The Program operation is independent of the Set Device Read Mode bit in the Burst Mode Configuration Register.

(14) Chip/Sector Erase Command Sequence



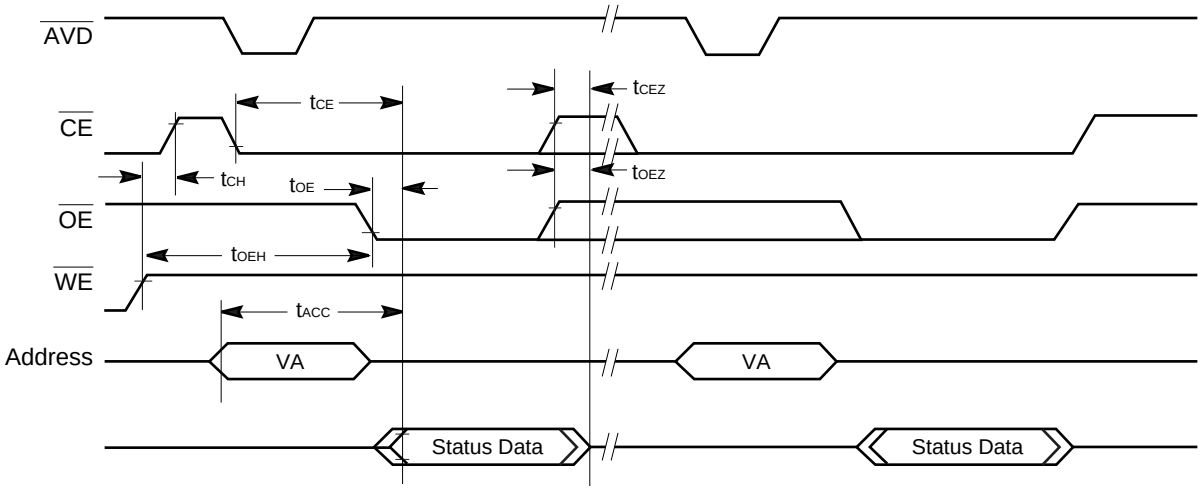
Notes: • SA is the sector address for Sector Erase.
• Address bits A_{20} to A_{12} are don't cares during unlock cycles in the command sequence.

(15) Accelerated Fast mode Programming Timing



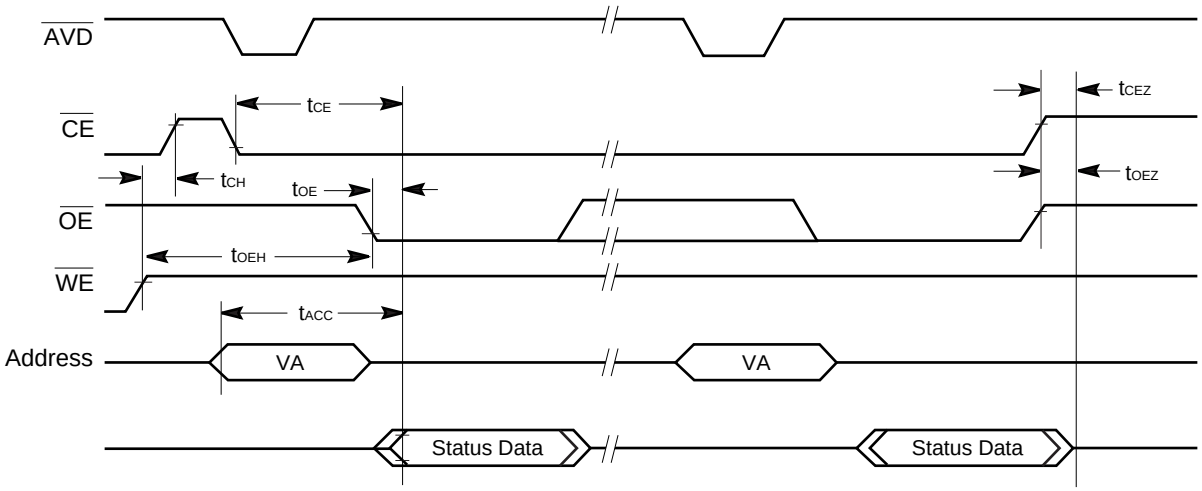
Note: Use setup and hold times from conventional program operation.

(16) $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithm)



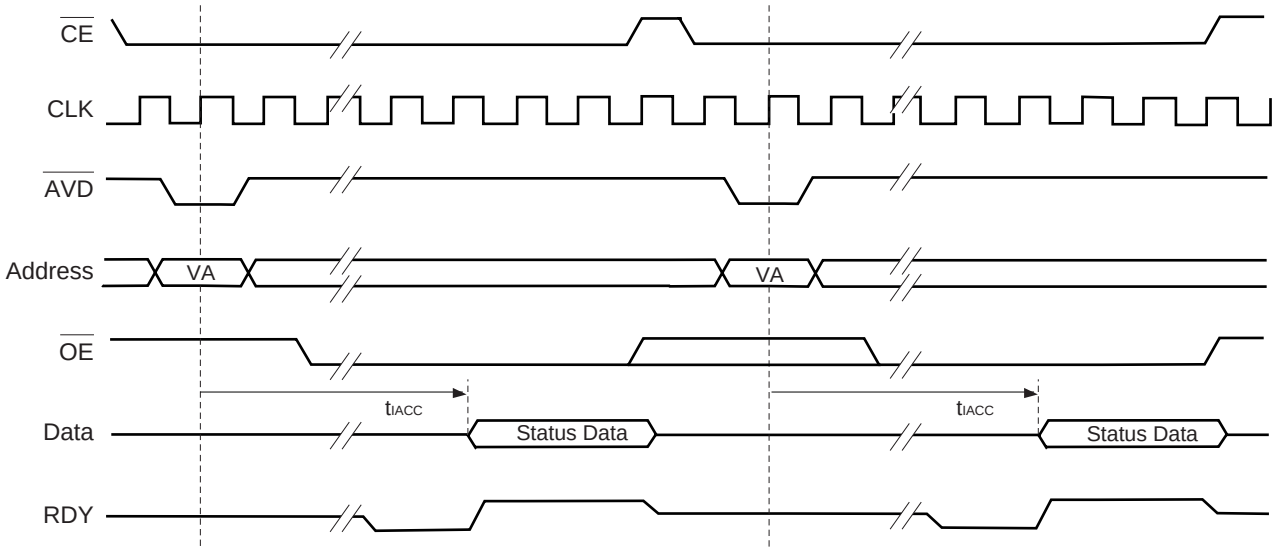
Notes:
- Status reads in figure are shown as asynchronous.
- VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and $\overline{\text{Data}}$ Polling will output true data.

(17) Toggle Bit Timings (During Embedded Algorithm)



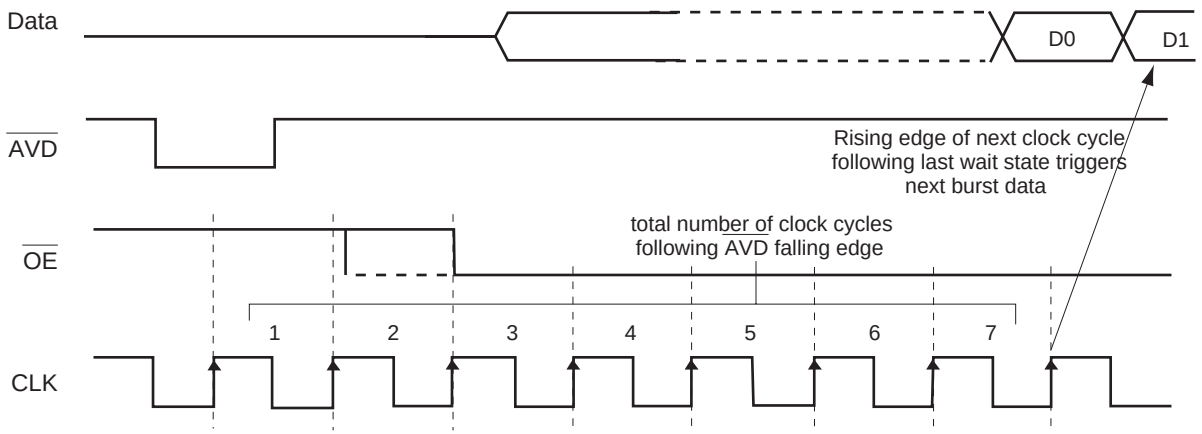
Notes: • Status reads in figure are shown as asynchronous.
• VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.

(18) Synchronous Read Data Polling Timings/Toggle Bit Timings



Notes: • The timings are similar to synchronous read timings.
• VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.
• RDY is active with data (A_{18} = 1in the Burst Mode Configuration Register). When A_{18} = 0 in the Burst Mode Configuration Register, RDY is active one clock cycle before data.

(19) Example of Wait States Insertion

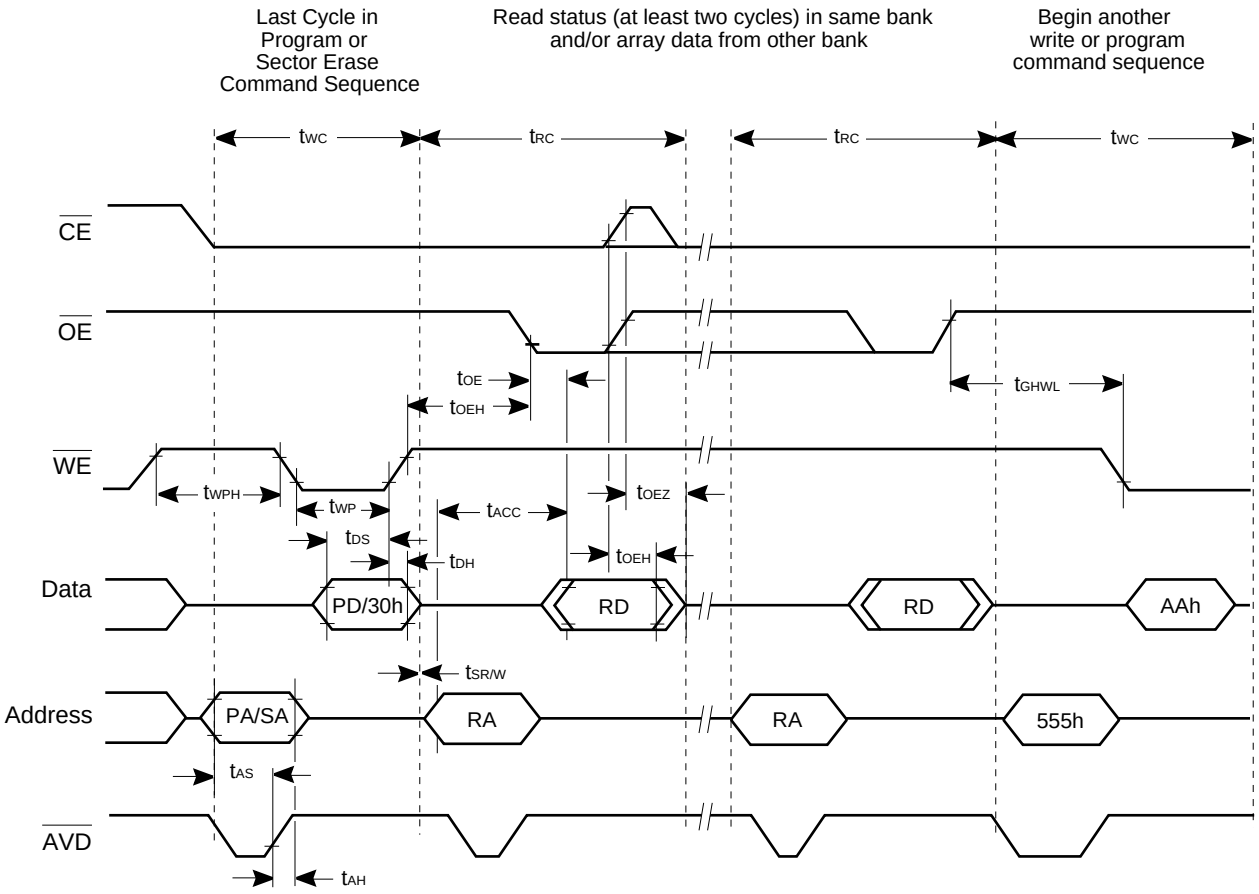


Wait State Decoding Addresses:

A_{14}, A_{13}, A_{12} = "101" ⇒ 7 cycles
A_{14}, A_{13}, A_{12} = "100" ⇒ 6 cycles
A_{14}, A_{13}, A_{12} = "011" ⇒ 5 cycles
A_{14}, A_{13}, A_{12} = "010" ⇒ 4 cyclesl
A_{14}, A_{13}, A_{12} = "001" ⇒ 3 cycles
A_{14}, A_{13}, A_{12} = "000" ⇒ 2 cycles

Note: Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to “101”.

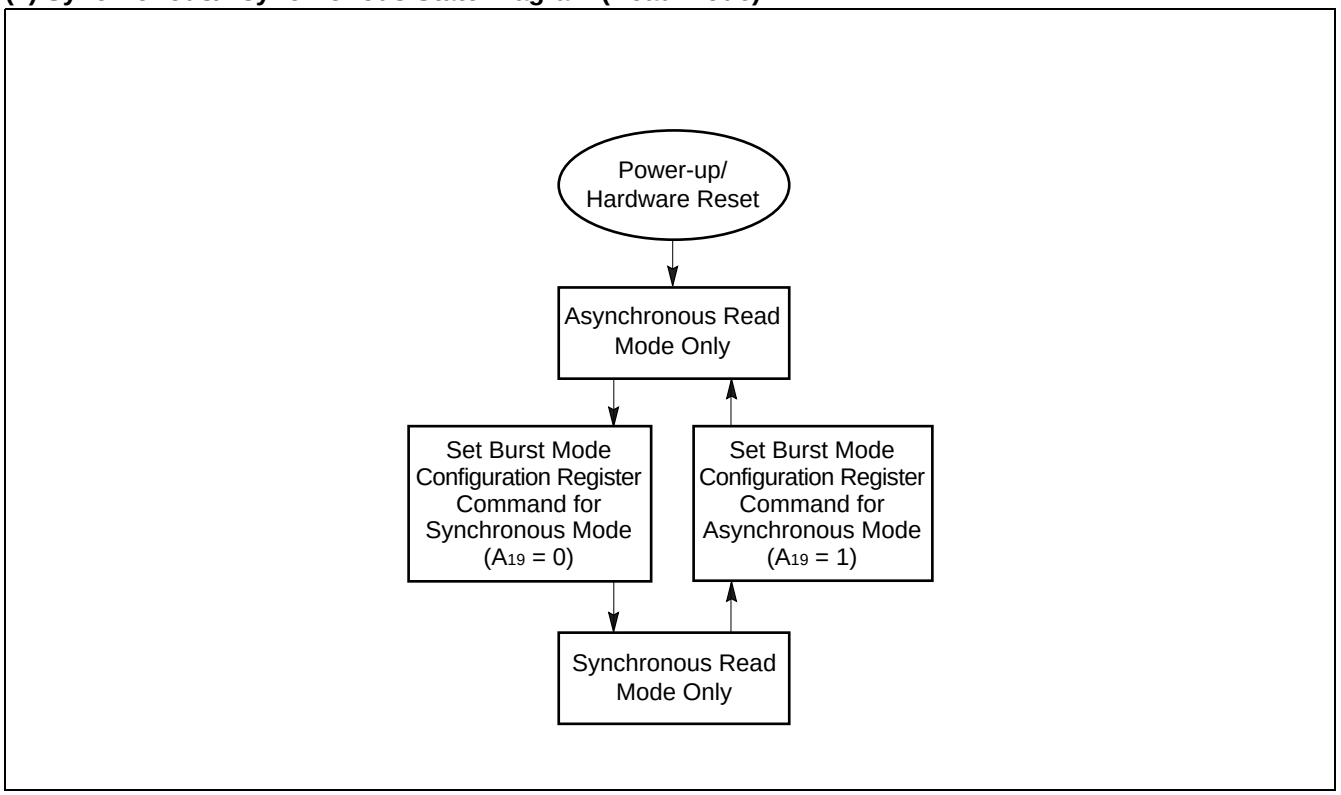
(20) Bank-to-Bank Read/Write Cycle Timings



Note: Break points in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.

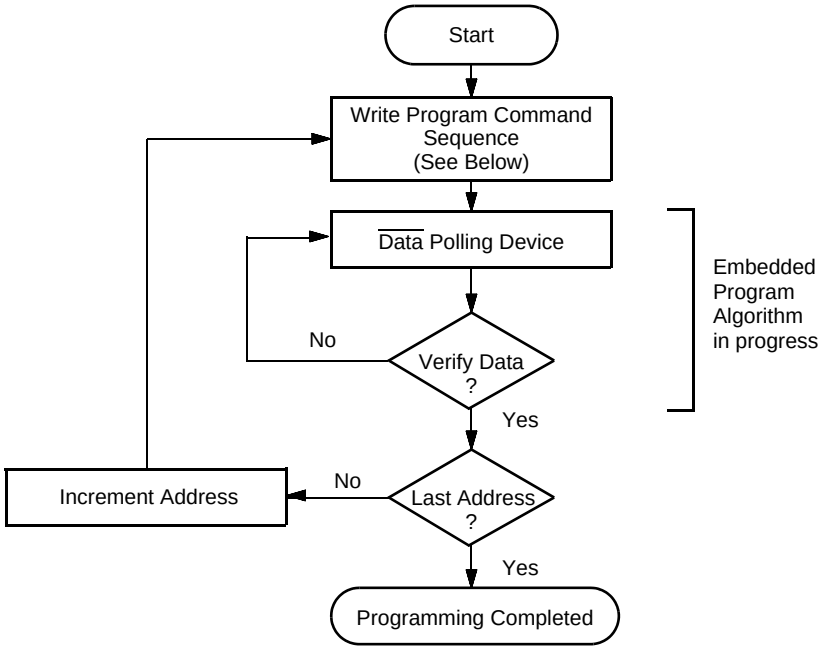
■ FLOW CHART

(1) Synchronous/Asynchronous State Diagram (Read Mode)

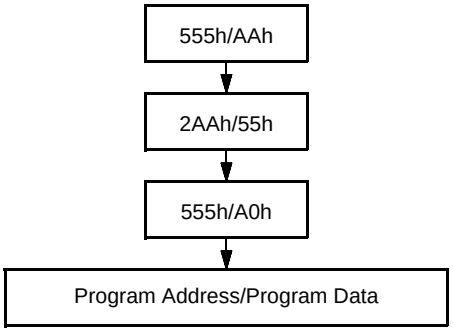


(2) Embedded Program™ Algorithm

EMBEDDED ALGORITHM

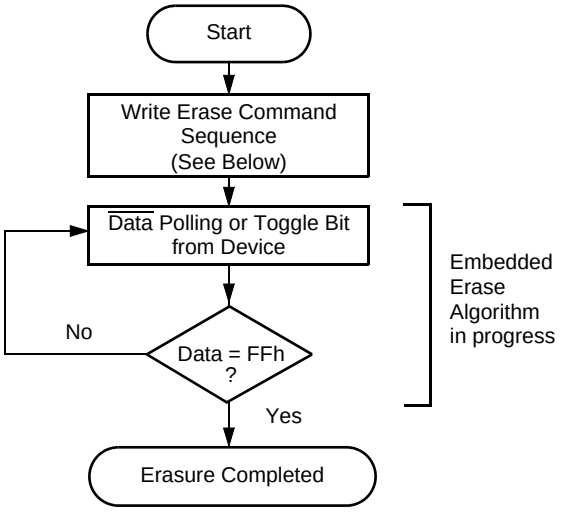


Program Command Sequence (Address/Command):

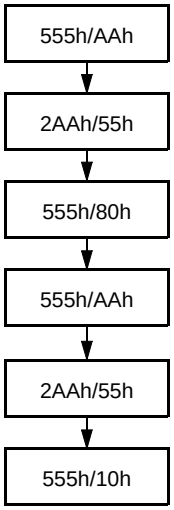


(3) Embedded Erase™ Algorithm

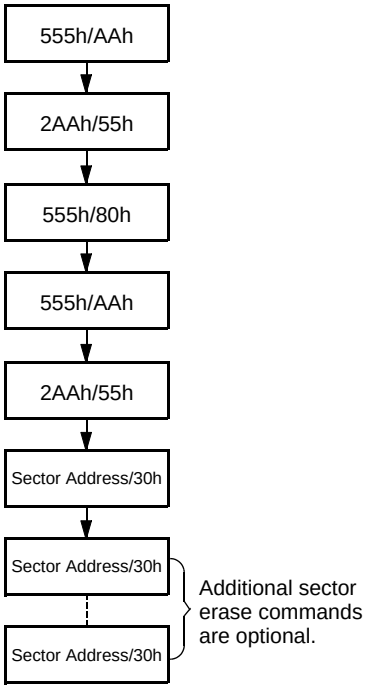
EMBEDDED ALGORITHM



Chip Erase Command Sequence (Address/Command):



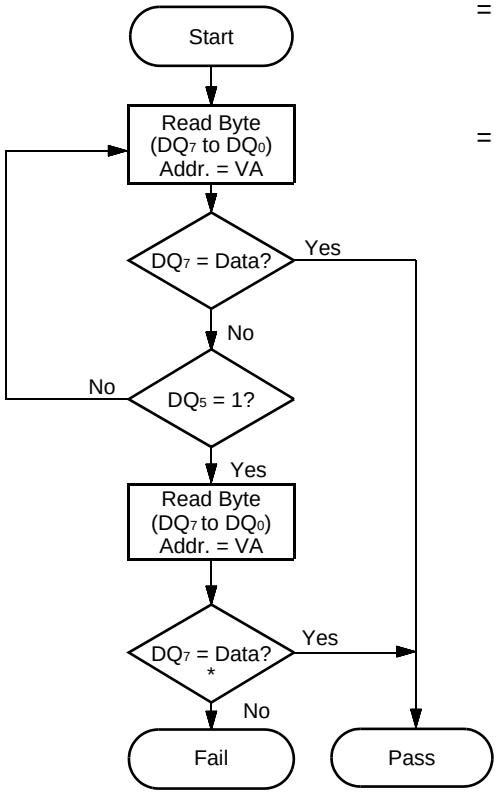
Individual Sector/Multiple Sector Erase Command Sequence (Address/Command):



Notes: • See “MBM29BS/BT32LF Command Definitions Table” in ■DEVICE BUS OPERATIONS for erase command sequence.
• See the section on DQ_3 for information on the sector erase timer.

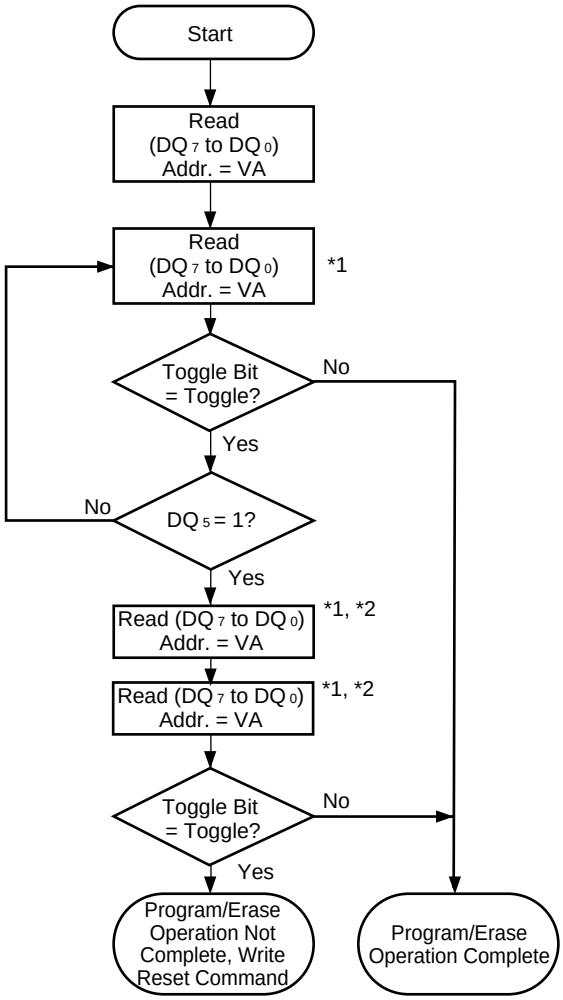
(4) $\overline{\text{Data}}$ Polling Algorithm

VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.



*: DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

(5) Toggle Bit Algorithm

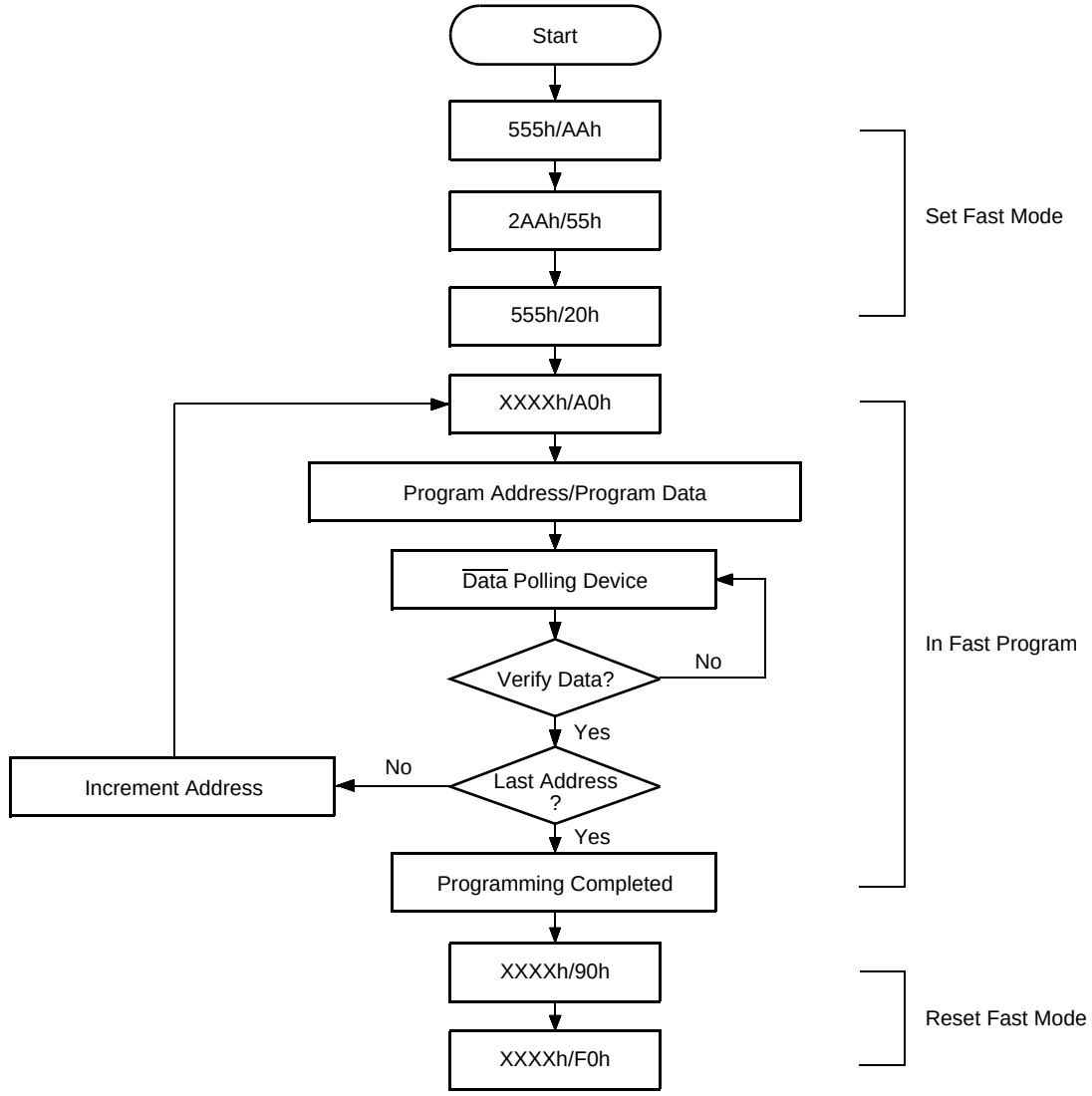


VA = Bank address being executed Embeded Algorithm.

*1 : Read toggle bit twice to determine whether or not it is toggling.
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

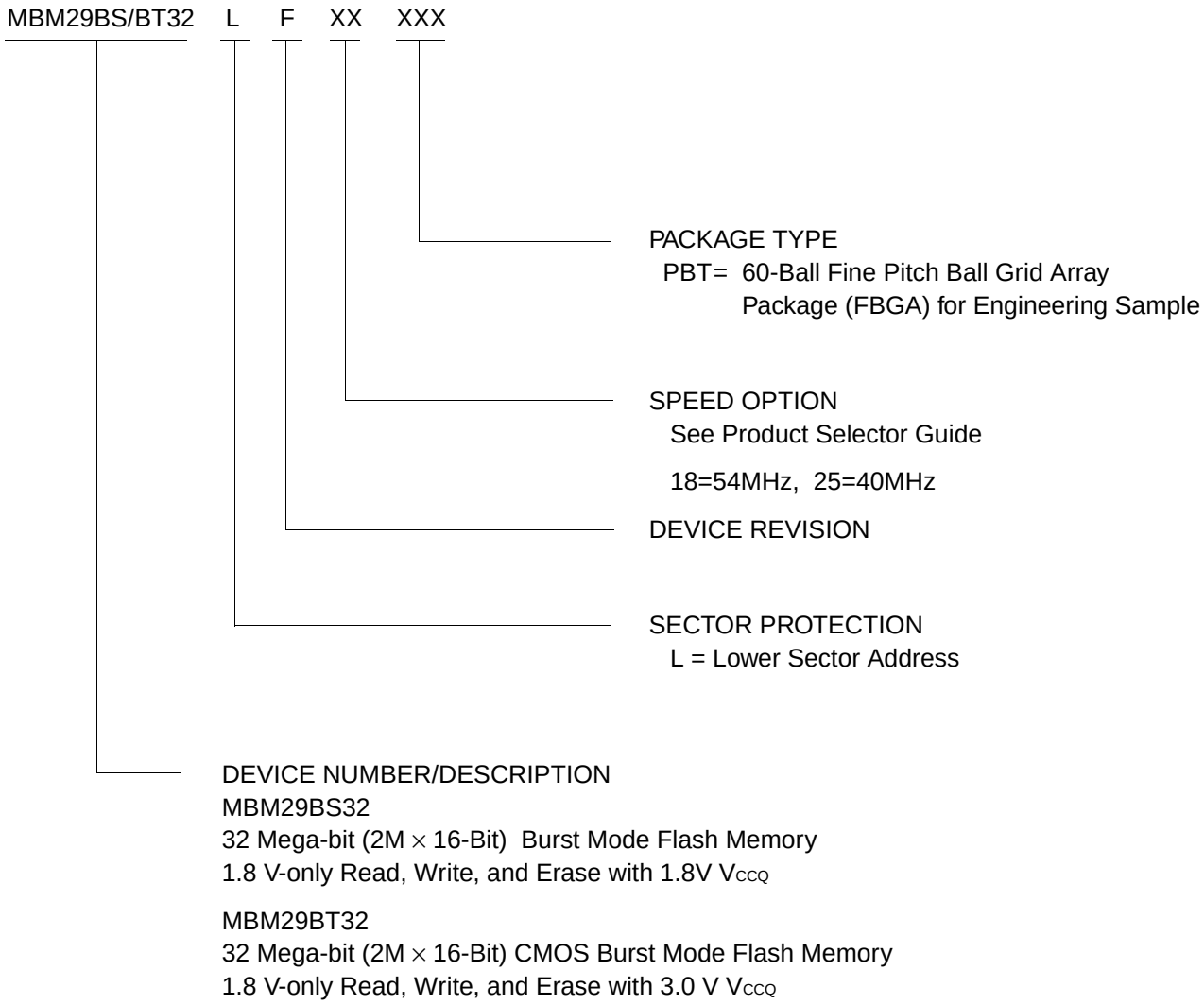
(6) Embedded Programming Algorithm for Fast Mode

FAST MODE ALGORITHM



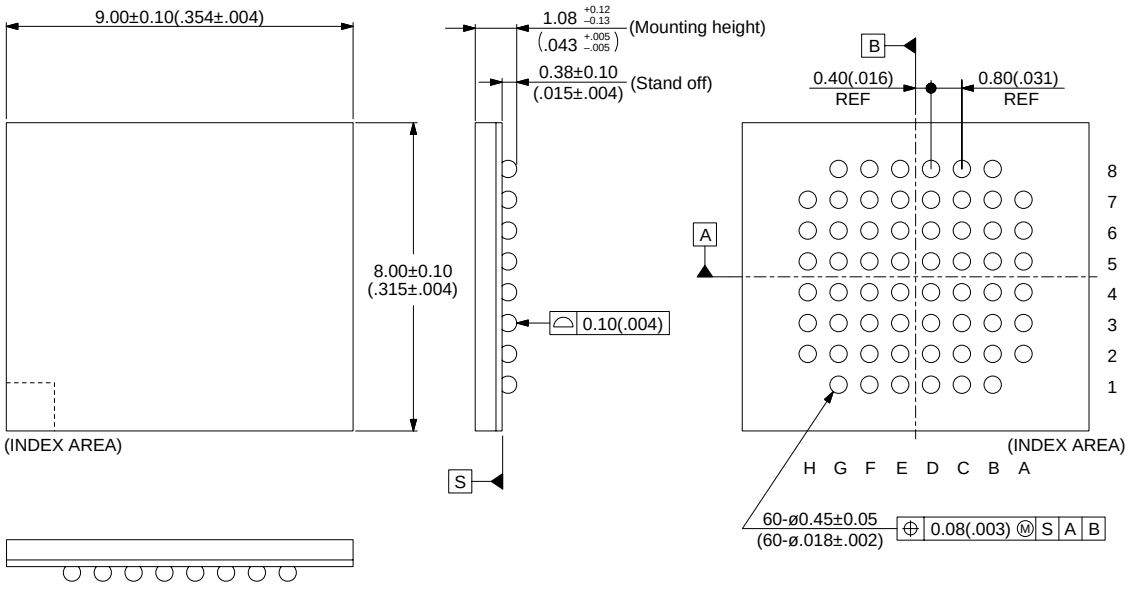
■ ORDERING INFORMATION

Part No.	Package	Access Time(ns)	Remarks
MBM29BS32LF18PBT MBM29BS32LF25PBT	60-pin plastic FBGA (BGA-60P-M05)	54 40	
MBM29BT32LF18PBT MBM29BT32LF25PBT		54 40	



■ PACKAGE DIMENSIONS

60-ball plastic FBGA
(BGA-60P-M05)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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