
ML1538 4-ch Motor Driver for Portable CD players

❖ Application

- ◆ *Portable CD player*

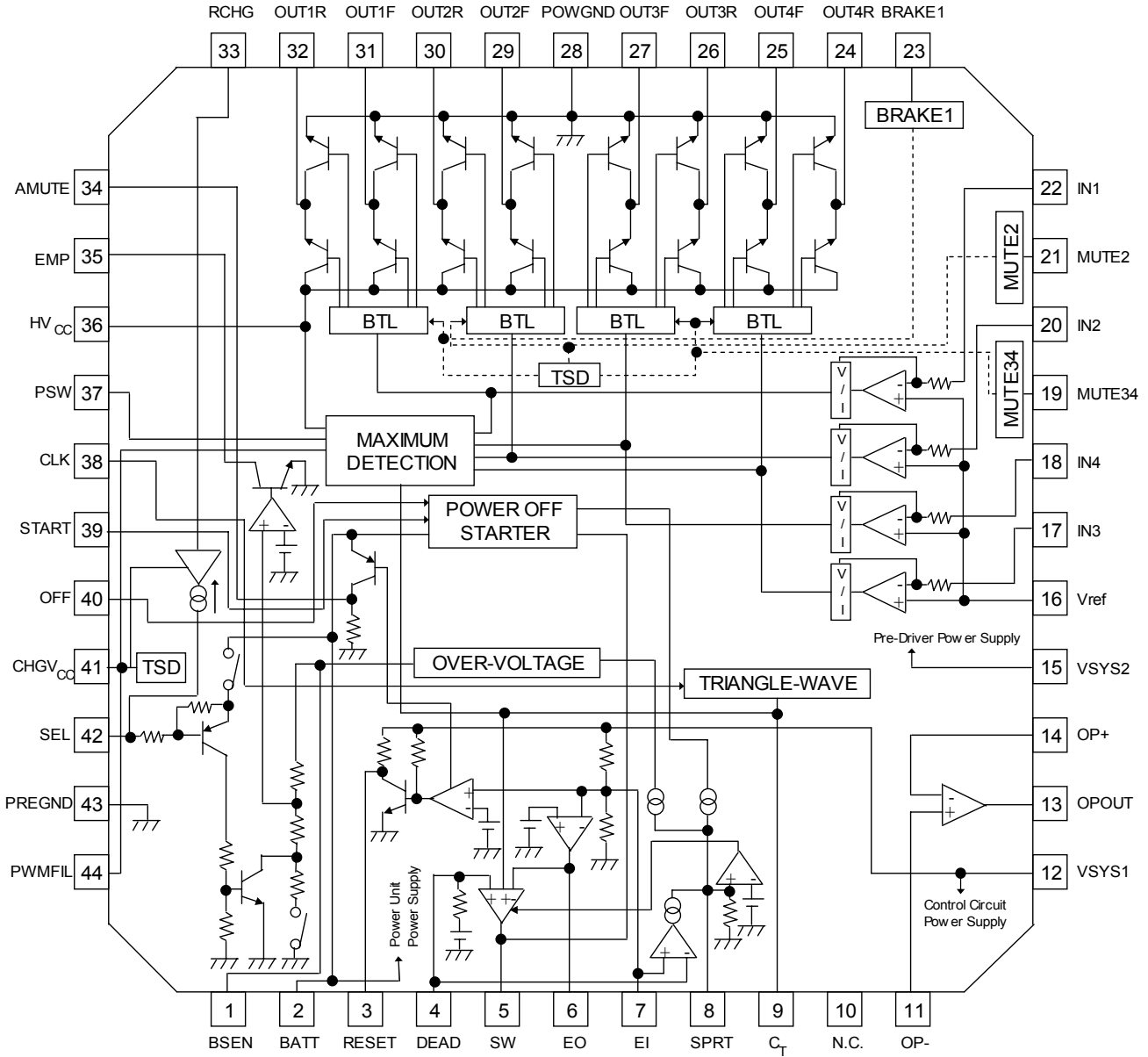
❖ Features

- Built-in 4ch H bridge driver, and PWM control of load drive voltage is made possible by external components.
- DC-DC converter control circuit on chip.
- With inverted reset output pin.
- Empty detection level can be switched between rechargeable battery and dry battery.
- Constant current charging; amount of current can be varied by external resistor.
- Built-in power transistor for charging.
- Built-in independent thermal shutdown circuit
- Package : QFP-44

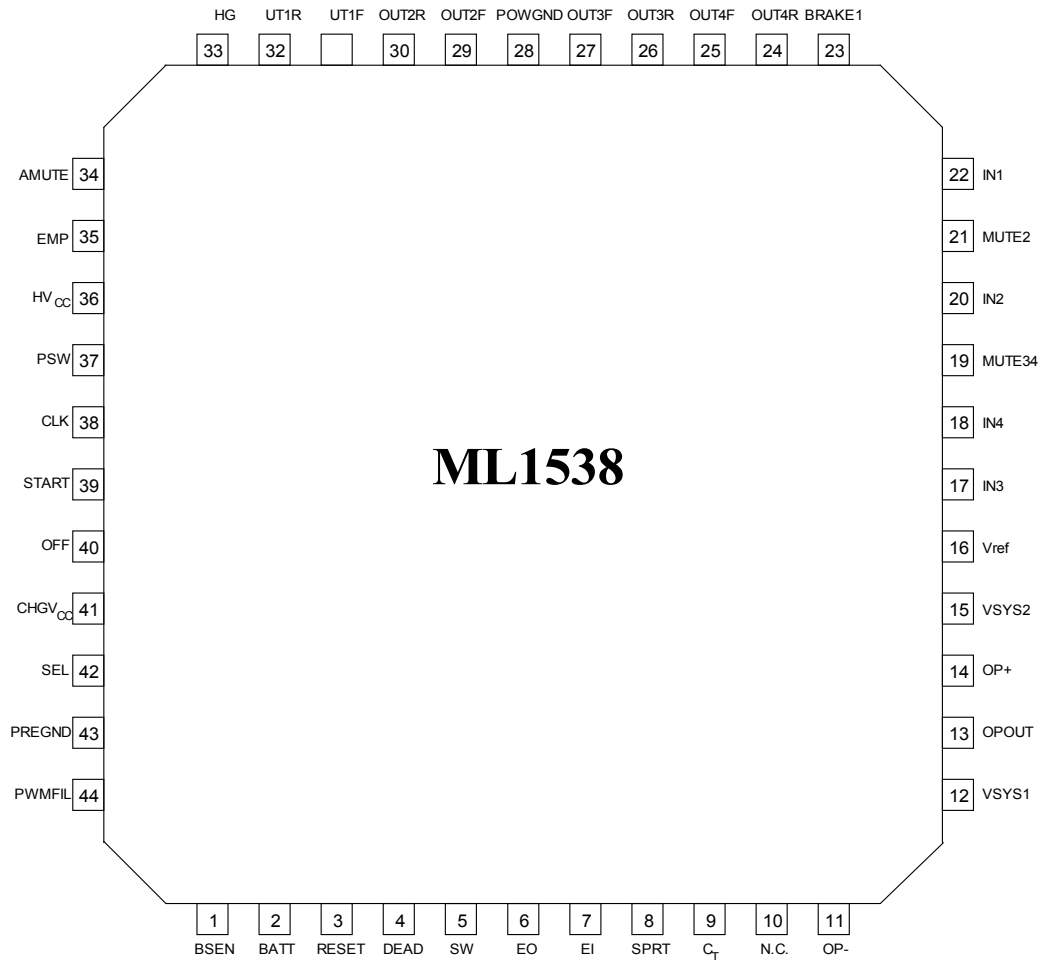
❖ General Description

ML1538 driver IC contains a 4ch H bridge driver and DC-DC converter control circuit, and was developed for portable CD players. The package in use is QFP-44, making it ideal for smaller set.

❖ **Block Diagram**



❖ **Pin Configuration**



Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	BSEN	12	VSYS1	23	BRAKE1	34	AMUTE
2	BATT	13	OPOUT	24	OUT4R	35	EMP
3	RESET	14	OP+	25	OUT4F	36	HV _{CC}
4	DEAD	15	VSYS2	26	OUT3R	37	PSW
5	SW	16	Vref	27	OUT3F	38	CLK
6	EO	17	IN3	28	POWGND	39	START
7	EI	18	IN4	29	OUT2F	40	OFF
8	SPRT	19	MUTE34	30	OUT2R	41	CHGV _{CC}
9	C _T	20	IN2	31	OUT1F	42	SEL
10	N.C.	21	MUTE2	32	OUT1R	43	PREGND
11	OP-	22	IN1	33	RCHG	44	PWMFIL

❖ *Pin Description*

Pin No.	Pin Name	I/O	Function	Internal Equivalent Circuit
1	BSEN	Input	Battery Voltage Monitor	
2	BATT	Input	Battery Power Supply Input	Power Supply
3	RESET	Output	Reset Detect Output	
4	DEAD	Input	DEAD Time Setting	
5	SW	Output	Transistor Drive For Voltage Multiplier	
6	EO	Output	Error Amplifier Output	

Pin No.	Pin Name	I/O	Function	Internal Equivalent Circuit
7	EI	Input	Error Amplifier Input	
8	SPRT	Output	Short Circuit Protection Setting	
9	CT	Output	Triangular-Wave Output	
10	N.C.			
11 14	OP- OP+	Input	Op Amp Negative Input Op Amp Positive Input	
12	VSYS1	Input	Control Circuit Power Supply Input	Control Circuit Power Supply
13	OPOUT	Output	Op Amp Output	

Pin No.	Pin Name	I/O	Function	Internal Equivalent Circuit
15	VSYS2	Input	Driver Pre-step Power Supply	Pre-Drive Power Supply
16	Vref	Input	Reference Voltage Input	
17	IN3	Input	CH3 Control Signal Input	
18	IN4		CH4 Control Signal Input	
20	IN2		CH2 Control Signal Input	
22	IN1		CH1 Control Signal Input	
19	MUT34	Input	CH3 and 4 Mute	
21	MUT2		CH2 Mute	
23	BRAKE1		CH1 Brake	
24	OUT4R	Output	CH4 Negative Output	
25	OUT4F		CH4 Positive Output	
26	OUT3R		CH3 Negative Output	
27	OUT3F		CH3 Positive Output	
29	OUT2F		CH2 Positive Output	
30	OUT2R		CH2 Negative Output	
31	OUT1F		CH1 Positive Output	
32	OUT1R		CH1 Negative Output	
28	POWGND		Power Block Power Supply Ground	
36	HV _{CC}	Input	H-Bridge Power Supply Input	

Pin No.	Pin Name	I/O	Function	Internal Equivalent Circuit
33	RCHG	Input	Charge Current Setting	
34	AMUTE	Output	Reset Invert Output	
35	EMP	Output	Empty Detect Output	
37	PSW	Output	PWM Transistor Drive	
38	CLK	Input	External Clock Synchronizing Input	

Pin No.	Pin Name	I/O	Function	Internal Equivalent Circuit
39	START	Input	Voltage Multiplier DC-DC Converter Start	
40	OFF	Input	Voltage Multiplier DC-DC Converter OFF	
41	CHGV _{CC}	Input	Charging Circuit Power Supply Input	Charging Circuit Power Supply
42	SEL	Input Output	Empty Detect Level Switch	
43	PREGND		Pre Section Power Supply	Pre Section Power Supply Ground
44	PWMFIL	Input	PWM Phase Compensation	

* The positive and negative outputs are the polarity with respect to the input

❖ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	$V_{CC} *1$	13.5	V
Driver Output Current	I_O	500	mA
Power Dissipation	P_d	625 *2	mW
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

*1 V_{cc} shows input voltage of VSYS1, VSYS2, HV_{CC}, BATT, and CHGV_{CC}.

*2 Reduced by 5mW for each increase in Ta of 1°C over 25°C

❖ Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Control Circuit Power Supply Voltage	VSYS1	2.7	3.2	5.5	V
Pre-Driver Circuit Power Supply Voltage	VSYS2	2.7	3.2	5.5	V
H-Bridge Power Supply Voltage	HVcc		PWM	BATT	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Charging Circuit Power Supply Voltage	CHGVcc	3.0	4.5	8.0	V
Operating Temperature	Ta	-10	25	70	°C

❖ Electrical Characteristics

(unless otherwise specified, Ta=25°C, BATT=2.4V, VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
< Common Section >						
BATT Stand-by Current	I_{ST}	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No load)	I_{BAT}	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No load)	I_{SYS1}	HVcc=0.45V, MUTE34=3.2V, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No load)	I_{SYS2}	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No load)	I_{CGVCC}	CHGVcc=4.5V, R _{OUT} =OPEN		0.65	2.00	mA
< H-Bridge Driver Part >						
Voltage Gain ch1, ch3, ch4	G_{VC134}		12	14	16	dB
Voltage Gain ch2	G_{VC2}		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔG_{VC}		-2	0	2	dB
Input pin resistance ch1, ch3, ch4	R_{IN134}	IN=1.7V and 1.8V	9	11	13	kΩ
Input pin resistance ch2	R_{IN2}	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	V_{OUT}	R _L =8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	V_{satL}	I _o =-300mA, IN=0 and 3.2V		240	400	mV
Saturation Voltage (Upper)	V_{satU}	I _o =-300mA, IN=0 and 3.2V		240	400	mV
Input Offset Voltage	V_{OI}		-8	0	8	mV
Output Offset Voltage ch1, ch3, ch4	V_{OO134}	Vref=IN=1.6V	-50	0	50	mV
Output Offset Voltage ch2	V_{OO2}	Vref=IN=1.6V	-130	0	130	mV
Dead Zone	V_{DB}		-10	0	10	mV
BRAKE1ON Threshold Voltage	V_{BRON}	IN1=1.8V	2.0			V
BRAKE1OFF Threshold Voltage	V_{BROFF}	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	V_{M2ON}	IN2=1.8V	2.0			V

❖ Electrical Characteristics

(unless otherwise specified, Ta=25°C, BATT=2.4V, VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
< H-Bridge Driver Part >						
MUTE2 OFF Threshold Voltage	V _{M2OFF}	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	V _{M34ON}	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V _{M34OFF}	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	V _{refON}	IN1=IN2=IN3=IN4=1.8V	1.2			V
Vref OFF Threshold Voltage	V _{refOFF}	IN1=IN2=IN3=IN4=1.8V			0.8	V
BRAKE1 Brake Current	I _{BRAKE1}	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
< PWM Power Supply Driving >						
PSW Sink Current	I _{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V _{SHIF}	IN1=1.8V, HVcc=OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I _{HLK}	HVcc=9.0V, VSYS1=VSYS2=BATT=0V		0	5	μA
PWM Amp Transfer Gain	G _{PWM}	IN1=1.8V, HVcc=1.2~1.4V	1/60	1/50	1/40	1/kΩ
< DC-DC Converter >						
< Error Amp >						
VSYS1 Threshold Voltage	V _{S1TH}		3.05	3.20	3.35	V
EO Pin Output Voltage "H"	V _{EOH}	EI=0.7V, Io=-100μA	1.4	1.6		V
EO Pin Output Voltage "L"	V _{EOL}	EI=1.3V, Io=100μA			0.3	V
< Short Circuit Protection >						
SPRT Pin Voltage	V _{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I _{SPR1}	EI=0.7V	6	10	16	μA
OFF=L SPRT Pin Current2	I _{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA
SPRT Pin Current3 Over-Voltage	I _{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA
SPRT Pin Impedance	R _{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V _{SPTH}	EI=0.7V, C _T =0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V _{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
< Transistor Driving >						
SW Pin Output Voltage1 "H"	V _{SW1H}	BATT= C _T =1.5V, VSYS1=VSYS2=0V, IO=-2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage 2 "H"	V _{SW2H}	C _T =0V, IO=-10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage 2 "L"	V _{SW2L}	C _T =2.0V, IO=10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f _{SW1}	C _T =470pF, VSYS1=VSYS2=0V Starting Time	65	80	95	kHz
SW Pin Oscillating Frequency2	f _{SW2}	C _T =470pF, CLK=0mA	60	70	82	kHz
SW Pin Oscillating Frequency3	f _{SW3}	C _T =470pF		88.2		kHz
SW Pin Minimum Pulse Width	T _{SWmin}	C _T =470pF, EO=0.5V → 0.7V Sweep	0.01		0.60	μs
Pulse Duty Start	D _{SW1}	C _T =470pF, VSYS1=VSYS2=0V	40	50	60	%
Max.Pulse Duty At Self-Running	D _{SW2}	C _T =470pF, EI=0.7V, CLK=0V	70	80	90	%
Max.Pulse Duty At CLK Synchronization	D _{SW3}	C _T =470pF, EI=0.7V	65	75	85	%

❖ Electrical Characteristics

(unless otherwise specified, $T_a=25^\circ\text{C}$, $BATT=2.4\text{V}$, $VSYS1=VSYS2=3.2\text{V}$, $V_{ref}=1.6\text{V}$, $CHGV_{cc}=0\text{V}$, $f_{CLK}=88.2\text{kHz}$)

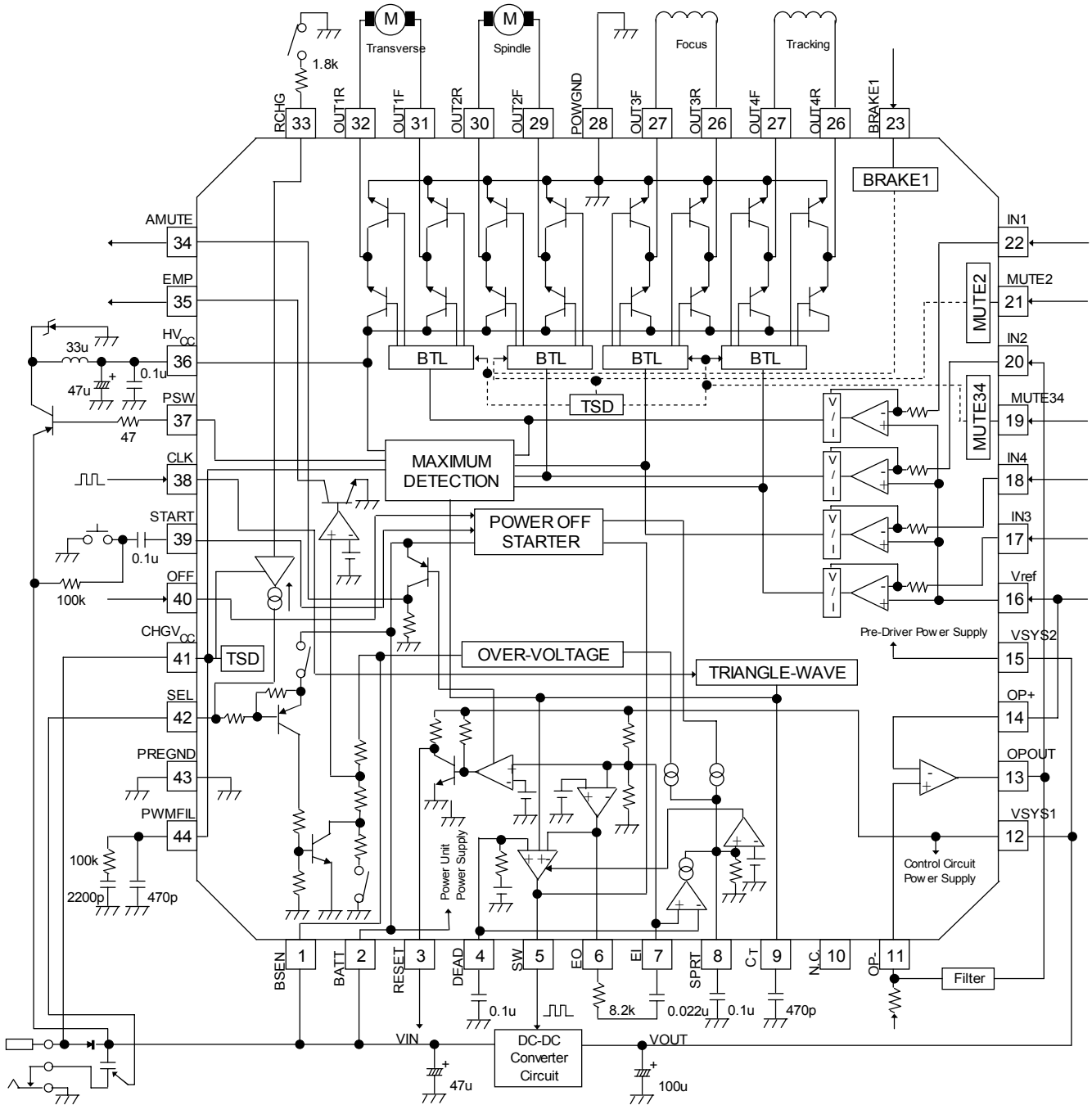
Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
< Interface >						
OFF Pin Threshold Voltage	V_{OFFTH}	EI=1.3V			$VSYS1 - 2.0$	V
OFF Pin Bias Current	I_{OFF}	OFF=0V	75	95	115	μA
START Pin ON Threshold Voltage	V_{SATH1}	$VSYS1=VSYS2=0\text{V}$, $C_T=2.0\text{V}$			BATT -1.0	V
START Pin OFF Threshold Voltage	V_{SATH2}	$VSYS1=VSYS2=0\text{V}$, $C_T=2.0\text{V}$	BATT -0.3			V
START Pin Bias Current	I_{START}	START=0V	10	20	30	μA
			13	16	19	
CLK Pin Threshold Voltage "H"	V_{CLKTHH}		2.0			V
CLK Pin Threshold Voltage "L"	V_{CLKTHL}				0.8	V
CLK Pin Bias Current	I_{CLK}	CLK=3.2V			10	μA
< Dead Time >						
DEAD Pin Impedance	R_{DEAD}		52	65	78	$\text{k}\Omega$
DEAD Pin Output Voltage	V_{DEAD}		0.78	0.88	0.98	V
< Starter Circuit >						
Starter Switching Voltage	V_{STNM}	$VSYS1=VSYS2=0\text{V} \rightarrow 3.2\text{V}$, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SNHS}	START=0V	130	200	300	mV
Discharge Release	V_{DIS}		1.63	1.83	2.03	V
< Empty Detection >						
EMP Detection Voltage 1	V_{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage 2	V_{EMPT2}	ISEL=-2 μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage1	V_{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage2	V_{EMHS2}	ISEL=-2 μA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	$I_o=1\text{mA}$, BSEN=1V			0.5	V
EMP Pin Output Leak Current	I_{EMPL}	BSEN=2.4V			1.0	μA
BSEN Pin Input Resistance	R_{BSEN}	VSEL=0V	17	23	27	$\text{k}\Omega$
BSEN Pin Leak Current	I_{BSENL}	$VSYS1=VSYS2=0\text{V}$, BSEN=4.5V			1.0	μA
SEL Pin Detection Voltage	V_{SELTH}	$V_{SELTH}=BATT-SEL$, BSEN=2.0V	1.5			V
SEL Pin Detection Current	I_{SELT}		-2			μA
< Reset Circuit >						
VSYS1 RESET Threshold Voltage Ratio	H_{SRT}	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}		25	50	100	mV
RESET Pin Output Voltage	V_{RST}	$I_o=1\text{mA}$, $VSYS1=VSYS2=2.8\text{V}$			0.5	V
RESET Pin Pull Up Resistance	R_{RST}		72	90	108	$\text{k}\Omega$
AMUTE Pin Output Voltage 1	V_{AMT1}	$I_o=-1\text{mA}$, $VSYS1=VSYS2=2.8\text{V}$	BATT -04		BATT	V
AMUTE Pin Output Voltage 2	V_{AMT2}	$I_o=-1\text{mA}$, START=0V, $VSYS1=VSYS2=0\text{V}$	BATT -04		BATT	V
AMUTE Pin Pull DOWN Resistance	R_{AMT}		77	95	113	$\text{k}\Omega$

❖ Electrical Characteristics

(unless otherwise specified, $T_a=25^\circ\text{C}$, $BATT=2.4\text{V}$, $VSYS1=VSYS2=3.2\text{V}$, $V_{ref}=1.6\text{V}$, $CHGV_{cc}=0\text{V}$, $f_{CLK}=88.2\text{kHz}$)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
< Op Amp >						
Input Bias Current	I_{BIAS}	$OP+=1.6\text{V}$			300	nA
Input Offset Voltage	V_{OIOP}		-5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	$R_L=OPEN$	2.8			V
Low Level Output Voltage	V_{OLOP}	$R_L=OPEN$			0.2	V
Output Drive Current (Source)	I_{SOU}	50Ω GND		-6.5	-3.0	mA
Output Drive Current (Sink)	I_{SIN}	50Ω $VSYS1$	0.4	0.7		mA
Open Loop Voltage Gain	GVO	$V_{IN}=-75\text{dBV}$, $f=1\text{kHz}$		70		dB
Slew Rate	SR			0.5		V/ μs
< Battery Charging Circuit >						
RCHG Pin Bias Voltage	V_{RCHG}	$CHGV_{cc}=4.5\text{V}$, $RCHG=1.8\text{ k}\Omega$	0.71	0.81	0.91	V
RCHG Pin Output Resistance	R_{RCHG}	$CHGV_{cc}=4.5\text{V}$, $RCHG=0.5$ and 0.6V	0.75	0.95	1.2	$\text{k}\Omega$
SEL Pin Leak Current 1	I_{SELLK1}	$CHGV_{cc}=4.5\text{V}$, $RCHG=OPEN$, $BATT=4.5\text{V}$			1.0	μA
SEL Pin Leak Current 2	I_{SELLK2}	$CHGV_{cc}=0.6\text{V}$, $RCHG=1.8\text{ k}\Omega$, $BATT=4.5\text{V}$			1.0	μA
SEL Pin Saturation Voltage	V_{SELCG}	$CHGV_{cc}=4.5\text{V}$, $I_o=300\text{mA}$, $RCHG=0\text{k}\Omega$		0.45	1.00	V

❖ **Application Circuit**



Note : We shall not be liable for any trouble or damage caused by using this circuit.

❖ Circuit Operation

1. H-bridge driver block

(1) Gain setting

The driver input resistance (ch 1,3 and 4) are 11kΩ typ., ch2 is 7.5 kΩ typ. . Set the gain according to the following formula.

ch1	GV=20log	$\frac{55k}{11k+R}$	(db)
ch2			
ch3			
ch2	GV=20log	$\frac{110k}{7.5k+R}$	(db)

R: Externally-connected input

The driver output stage power supply is HV_{CC}(PIN 36), and the bridge circuit power supply is V_{SY2}(PIN 15). Connect a bypass capacitor between these two power supplies (approximately 0.1μF).

(2) Mute function

Of the four drivers, ch1 has a brake function, and the other channels have a mute function.

When BRAKE1(PIN 23) is set to high level, both ch1 outputs go low level, and the circuit enters brake mode.

When MUTE2(PIN 21) is set to high level, the ch2 output is muted.

When MUTE34(PIN 19) is set to high level, the ch3 and 4 outputs are muted.

(3) Vref drop mute

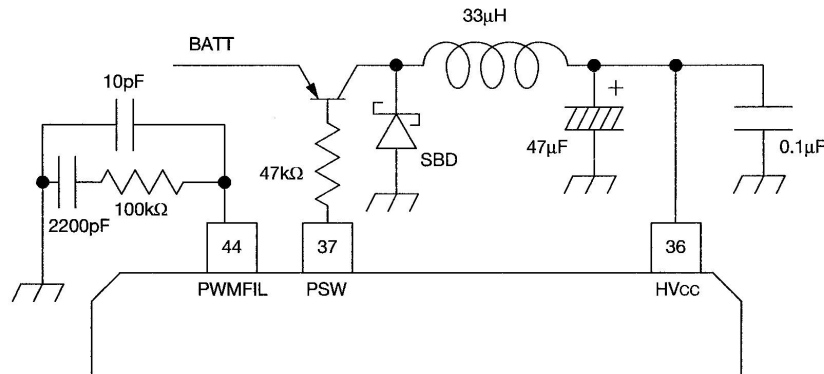
When the voltage applied to Vref(PIN16) is 1.0V or less typ., the driver outputs are set to high impedance.

(4) Thermal shutdown

When the chip temperature reaches 150°C typ., the output current is cut. The chip starts operating again at about 120°C typ. .

2. PWM power supply drive block

This detects the maximum output level from among the four channels, and supplies the load drive power supply (PIN 36) for the PWM. The external components are a PNP transistor, coil, Schottky diode, and capacitor.

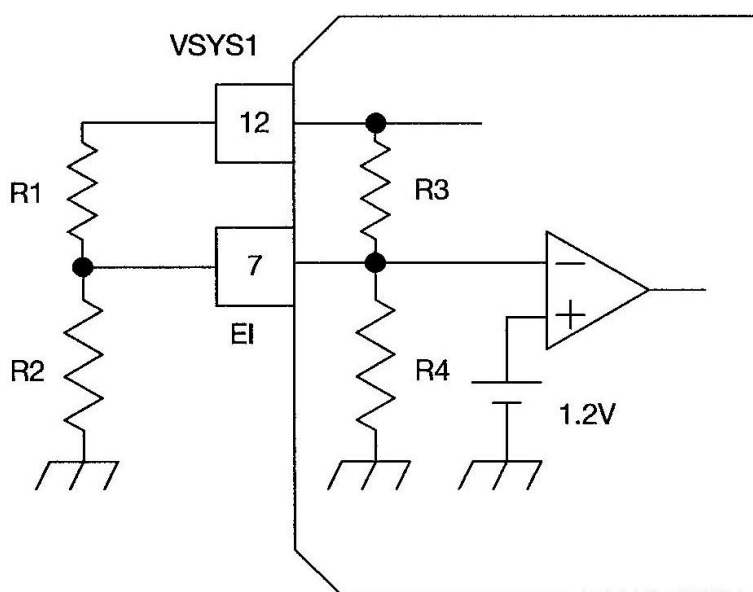


3. DC-DC converter block

(1) Output voltage

3.2V typ. Voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$V_{SYS1} = 1.2 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}} \quad (V)$$



- R1 = external resistor
- R2 = external resistor
- R3 = 35 kΩ
- R4 = 21 kΩ

(2) Short protect function

When the error amplifier output(PIN 6) has switched to the high-level state, SPRT(PIN 8) is charged, and when the voltage reaches 1.2V typ. , the SW(PIN 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT(PIN 8) according to the following formula.

$$t = C_{SPRT} \times \frac{V_{TH}}{I_{SPRT}} \text{ (sec) } (V_{TH}=1.2V, I_{SPRT}=10\mu A)$$

(3) Soft start function

The soft start function operates when a capacitor is connected between DEAD(PIN 4) and GND. Also, the maximum duty can be varied by connecting a resistor to PIN 4.

$$t = C_{DEAD} \times R \text{ (sec) } (R=65 \text{ k}\Omega)$$

(4) Power off function

When low-level is applied to OFF(PIN 40), SPRT(PIN 8) is charged, and when the voltage reaches 1.2V typ., the SW(PIN 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT(PIN 8) according to the following formula.

$$t = C_{SPRT} \times \frac{V_{TH}}{I_{OFF}} \text{ (sec) } (V_{TH}=1.2V, I_{OFF}=20\mu A)$$

(5) Over voltage protection circuit

When the voltage applied to BSEN(PIN 1) reaches 8.4V typ., SPRT(PIN 8) is charged, and when the voltage reaches 1.2V typ., the SW(PIN 5) switching stops. The time until switching stops is set by the capacitor connected to SPRT(PIN 8) according to the following formula.

$$t = C_{SPRT} \times \frac{V_{TH}}{I_{OFF}} \text{ (sec) } (V_{TH}=1.2V, I_{OFF}=20\mu A)$$

4. Empty detector block

(1) Output voltage

When the voltage applied to the BSEN(PIN 1) falls below the detector voltage, EMP(PIN 35) goes from high level to low level (open-collector output). The detector voltage has 50mV typ. of hysteresis to prevent output chattering. Use SEL(PIN 42) to switch the detection voltage as shown below.

SEL	Detect Voltage	Return Voltage
L	2.20V typ.	2.25V typ.
High-Z	1.80V typ.	1.85V typ.

5. Reset circuit block

At about 90% typ. Of the DC-DC converter output voltage, RESET(PIN 3) goes from low level to high level, and AMUTE(PIN 34) goes from high level to low level. The reset voltage has 50mV typ. of hysteresis to prevent output chattering.

6. Charging circuit block

The power supply for the charging circuit block is CHGV_{CC}(PIN 41), and is independent from the other circuits. The resistance between RCHG(PIN 33) and GND sets the charging current. This current is drawn from SEL(PIN 42).

A thermal shutdown circuit is provided, and when the chip temperature reaches 150°C typ. the charging current is cut. The chip starts operating again at about 120°C typ. .

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use.
