

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μ PD78P0308 and 78P0308Y are members of the μ PD780308 and 780308Y Subseries of the 78K/0 Series, in which the on-chip mask ROM of the μ PD780308 and 780308Y is replaced with a one-time PROM.

Because this device can be programmed by users, it is ideally suited for system evaluation, small-scale and multiple-device production, and early development and time-to-market.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD780308, 780308Y Subseries User's Manual: U11377E

78K/0 Series Instructions User's Manual: U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Program memory (one-time PROM): 60 KB^{Note}
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes
- LCD display RAM: 40 x 4 bits
- ★ Supply voltage: $V_{DD} = 2.0$ to 5.5 V

Note The internal PROM capacity can be changed by setting the internal memory size switching register (IMS).

Remark Refer to 1. DIFFERENCES BETWEEN μ PD78P0308, 78P0308Y AND MASK ROM VERSIONS for the difference between the one-time PROM and mask ROM versions.

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μ PD78P0308GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	One-time PROM
μ PD78P0308YGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	One-time PROM
μ PD78P0308GF-3BA	100-pin plastic QFP (14 × 20)	One-time PROM
μ PD78P0308YGF-3BA	100-pin plastic QFP (14 × 20)	One-time PROM

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries name.



Y subseries products are compatible with I²C bus.

Pin Count	Subseries Name	Description
Control		
100-pin	μPD78075B	EMI-noise reduced version of the μPD78078
100-pin	μPD78078	μPD78054 with timer and enhanced external interface
100-pin	μPD78070A	ROMless version of the μPD78078
100-pin	μPD780018AY	μPD78078Y with enhanced serial I/O and limited functions
80-pin	μPD780058	μPD78054 with enhanced serial I/O
80-pin	μPD78058F	EMI-noise reduced version of the μPD78054
80-pin	μPD78054	μPD78018F with UART and D/A converter, and enhanced I/O
80-pin	μPD780065	μPD780024A with expanded RAM
64-pin	μPD780078	μPD780034A with timer and enhanced serial I/O
64-pin	μPD780034A	μPD780024A with enhanced A/D converter
64-pin	μPD780024A	μPD78018F with enhanced serial I/O
52-pin	μPD780034AS	52-pin version of the μPD780034A
52-pin	μPD780024AS	52-pin version of the μPD780024A
64-pin	μPD78014H	EMI-noise reduced version of the μPD78018F
64-pin	μPD78018F	Basic subseries for control
64-pin	μPD78018FY	Basic subseries for control
42/44-pin	μPD78083	On-chip UART, capable of operating at low voltage (1.8 V)
Inverter control		
64-pin	μPD780988	On-chip inverter controller and UART. EMI-noise reduced.
VFD drive		
100-pin	μPD780208	μPD78044F with enhanced I/O and VFD C/D. Display output total: 53
80-pin	μPD780232	For panel control. On-chip VFD C/D. Display output total: 53
80-pin	μPD78044H	μPD78044F with N-ch open-drain I/O. Display output total: 34
80-pin	μPD78044F	Basic subseries for driving VFD. Display output total: 34
LCD drive		
100-pin	μPD780354	μPD780344 with enhanced A/D converter
100-pin	μPD780344	μPD780308 with enhanced display function and timer. Segment signal output: 40 pins max.
120-pin	μPD780338	μPD780308 with enhanced display function and timer. Segment signal output: 40 pins max.
120-pin	μPD780328	μPD780308 with enhanced display function and timer. Segment signal output: 32 pins max.
120-pin	μPD780318	μPD780308 with enhanced display function and timer. Segment signal output: 24 pins max.
100-pin	μPD780308	μPD78064 with enhanced SIO, and expanded ROM and RAM
100-pin	μPD78064B	EMI-noise reduced version of the μPD78064
100-pin	μPD78064	Basic subseries for driving LCDs, on-chip UART
Bus interface supported		
100-pin	μPD780948	On-chip CAN controller
80-pin	μPD78098B	μPD78054 with IEBus™ controller
80-pin	μPD780702Y	On-chip IEBus controller
80-pin	μPD780703AY	On-chip CAN controller
80-pin	μPD780833Y	On-chip controller compliant with J1850 (Class 2)
64-pin	μPD780816	Specialized for CAN controller function
Meter control		
100-pin	μPD780958	For industrial meter control
80-pin	μPD780852	On-chip automobile meter controller/driver
80-pin	μPD780828B	For automobile meter driver. On-chip CAN controller

Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences between the subseries are shown below.

• Subseries without the suffix Y

Subseries Name	Function	ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion	
			8-Bit	16-Bit	Watch	WDT								
Control	μPD78075B	32 KB to 40 KB	4 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Yes	
	μPD78078	48 KB to 60 KB									61	2.7 V		
	μPD78070A	-									61	2.7 V		
	μPD780058	24 KB to 60 KB	2 ch	-	-	-	-	-	-	3 ch (time-division UART: 1 ch)	68	1.8 V	-	
	μPD78058F	48 KB to 60 KB									69	2.7 V		
	μPD78054	16 KB to 60 KB									69	2.0 V		
	μPD780065	40 KB to 48 KB									60	2.7 V		
	μPD780078	48 KB to 60 KB									52	1.8 V		
	μPD780034A	8 KB to 32 KB									51			
	μPD780024A										39			
	μPD780034AS										39			
	μPD780024AS										39			
	μPD78014H										53			
	μPD78018F	8 KB to 60 KB	53											
	μPD78083	8 KB to 16 KB	33											
Inverter control	μPD780988	16 KB to 60 KB	3 ch	Note	-	1 ch	-	8 ch	-	3 ch (UART: 2 ch)	47	4.0 V	Yes	
VFD drive	μPD780208	32 KB to 60 KB	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	2 ch	74	2.7 V	-	
	μPD780232	16 KB to 24 KB	3 ch	-	-	-	4 ch	-	-	2 ch	40	4.5 V		
	μPD78044H	32 KB to 48 KB	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	1 ch	68	2.7 V		
	μPD78044F	16 KB to 40 KB	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	2 ch	68	2.7 V		
LCD drive	μPD780354	24 KB to 32 KB	4 ch	1 ch	1 ch	1 ch	-	8 ch	-	3 ch (UART: 1 ch)	66	1.8 V	-	
	μPD780344						8 ch	-						
	μPD780338	48 KB to 60 KB	3 ch	2 ch	-	-	-	-	-	2 ch (UART: 1 ch)	54	-		
	μPD780328										62			
	μPD780318										70			
	μPD780308	48 KB to 60 KB	2 ch	1 ch	-	-	-	-	-	3 ch (time-division UART: 1 ch)	57	2.0 V		
	μPD78064B	32 KB												2 ch (UART: 1 ch)
	μPD78064	16 KB to 32 KB												
Bus interface supported	μPD780948	60 KB	2 ch	2 ch	1 ch	1 ch	8 ch	-	-	3 ch (UART: 1 ch)	79	4.0 V	Yes	
	μPD78098B	40 KB to 60 KB		1 ch							69	2.7 V		-
	μPD780816	32 KB to 60 KB		2 ch							12 ch	46		
Meter control	μPD780958	48 KB to 60 KB	4 ch	2 ch	-	1 ch	-	-	-	2 ch (UART: 1 ch)	69	2.2 V	-	
Dashboard control	μPD780852	32 KB to 40 KB	3 ch	1 ch	1 ch	1 ch	5 ch	-	-	3 ch (UART: 1 ch)	56	4.0 V	-	
	μPD780828B	32 KB to 60 KB									59			

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

• Subseries with the suffix Y

Function Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion	
			8-Bit	16-Bit	Watch	WDT								
Control	μPD78078Y	48 KB to 60 KB	4 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART: 1 ch, I ² C: 1 ch)	88	1.8 V	Yes	
	μPD78070AY	-									61	2.7 V		
	μPD780018AY	48 KB to 60 KB								2 ch	-	3 ch (I ² C: 1 ch)		88
	μPD780058Y	24 KB to 60 KB	3 ch (time-division UART: 1 ch, I ² C: 1 ch)	68										
	μPD78058FY	48 KB to 60 KB		3 ch (UART: 1 ch, I ² C: 1 ch)	69									
	μPD78054Y	16 KB to 60 KB	2.0 V											
	μPD780078Y	48 KB to 60 KB	2 ch	-	8 ch	-	4 ch (UART: 2 ch, I ² C: 1 ch)	52	1.8 V					
	μPD780034AY	8 KB to 32 KB	1 ch	3 ch (UART: 1 ch, I ² C: 1 ch)	8 ch	-	51							
	μPD780024AY	8 KB to 60 KB												
μPD78018FY	8 KB to 60 KB	2 ch (I ² C: 1 ch)	53											
LCD drive	μPD780354Y	24 KB to 32 KB	4 ch	1 ch	1 ch	1 ch	-	8 ch	-	4 ch (UART: 1 ch, I ² C: 1 ch)	66	1.8 V	-	
	μPD780344Y	48 KB to 60 KB					8 ch	-						
	μPD780308Y	48 KB to 60 KB	2 ch	3 ch (time-division UART: 1 ch, I ² C: 1 ch)	57	2.0 V								
	μPD78064Y	16 KB to 32 KB					2 ch (UART: 1 ch, I ² C: 1 ch)							
Bus interface supported	μPD780702Y	60 KB	3 ch	2 ch	1 ch	1 ch	16 ch	-	-	4 ch (UART: 1 ch, I ² C: 1 ch)	67	3.5 V	-	
	μPD780703AY	59.5 KB												
	μPD780833Y	60 KB									65	4.5 V		

Remark The functions of the subseries without the suffix Y and the subseries with the suffix Y are the same, except for the serial interface (if a subseries without the suffix Y is available).

OVERVIEW OF FUNCTIONS

Item		μPD78P0308	μPD78P0308Y
Internal memory	One-time PROM	60 KB ^{Note}	
	High-speed RAM	1024 bytes	
	Expansion RAM	1024 bytes	
	LCD display RAM	40 x 4 bits	
General-purpose registers		8 bits x 32 registers (8 bits x 8 registers x 4 banks)	
Minimum instruction execution time		On-chip minimum instruction execution time variable function	
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz operation)	
	When subsystem clock is selected	122 μs (@ 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc. 	
I/O ports (Segment signal output pins included)		Total: 57 <ul style="list-style-type: none"> • CMOS input: 2 • CMOS I/O: 55 	
A/D converter		8-bit resolution x 8 channels	
LCD controller/driver		<ul style="list-style-type: none"> • Segment signal output: 40 pins maximum • Common signal output: 4 pins maximum • Bias: 1/2, 1/3 bias convertible 	
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel 	<ul style="list-style-type: none"> • 3-wire serial I/O/2-wire serial I/O/I²C bus mode selectable: 1 channel
		<ul style="list-style-type: none"> • 3-wire serial I/O/UART mode selectable: 1 channel • 3-wire serial I/O mode: 1 channel 	
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel 	
Timer output		3 pins (14-bit PWM output enable: 1 pin)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0 MHz operation with main system clock) 32.768 kHz (@ 32.768 kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0 MHz operation with main system clock)	

Note The internal PROM capacity can be changed by setting the internal memory size switching register (IMS).

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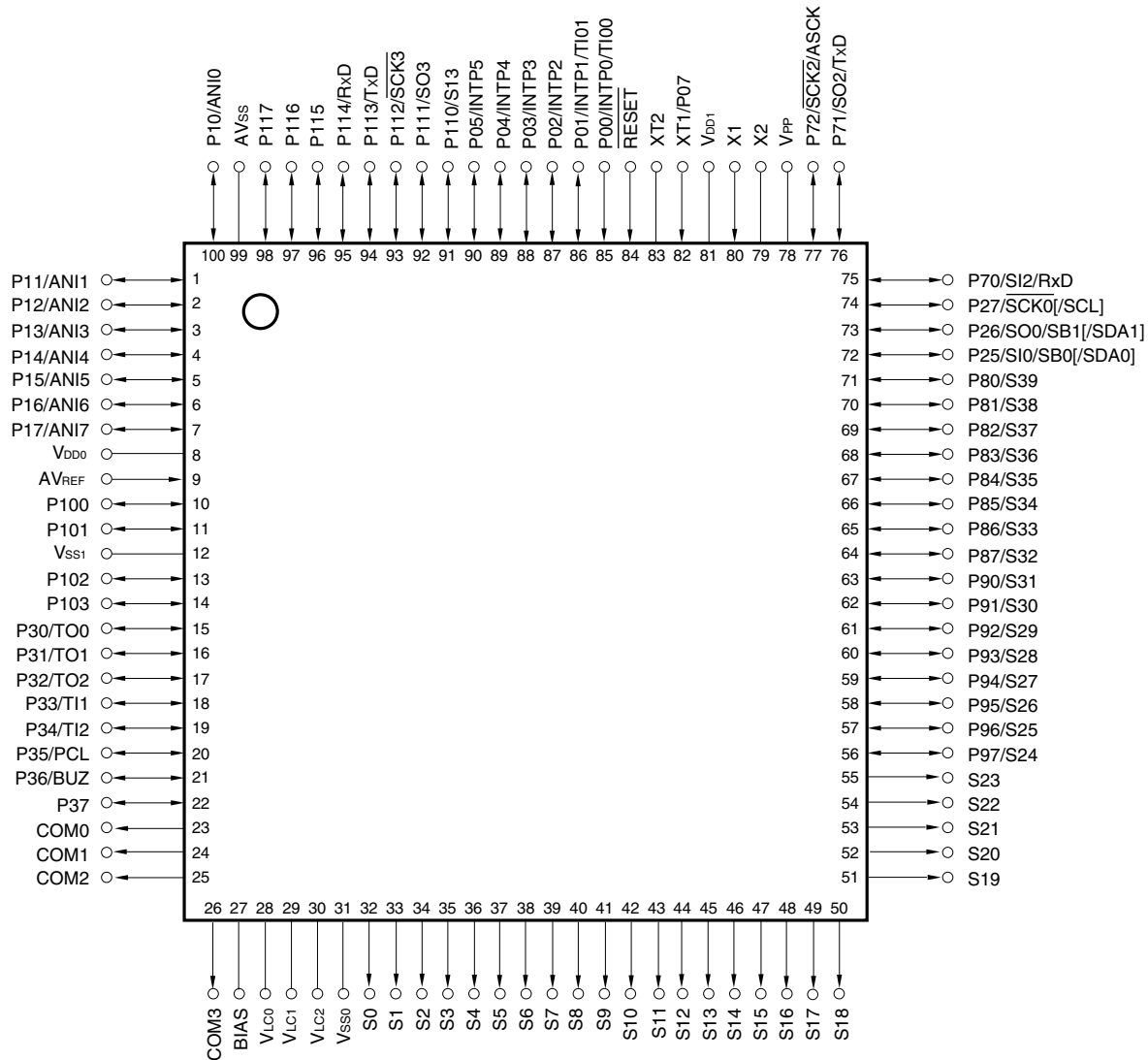
Item		μPD78P0308	μPD78P0308Y
Vectored interrupt sources	Maskable	Internal: 13, External: 6	
	Non-maskable	Internal: 1	
	Software	1	
Test input		Internal: 1, External: 1	
Supply voltage		V _{DD} = 2.0 to 5.5 V	
Package		<ul style="list-style-type: none"> • 100-pin plastic LQFP (fine pitch) (14 × 14) • 100-pin plastic QFP (14 × 20) 	

PIN CONFIGURATIONS (TOP VIEW)

(1) Normal operating mode

• 100-pin plastic LQFP (fine pitch) (14 × 14)

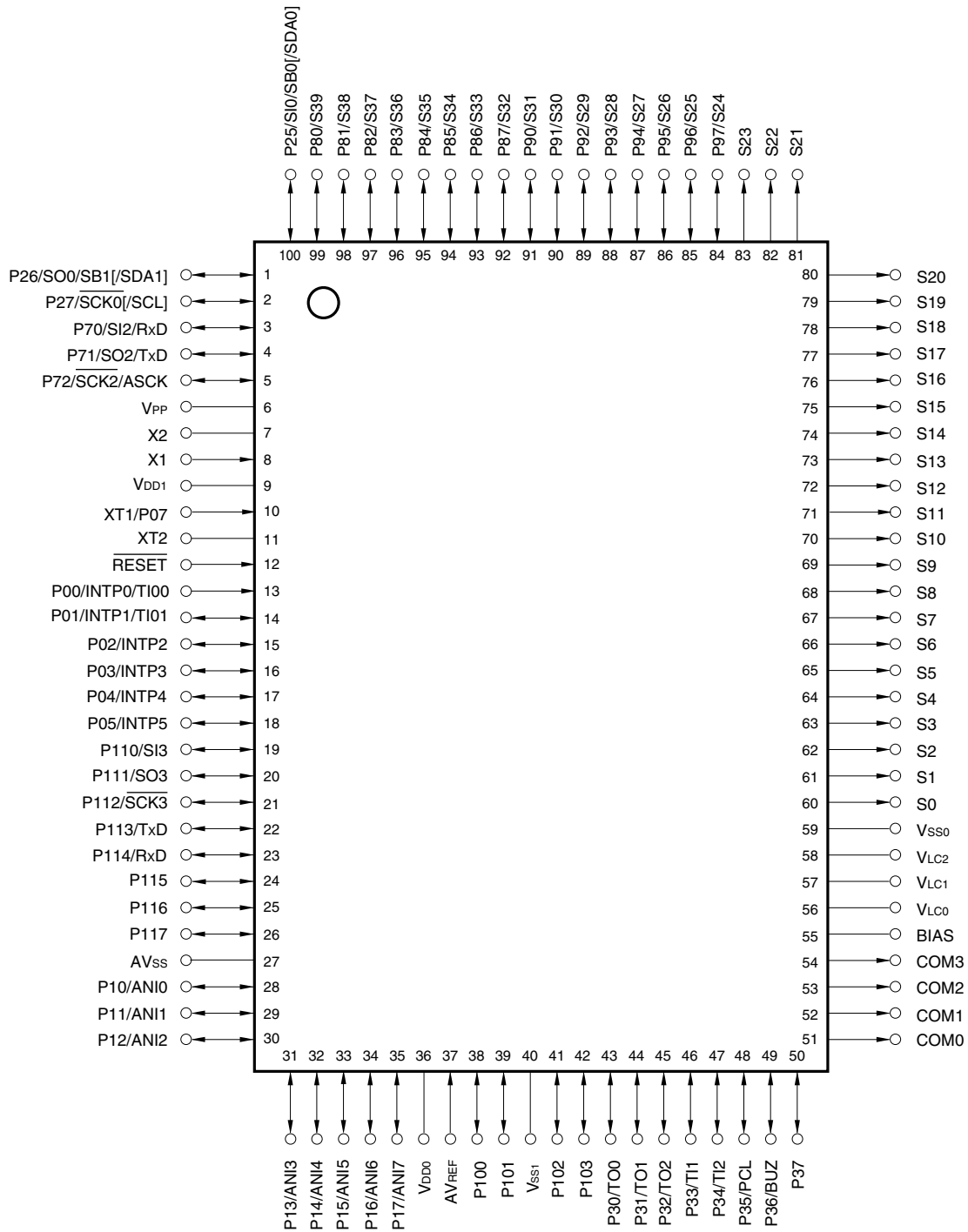
μPD78P0308GC-8EU, 78P0308YGC-8EU



- Cautions**
1. Connect the VPP pin directly to VSS0 or VSS1.
 2. Connect the AVss pin to VSS0.

- Remarks**
1. []: μPD78P0308Y only
 2. When the device is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to VDD0 and VDD1 individually and connecting VSS0 and VSS1 to different ground lines, is recommended.

- 100-pin plastic QFP (14 × 20)
- μPD78P0308GF-3BA, 78P0308YGF-3BA



- Cautions**
1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1}.
 2. Connect the AV_{SS} pin to V_{SS0}.

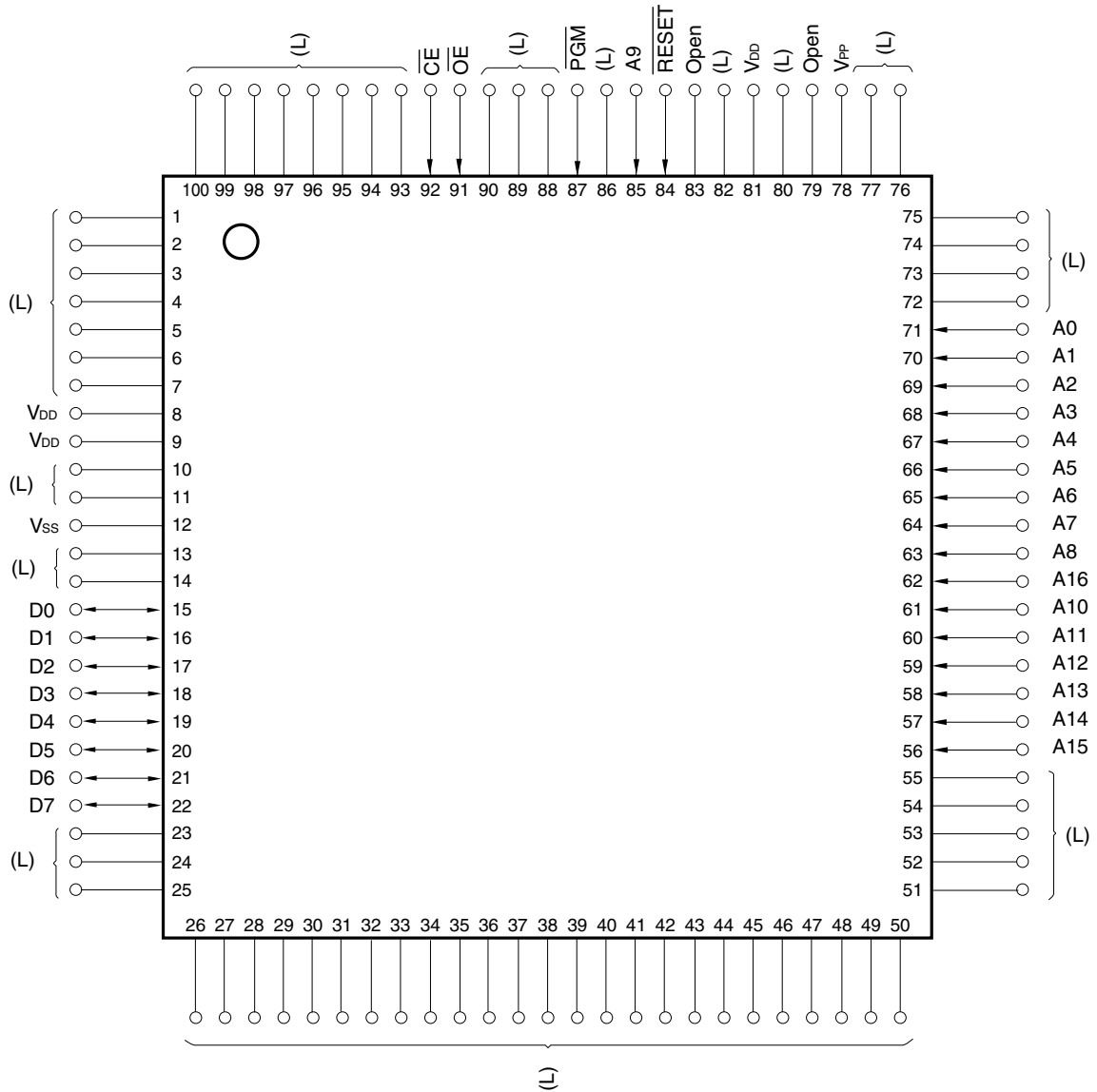
Remarks 1. []: μPD78P0308Y only

2. When the device is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI7:	Analog input	RxD:	Receive data
ASCK:	Asynchronous serial clock	S0 to S39:	Segment output
AVREF:	Analog reference voltage	SB0, SB1:	Serial bus
AVss:	Analog ground	$\overline{\text{SCK0}}, \overline{\text{SCK2}}, \overline{\text{SCK3}}$:	Serial clock
BIAS:	LCD power supply bias control	SCL:	Serial clock
BUZ:	Buzzer clock	SDA0, SDA1:	Serial data
COM0 to COM3:	Common output	SI0, SI2, SI3:	Serial input
INTP0 to INTP5:	External interrupt input	SO0, SO2, SO3:	Serial output
P00 to P05, P07:	Port 0	TI00, TI01:	Timer input
P10 to P17:	Port 1	TI1, TI2:	Timer input
P25 to P27:	Port 2	TO0 to TO2:	Timer output
P30 to P37:	Port 3	TxD:	Transmit data
P70 to P72:	Port 7	VDD0, VDD1:	Power supply
P80 to P87:	Port 8	VLC0 to VLC2:	LCD power supply
P90 to P97:	Port 9	VPP:	Programming power supply
P100 to P103:	Port 10	VSS0, VSS1:	Ground
P110 to P117:	Port 11	X1, X2:	Crystal (main system clock)
PCL:	Programmable clock	XT1, XT2:	Crystal (subsystem clock)
$\overline{\text{RESET}}$:	Reset		

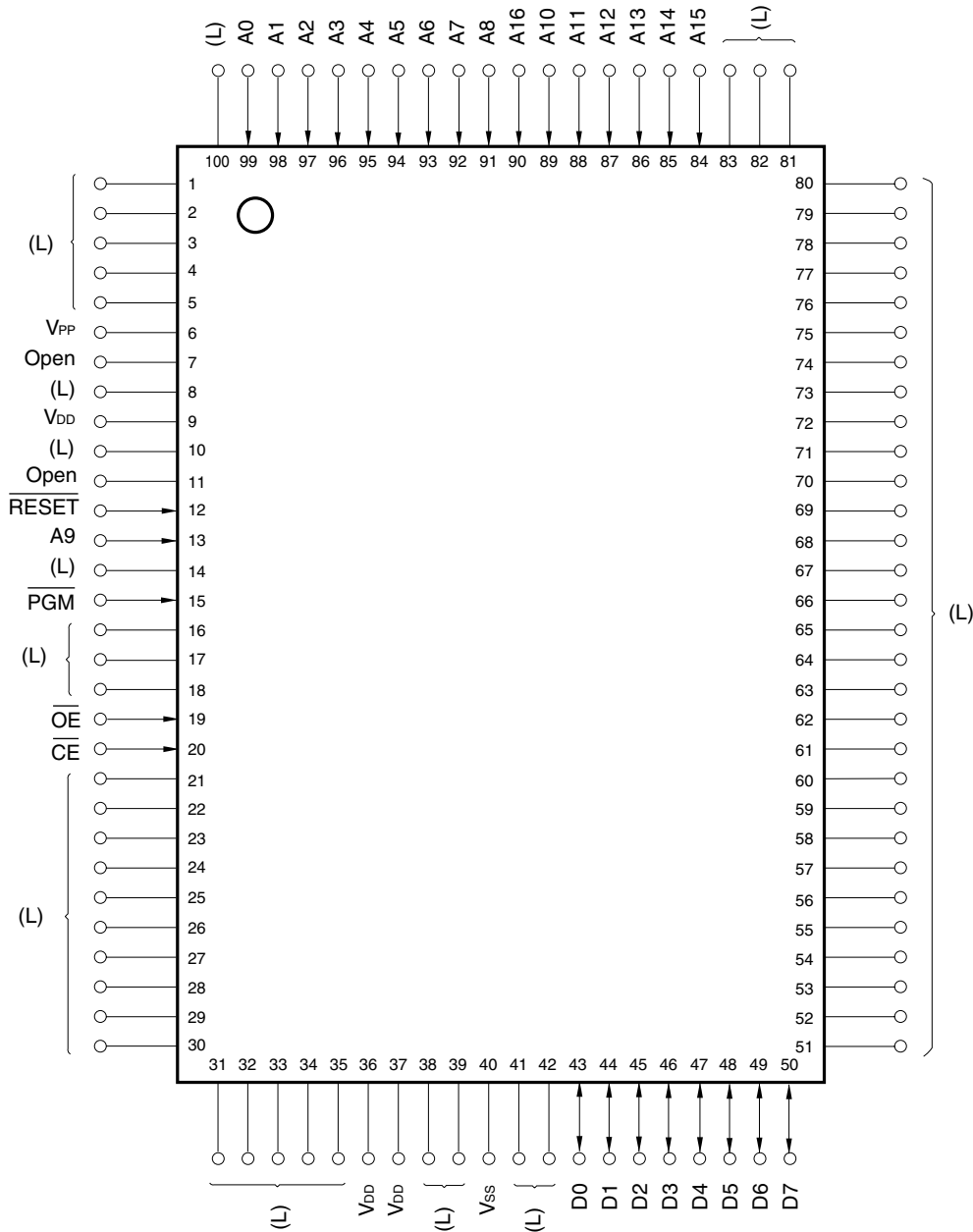
(2) PROM programming mode

- 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD78P0308GC-8EU, 78P0308YGC-8EU



- Cautions**
1. (L): Independently connect to Vss via a pull-down resistor.
 2. Vss: Connect to GND.
 3. $\overline{\text{RESET}}$: Set to low level.
 4. Open: Leave open.

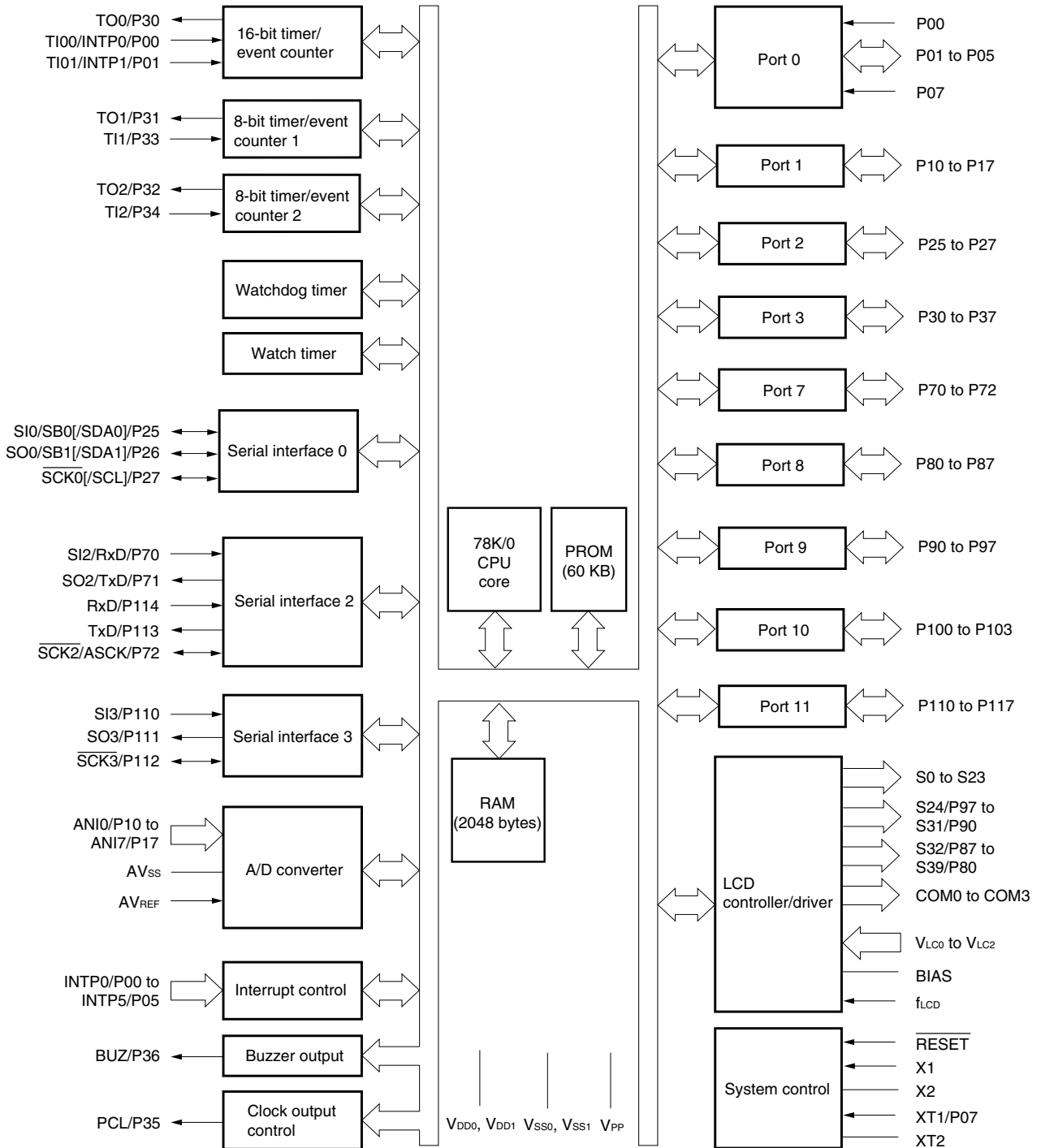
- 100-pin plastic QFP (14 × 20)
μPD78P0308GF-3BA, 78P0308YGF-3BA



- Cautions**
1. (L): Independently connect to V_{ss} via a pull-down resistor.
 2. V_{ss}: Connect to GND.
 3. $\overline{\text{RESET}}$: Set to low level.
 4. Open: Leave open.

A0 to A16:	Address bus	$\overline{\text{RESET}}$:	Reset
$\overline{\text{CE}}$:	Chip enable	V _{DD} :	Power supply
D0 to D7:	Data bus	V _{PP} :	Programming power supply
$\overline{\text{OE}}$:	Output enable	V _{SS} :	Ground
PGM:	Program		

BLOCK DIAGRAM



Remark []: μPD78P0308Y only

CONTENTS

1. DIFFERENCES BETWEEN μPD78P0308, 78P0308Y AND MASK ROM VERSIONS	15
2. PIN FUNCTIONS	16
2.1 Pins in Normal Operating Mode	16
2.2 Pins in PROM Programming Mode	19
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins	20
3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)	24
4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)	25
5. PROM PROGRAMMING	26
5.1 Operating Modes	26
5.2 PROM Write Procedure	28
5.3 PROM Read Procedure	32
6. ONE-TIME PROM VERSION SCREENING	32
7. ELECTRICAL SPECIFICATIONS	33
8. PACKAGE DRAWINGS	61
★ 9. RECOMMENDED SOLDERING CONDITIONS	63
APPENDIX A. DEVELOPMENT TOOLS	64
APPENDIX B. RELATED DOCUMENTS	70

1. DIFFERENCES BETWEEN μPD78P0308, 78P0308Y AND MASK ROM VERSIONS

The μPD78P0308 and 78P0308Y are single-chip microcontrollers with an on-chip one-time PROM to which a program can be written only once.

It is possible to make all the functions except for the PROM specifications and the mask option of LCD drive power supply dividing resistor the same as those of mask ROM versions by setting the internal memory size switching register (IMS).

Differences between the one-time PROM versions (μPD78P0308, 78P0308Y) and mask ROM versions (μPD780306, 780308, 780306Y, 780308Y) are shown in Table 1-1.

Table 1-1. Differences Between μPD78P0308, 78P0308Y and Mask ROM Versions

Item	μPD78P0308	μPD78P0308Y	Mask ROM Versions	
			μPD780308 Subseries	μPD780308Y Subseries
Internal ROM configuration	One-time PROM		Mask ROM	
Internal ROM capacity	60 KB		μPD780306, 780306Y: 48 KB μPD780308, 780308Y: 60 KB	
Internal ROM capacity change by the internal memory size switching register (IMS)	Possible ^{Note}		Impossible	
IC pin	No		Yes	
V _{PP} pin	Yes		No	
Mask options of LCD drive power supply dividing resistor	None		Available	
Serial interface (SBI)	Provided	Not provided	Provided	Not provided
Serial interface (I ² C)	Not provided	Provided	Not provided	Provided
Electrical specifications, recommended soldering conditions	Refer to the data sheet of the individual product.			

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Note The internal PROM capacity is set to 60 KB by $\overline{\text{RESET}}$ input.

Caution There are differences in noise immunity and noise radiation between the one-time PROM and mask ROM versions. When pre-producing an application set with a one-time PROM version and then mass-producing it with a mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit I/O port	Input only	Input	INTP0/TI00
P01	I/O		Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07 ^{Note 1}	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings. ^{Note 2}	Input	ANI0 to ANI7	
P25	I/O	Port 2 3-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings.	Input	SI0/SB0[/SDA0]	
P26				SO0/SB1[/SDA1]	
P27				SCK0[/SCL]	
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	

- Notes**
1. When the P07/XT1 pin is used as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1, and be sure not to use the feedback resistor of the subsystem clock oscillator.
 2. When the P10/ANI0 to P17/ANI7 pins are used as the analog inputs for the A/D converter, shift port 1 to input mode. The on-chip pull-up resistors are automatically disabled.

Remark []: μPD78P0308Y only

(1) Port pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 3-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings.	Input	SI2/RxD
P71				SO2/TxD
P72				SCK2/ASCK
P80 to P87	I/O	Port 8 8-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings. The I/O port/segment signal output function is specifiable in 2-bit units by the LCD display control register (LCDC).	Input	S39 to S32
P90 to P97	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings. The I/O port/segment signal output function is specifiable in 2-bit units by the LCD display control register (LCDC).	Input	S31 to S24
P100 to P103	I/O	Port 10 4-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings. It is possible to directly drive LEDs.	Input	—
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units. When used as the input port, on-chip pull-up resistor connection can be specified by software settings. Falling edge detection is possible.	Input	SI3
P111				SO3
P112				SCK3
P113				TxD
P114				RxD
P115 to P117				—

(2) Non-port pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function	
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00	
INTP1				P01/TI01	
INTP2				P02	
INTP3				P03	
INTP4				P04	
INTP5				P05	
SI0	Input	Serial interface serial data input.	Input	P25/SB0[/SDA0]	
SI2				P70/RxD	
SI3				P110	
SO0	Output	Serial interface serial data output.	Input	P26/SB1[/SDA1]	
SO2				P71/TxD	
SO3				P111	
SB0	I/O	Serial interface serial data input/output.	Input	P25/SI0[/SDA0]	
SB1				P26/SO0[/SDA1]	
SDA0				μPD78P0308Y only	P25/SI0/SB0
SDA1				P26/SO0/SB1	
SCK0	I/O	Serial interface serial clock input/output.	Input	P27[/SCL]	
SCK2				P72/ASCK	
SCK3				P112	
SCL				μPD78P0308Y only	P27/SCK0
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2, P114	
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2, P113	
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2	
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0	
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1	
TI1		External count clock input to 8-bit timer (TM1).		P33	
TI2		External count clock input to 8-bit timer (TM2).		P34	
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output).	Input	P30	
TO1		8-bit timer (TM1) output.		P31	
TO2		8-bit timer (TM2) output.		P32	
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35	
BUZ	Output	Buzzer output.	Input	P36	
S0 to S23	Output	LCD controller/driver segment signal output.	Output	—	
S24 to S31			Input	P97 to P90	
S32 to S39			P87 to P80		
COM0 to COM3	Output	LCD controller/driver common signal output.	Output	—	
V _{LC0} to V _{LC2}	—	LCD drive voltage.	—	—	
BIAS	—	LCD drive power supply.	—	—	

Remark []: μPD78P0308Y only

(2) Non-port pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV _{REF}	Input	A/D converter reference voltage input (also used for analog power supply).	—	—
AV _{SS}	—	A/D converter ground potential. Set to the same potential as V _{SS0} .	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Crystal resonator connection for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Crystal resonator connection for subsystem clock oscillation.	Input	P07
XT2	—		—	—
V _{DD0}	—	Positive power supply for ports.	—	—
V _{SS0}	—	Ground potential for ports.	—	—
V _{DD1}	—	Positive power supply (except for ports and analog).	—	—
V _{SS1}	—	Ground potential (except for ports and analog).	—	—
V _{PP}	—	High voltage application in program write/verify mode. Connect directly to V _{SS0} or V _{SS1} in normal operating mode.	—	—

2.2 Pins in PROM Programming Mode

Pin Name	I/O	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V _{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode.
V _{PP}	Input	PROM programming mode setting and high voltage application during program write/verification.
A0 to A16	Input	Address bus.
D0 to D7	I/O	Data bus.
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input.
$\overline{\text{OE}}$	Input	Read strobe input to PROM.
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programming mode.
V _{DD}	—	Positive power supply.
V _{SS}	—	Ground potential.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The types of pin I/O circuits and the recommended connection of unused pins are shown in Table 2-1.

For the configuration of each type of I/O circuit, see Figure 2-1.

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Table 2-1. Type of I/O Circuit of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins	
P00/INTP0/TI00	2	Input	Connect to V _{SS0} .	
P01/INTP1/TI01	8-C	I/O	Input: Independently connect to V _{SS0} via a resistor. Output: Leave open.	
P02/INTP2				
P03/INTP3				
P04/INTP4				
P05/INTP5				
P07/XT1	16	Input	Connect to V _{DD0} .	
P10/ANI0 to P17/ANI7	11-B	I/O	Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.	
P25/SI0/SB0[/SDA0]	10-B			
P26/SO0/SB1[/SDA1]				
P27/SCK0[/SCL]				
P30/TO0	5-H			
P31/TO1				
P32/TO2				
P33/TI1	8-C			
P34/TI2				
P35/PCL	5-H			
P36/BUZ				
P37				
P70/SI2/RxD	8-C			
P71/SO2/TxD	5-H			
P72/SCK2/ASCK	8-C			
P80/S39 to P87/S32	17-C			
P90/S31 to P97/S24				
P100 to P103				
P110/SI3	8-C			Input: Independently connect to V _{DD0} via a resistor. Output: Leave open.
P111/SO3				
P112/SCK3				
P113/TxD				
P114/RxD				
P115 to P117				
S0 to S23	17-B	Output	Leave open.	
COM0 to COM3	18-A			

Remark []: μPD78P0308Y only

Table 2-1. Type of I/O Circuit of Each Pin (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
V _{LC0} to V _{LC2}	—	—	Leave open.
BIAS			
RESET	2	Input	—
XT2	16	—	Leave open.
AV _{REF}	—	—	Connect to V _{SS0} .
AV _{SS}			
V _{PP}			Connect directly to V _{SS0} or V _{SS1} .

Figure 2-1. List of Pin I/O Circuits (1/2)

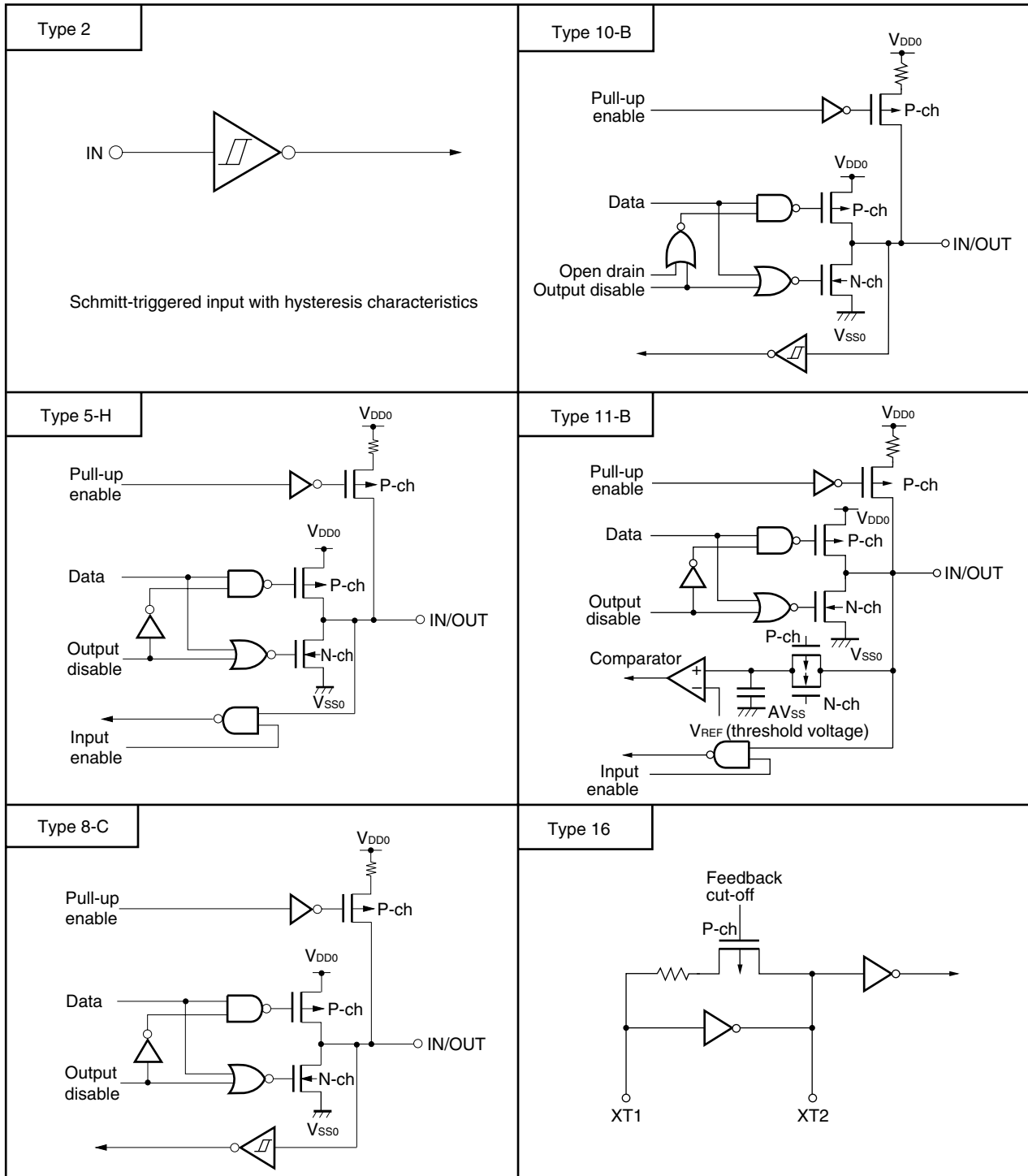
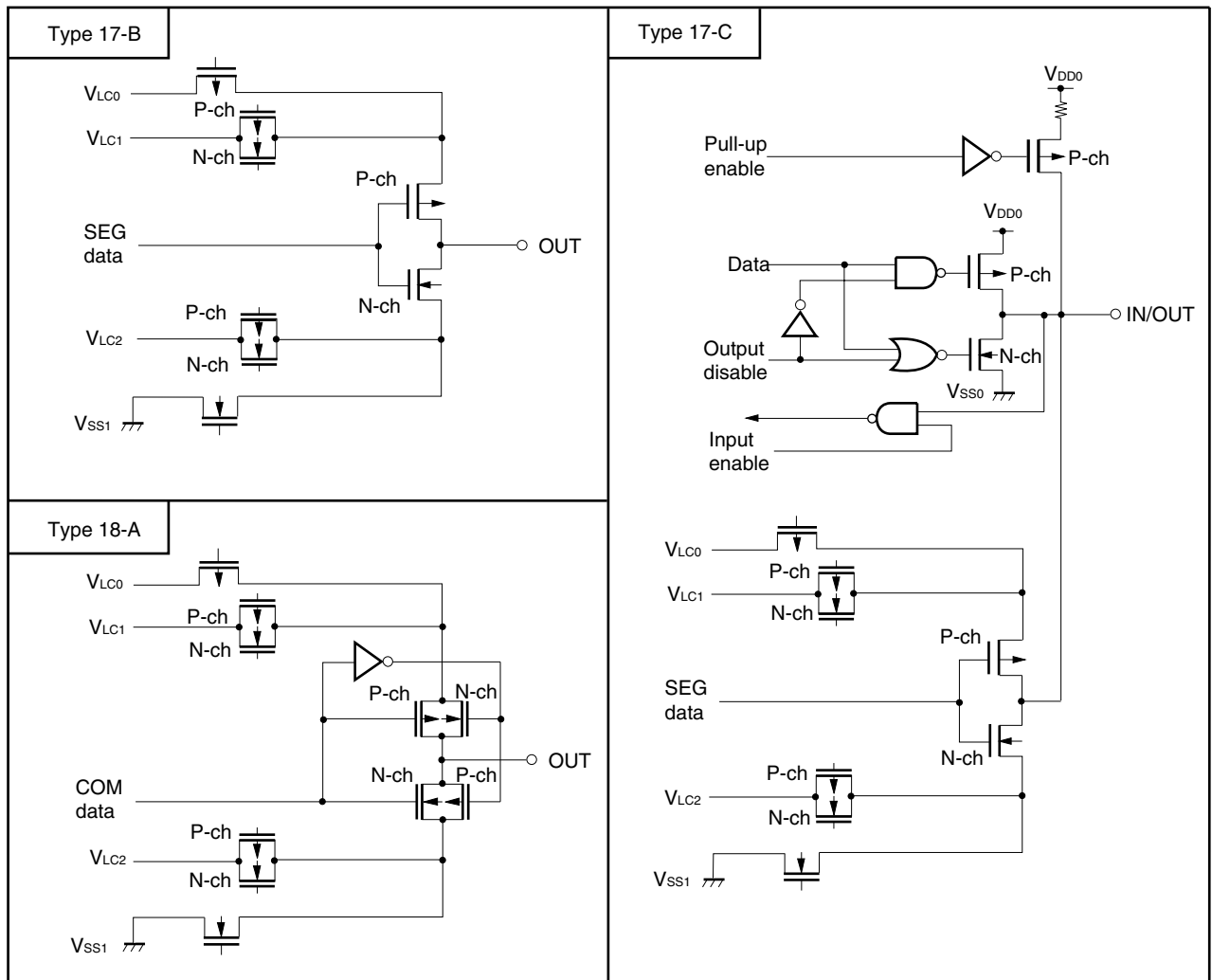


Figure 2-1. List of Pin I/O Circuits (2/2)



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register used to disable use of part of the internal memory by software. By setting the internal memory size switching register (IMS), it is possible to get the same memory map as that of the mask ROM versions with a different internal memory (ROM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Format of Internal Memory Size Switching Register

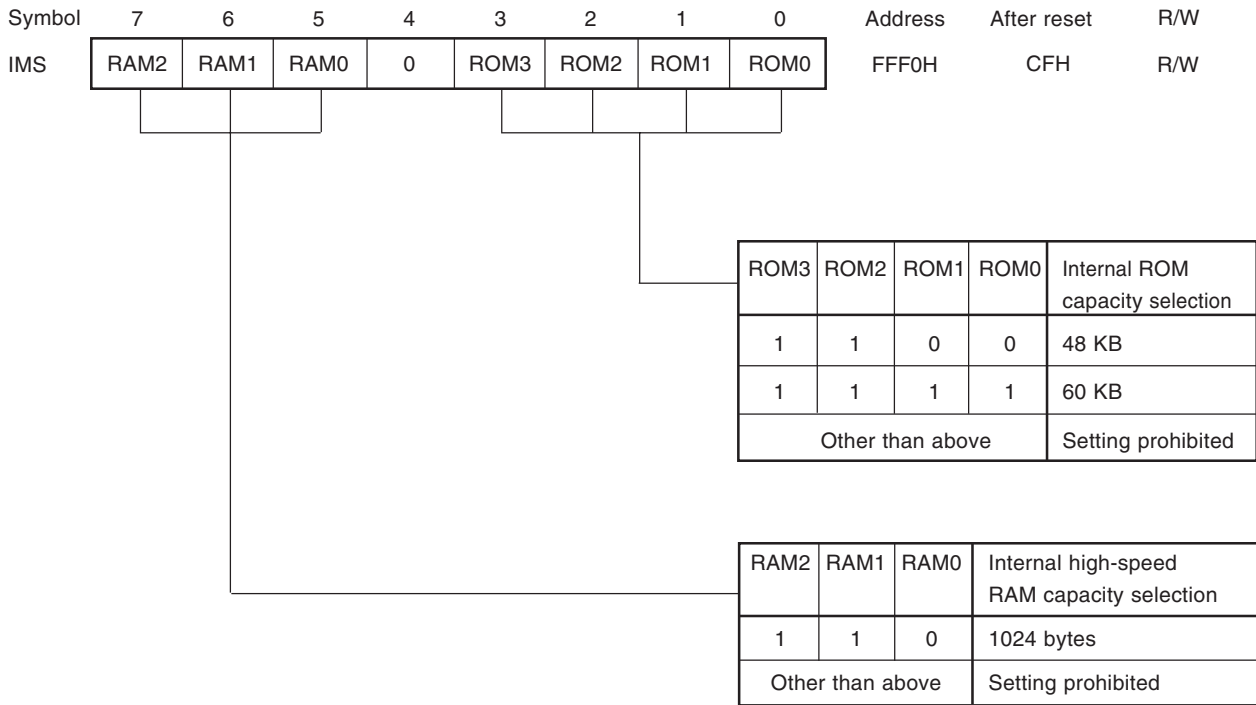


Table 3-1 shows the setting values of IMS that make the memory mapping the same as that of the mask ROM versions.

Table 3-1. Internal Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD780306, 780306Y	CCH
μPD780308, 780308Y	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set the internal expansion RAM capacity by software. By setting the internal expansion RAM size switching register (IXS), it is possible to get the same memory map as that of the mask ROM versions with a different internal expansion RAM capacity.

IXS is set with an 8-bit memory manipulation instruction.

RESET input sets IXS to 0AH.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

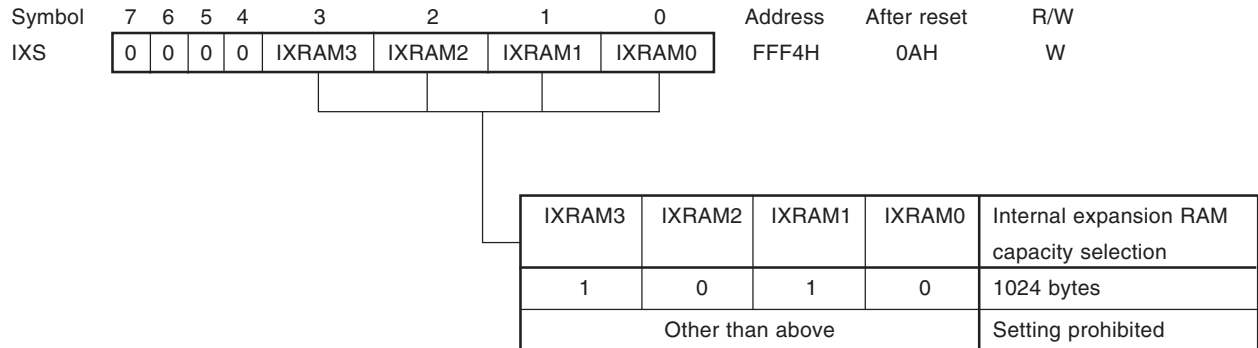


Table 4-1 shows the setting values of IXS that make the memory mapping the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting Value
μPD780306, 780306Y	0AH
μPD780308, 780308Y	

5. PROM PROGRAMMING

The μPD78P0308 and 78P0308Y have an on-chip 60 KB PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and $\overline{\text{RESET}}$ pins. For the connection of unused pins, refer to **PIN CONFIGURATIONS (2) PROM programming mode**.

Caution Programs must be written in addresses 0000H to EFFFH (the last address EFFFH must be specified). They cannot be written by a PROM programmer that cannot specify the write address.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin	$\overline{\text{RESET}}$	V _{PP}	V _{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0 to D7
Operating Mode							
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

×: L or H

(1) Read mode

Read mode is set if $\overline{CE} = L$, $\overline{OE} = L$ is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE} = H$ is set.

Therefore, data can be read from any device by controlling the \overline{OE} pin, if multiple μ PD78P0308 and 78P0308Ys are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE} = H$ is set.

In this mode, data outputs become high-impedance irrespective of the \overline{OE} status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE} = H$, $\overline{PGM} = H$, $\overline{OE} = L$ are set at the beginning of page write mode.

In this mode, 1-page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the \overline{PGM} pin with $\overline{CE} = H$, $\overline{OE} = H$. Then, program verification can be performed, if $\overline{CE} = L$, $\overline{OE} = L$ are set.

If programming is not performed by a one-time program pulse, write and verification operations should be executed X times ($X \leq 10$) repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the \overline{PGM} pin with $\overline{CE} = L$, $\overline{OE} = H$. Then, program verification can be performed if $\overline{OE} = L$ is set.

If programming is not performed by a one-time program pulse, write and verification operations should be executed X times ($X \leq 10$) repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE} = L$, $\overline{PGM} = H$, $\overline{OE} = L$ are set.

In this mode, check if the write operation was performed correctly after the write.

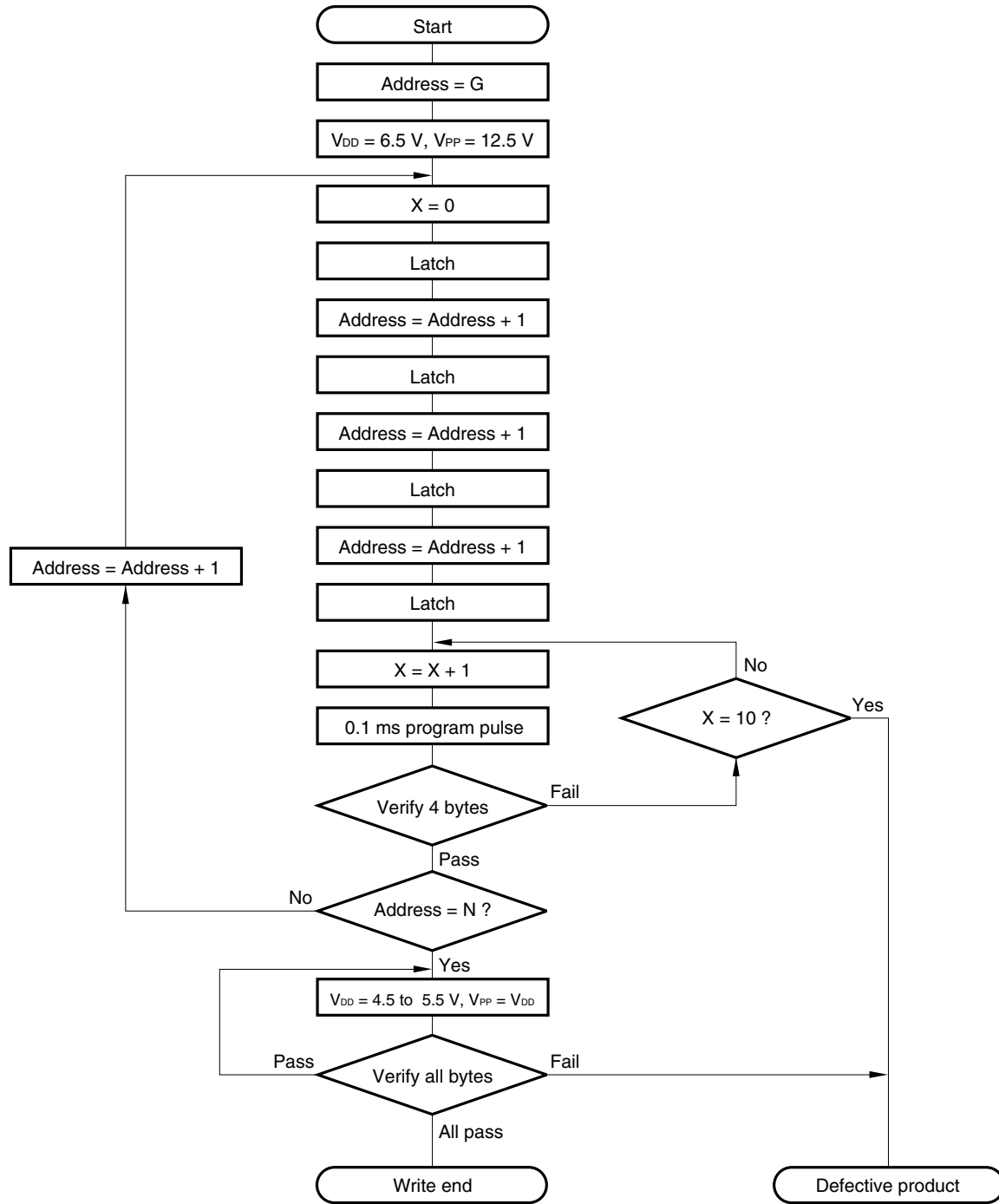
(8) Program inhibit mode

Program inhibit mode is used when the \overline{OE} pin, V_{PP} pin, and D0 to D7 pins of multiple μ PD78P0308 and 78P0308Ys are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device whose \overline{PGM} pin is driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart



G = Start address
 N = Program last address

Figure 5-2. Page Program Mode Timing

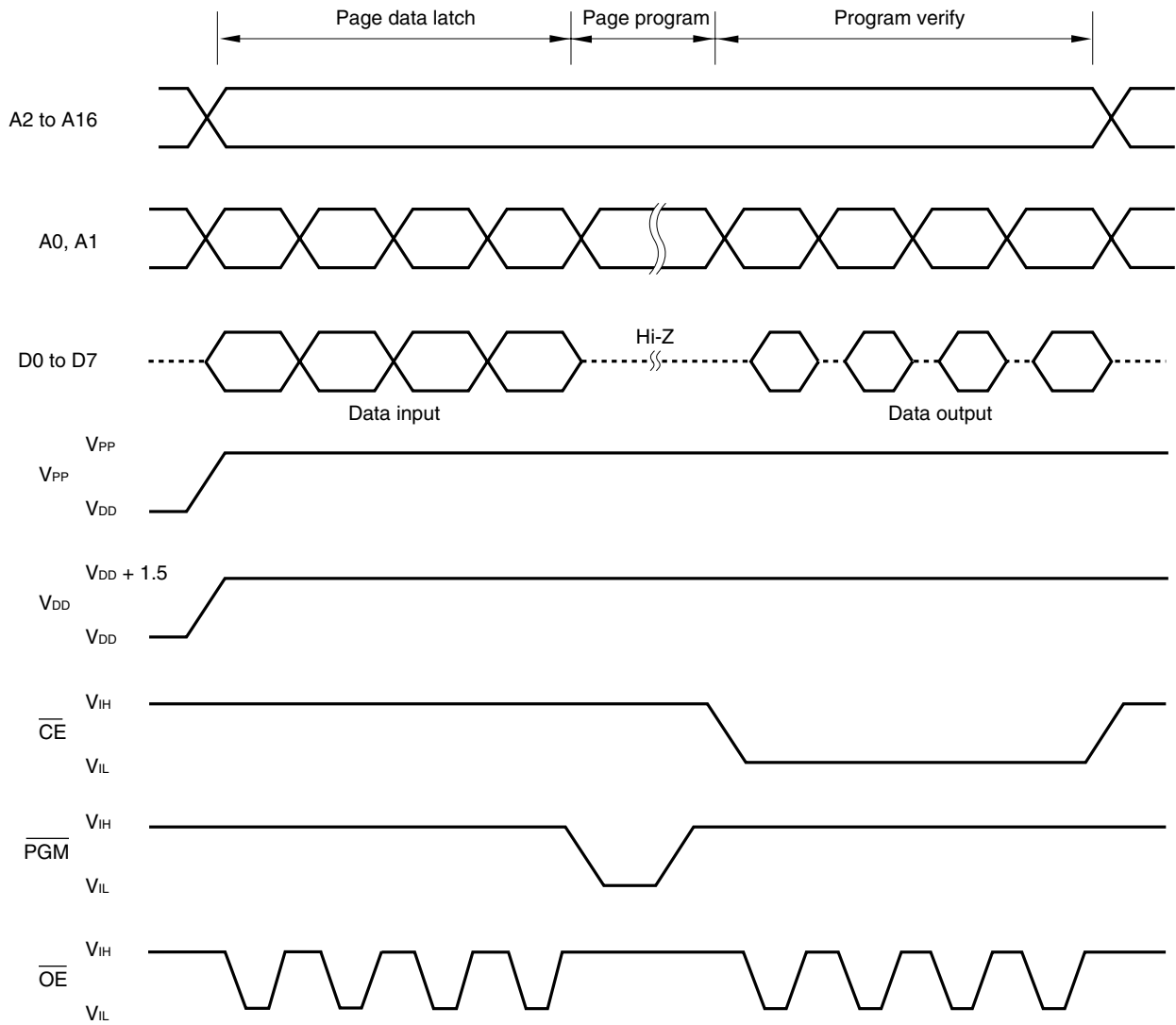
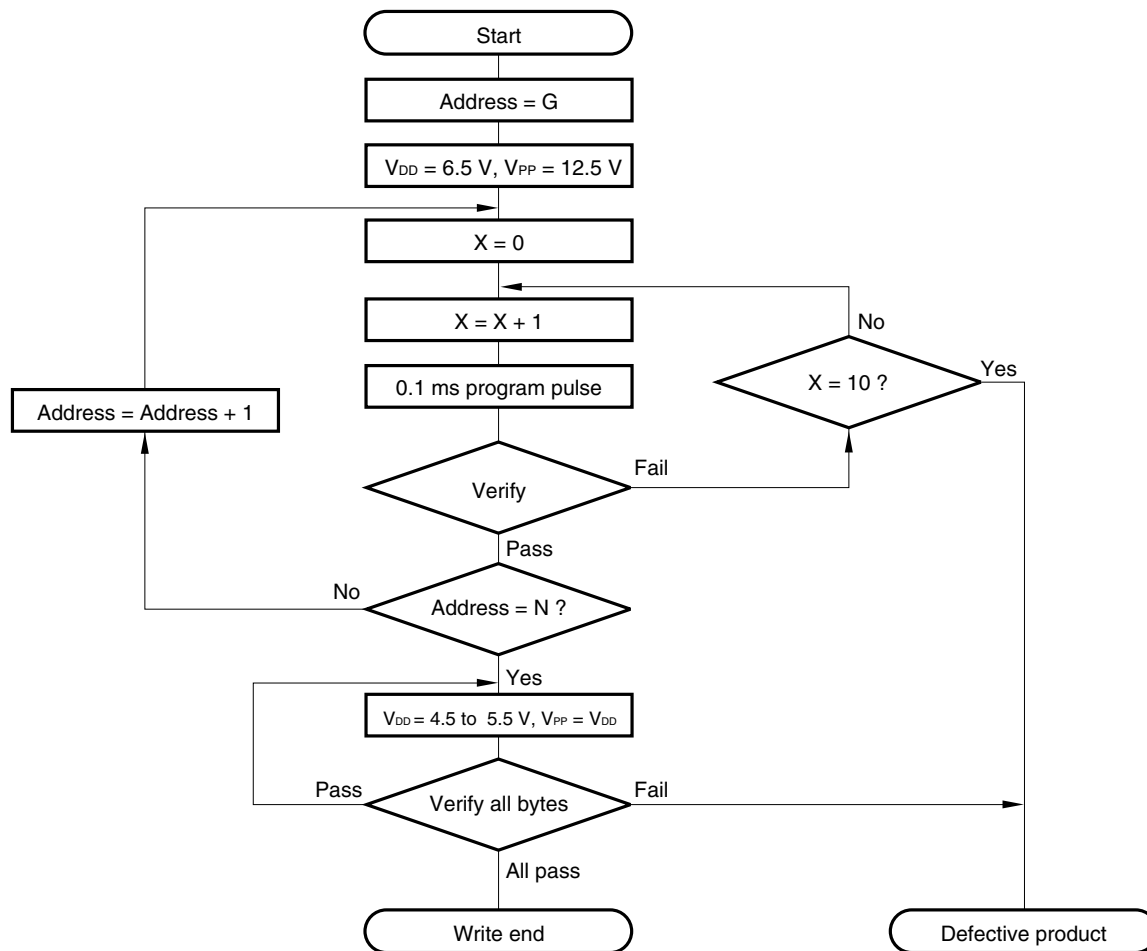
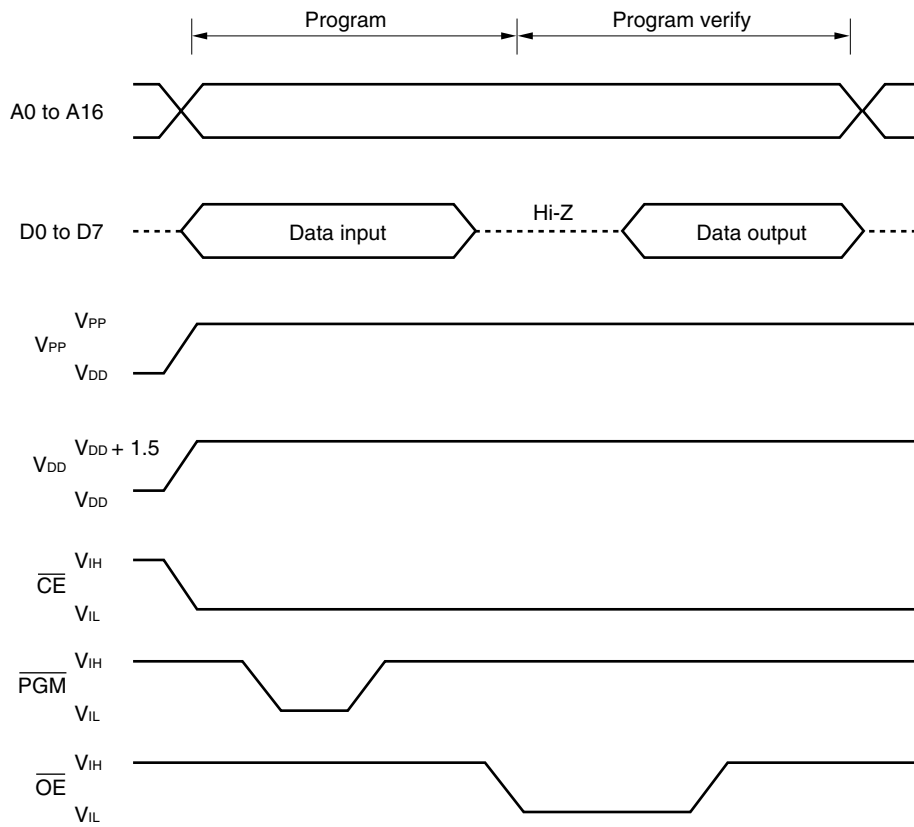


Figure 5-3. Byte Program Mode Flow Chart



G = Start address
 N = Program last address

Figure 5-4. Byte Program Mode Timing



- Cautions**
1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.
 2. V_{PP} should not exceed +13.5 V, including overshoot.
 3. Disconnection during application of +12.5 V to V_{PP} may have an adverse effect on reliability.

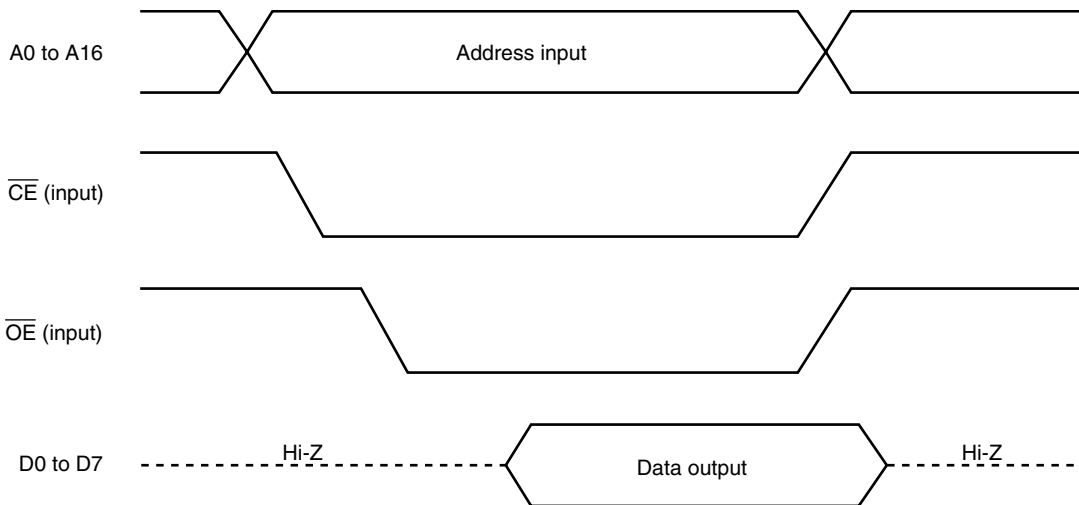
5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

- (1) Fix the $\overline{\text{RESET}}$ pin to low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **PIN CONFIGURATIONS (2) PROM programming mode.**
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) Input the address of the data to be read to the A0 to A16 pins.
- (4) Read mode
- (5) Output data to the D0 to D7 pins.

The timing of steps (2) to (5) above is shown in Figure 5-5.

Figure 5-5. PROM Read Timing



6. ONE-TIME PROM VERSION SCREENING

The one-time PROM versions ($\mu\text{PD78P0308GC-8EU}$, 78P0308GF-3BA , 78P0308YGC-8EU , and 78P0308YGF-3BA) cannot be tested completely by NEC Electronics before they are shipped, because of their structure. It is recommended to perform screening to verify PROM after writing the necessary data and performing high-temperature storage under the conditions below.

Storage Temperature	Storage Time
125°C	24 hours

★ 7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	V _{PP}			-0.3 to +13.5	V
	AV _{REF}			-0.3 to V _{DD} + 0.3	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _{I1}	P00 to P05, P07, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117, X1, X2, XT2, RESET		-0.3 to V _{DD} + 0.3	V
	V _{I2}	A9	PROM programming mode	-0.3 to +13.5	V
Output voltage	V _O			-0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pin	AV _{SS} - 0.3 to AV _{REF} + 0.3	V
Output current, high	I _{OH}	Per pin		-10	mA
		Total for P01 to P05, P10 to P17, P25 to P27, P70 to P72, P110 to P117		-15	mA
		Total for P30 to P37, P80 to P87, P90 to P97, P100 to P103		-15	mA
Output current, low	I _{OL}	Per pin	Peak value	30	mA
			r.m.s. value	15 ^{Note}	mA
		Total for P01 to P05, P10 to P17, P110 to P117	Peak value	60	mA
			r.m.s. value	40 ^{Note}	mA
		Total for P30 to P37, P100 to P103	Peak value	140	mA
			r.m.s. value	100 ^{Note}	mA
Total for P25 to P27, P70 to P72, P80 to P87, P90 to P97	Peak value	50	mA		
	r.m.s. value	20 ^{Note}	mA		
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note The root mean square (r.m.s.) value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

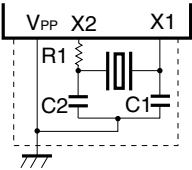
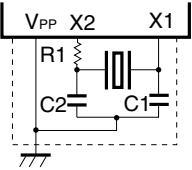
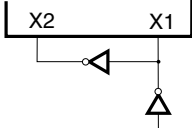
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C _{OUT}				15	pF
I/O capacitance	C _{IO}				15	pF

Main System Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0^{Note 4} to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time ^{Note 2}	4.5 V ≤ V _{DD} ≤ 5.5 V ^{Note 3} 2.0 V ≤ V _{DD} < 4.5 V ^{Note 3}			10 30	ms
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release.
 3. After V_{DD} reaches oscillation voltage range MIN.
 4. However, oscillation start voltage or higher and V_{DD} = 2.0 V or higher (for external clock, V_{DD} = 2.0 V or higher).

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0^{Note 4} to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f _{XT}) ^{Note 1}	V _{DD} = Oscillation voltage range	32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	4.5 V ≤ V _{DD} ≤ 5.5 V ^{Note 3} 2.0 V ≤ V _{DD} < 4.5 V ^{Note 3}		1.2	2	10
External clock		XT1 input frequency (f _{XT}) ^{Note 1}		32		100	kHz
		XT1 input high-/low-level width (t _{XTH} , t _{XTL})		5		15	μs

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.
 3. After V_{DD} reaches oscillation voltage range MIN.
 4. However, oscillation start voltage or higher and V_{DD} = 2.0 V or higher (for external clock, V_{DD} = 2.0 V or higher).

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P10 to P17, P30 to P32, P35 to P37, P80 to P87, P90 to P97, P100 to P103	2.7 V ≤ V _{DD} ≤ 5.5 V	0.7V _{DD}		V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V	0.8V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P05, P25 to P27, P33, P34, P70 to P72, P110 to P117, RESET	2.7 V ≤ V _{DD} ≤ 5.5 V	0.8V _{DD}		V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V	0.85V _{DD}		V _{DD}	V
	V _{IH3}	X1, X2	2.7 V ≤ V _{DD} ≤ 5.5 V	V _{DD} - 0.5		V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V	V _{DD} - 0.2		V _{DD}	V
	V _{IH4}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0.8V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9V _{DD}		V _{DD}	V
2.0 V ≤ V _{DD} < 2.7 V ^{Note}			0.9V _{DD}		V _{DD}	V	
Input voltage, low	V _{IL1}	P10 to P17, P30 to P32, P35 to P37, P80 to P87, P90 to P97, P100 to P103	2.7 V ≤ V _{DD} ≤ 5.5 V	0		0.3V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V	0		0.2V _{DD}	V
	V _{IL2}	P00 to P05, P25 to P27, P33, P34, P70 to P72, P110 to P117, RESET	2.7 V ≤ V _{DD} ≤ 5.5 V	0		0.2V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V	0		0.15V _{DD}	V
	V _{IL3}	X1, X2	2.7 V ≤ V _{DD} ≤ 5.5 V	0		0.4	V
			2.0 V ≤ V _{DD} < 2.7 V	0		0.2	V
	V _{IL4}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.2V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.1V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V ^{Note}	0		0.1V _{DD}	V
	Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = -1 mA	V _{DD} - 1.0		V _{DD}	V
I _{OH} = -100 μA			V _{DD} - 0.5		V _{DD}	V	
Output voltage, low	V _{OL1}	P100 to P103	V _{DD} = 4.5 to 5.5 V, I _{OL} = 15 mA		0.6	2.0	V
		P01 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P110 to P117	V _{DD} = 4.5 to 5.5 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, SCK0	V _{DD} = 4.5 to 5.5 V, open-drain, pulled up (R = 1 kΩ)			0.2V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V

Note When the XT1/P07 pin is used as P07, input the inverse phase of P07 to the XT2 pin.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	P00 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117, RESET _̄			3	μA
	I _{LIH2}		X1, X2, XT1/P07, XT2			20	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	P00 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117, RESET _̄			-3	μA
	I _{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
Output leakage current, high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leakage current, low	I _{LOL}	V _{OUT} = 0 V				-3	μA
Software pull-up resistor	R	V _{IN} = 0 V	P01 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117	15	45	90	kΩ
Supply current ^{Note 1}	I _{DD1}	5.00 MHz crystal oscillation (f _{xx} = 2.5 MHz) ^{Note 2} operating mode	V _{DD} = 5.0 V ±10% ^{Note 5}		5	15	mA
			V _{DD} = 3.0 V ±10% ^{Note 6}		0.7	2.1	mA
		5.00 MHz crystal oscillation (f _{xx} = 5.0 MHz) ^{Note 3} operating mode	V _{DD} = 2.2 V ±10% ^{Note 6}		0.4	1.2	mA
			V _{DD} = 5.0 V ±10% ^{Note 5}		9	27	mA
		5.00 MHz crystal oscillation (f _{xx} = 5.0 MHz) ^{Note 3} HALT mode	V _{DD} = 3.0 V ±10% ^{Note 6}		1	3	mA
			V _{DD} = 5.0 V ±10%		1.4	4.2	mA
	I _{DD2}	32.768 kHz crystal oscillation operating mode ^{Note 4}	V _{DD} = 3.0 V ±10%		500	1500	μA
			V _{DD} = 2.2 V ±10%		280	840	μA
		32.768 kHz crystal oscillation HALT mode ^{Note 4}	V _{DD} = 5.0 V ±10%		1.6	4.8	mA
			V _{DD} = 3.0 V ±10%		650	1950	μA
	I _{DD3}	32.768 kHz crystal oscillation HALT mode ^{Note 4}	V _{DD} = 5.0 V ±10%		135	270	μA
			V _{DD} = 3.0 V ±10%		95	190	μA
			V _{DD} = 2.2 V ±10%		70	140	μA
	I _{DD4}	XT1 = V _{DD} STOP mode When feedback resistor is connected	V _{DD} = 5.0 V ±10%		25	55	μA
			V _{DD} = 3.0 V ±10%		5	15	μA
V _{DD} = 2.2 V ±10%				2.5	12.5	μA	
I _{DD5}	XT1 = V _{DD} STOP mode When feedback resistor is disconnected	V _{DD} = 5.0 V ±10%		1	30	μA	
		V _{DD} = 3.0 V ±10%		0.5	10	μA	
		V _{DD} = 2.2 V ±10%		0.3	10	μA	
I _{DD6}	XT1 = V _{DD} STOP mode When feedback resistor is disconnected	V _{DD} = 5.0 V ±10%		0.1	30	μA	
		V _{DD} = 3.0 V ±10%		0.05	10	μA	
		V _{DD} = 2.2 V ±10%		0.05	10	μA	

- Notes**
1. Current flowing to the V_{DD} pin. Not including the current flowing to the A/D converter, on-chip pull-up resistors, or LCD dividing resistors.
 2. Main system clock f_{xx} = f_x/2 operation (when oscillation mode selection register (OSMS) is set to 00H)
 3. Main system clock f_{xx} = f_x operation (when OSMS is set to 01H)
 4. When the main system clock is stopped.
 5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)
 6. Low-speed mode operation (when PCC is set to 04H)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

LCD Controller/Driver Characteristics (at Normal Operation)

(1) Static display mode (T_A = -10 to +85°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.0		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} 2.0 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 bias method (T_A = -10 to +85°C, V_{DD} = 2.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.5		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} V _{LCD1} = V _{LCD} × 2/3 2.5 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 bias method (T_A = -10 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.7		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} V _{LCD1} = V _{LCD} × 1/2 2.7 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

LCD Controller/Driver Characteristics (at Low-Voltage Operation)

(1) Static display mode (T_A = -10 to +85°C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.0		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} 2.0 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 bias method (T_A = -10 to +85°C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.0		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} V _{LCD1} = V _{LCD} × 2/3	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		V _{LCD2} = V _{LCD} × 1/3 2.0 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 bias method (T_A = -10 to +85°C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.0		V _{DD}	V
LCD dividing resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	V _{LCD0} = V _{LCD} V _{LCD1} = V _{LCD} × 1/2	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		V _{LCD2} = V _{LCD1} 2.0 V ≤ V _{LCD} ≤ V _{DD}	0		±0.2

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

AC Characteristics

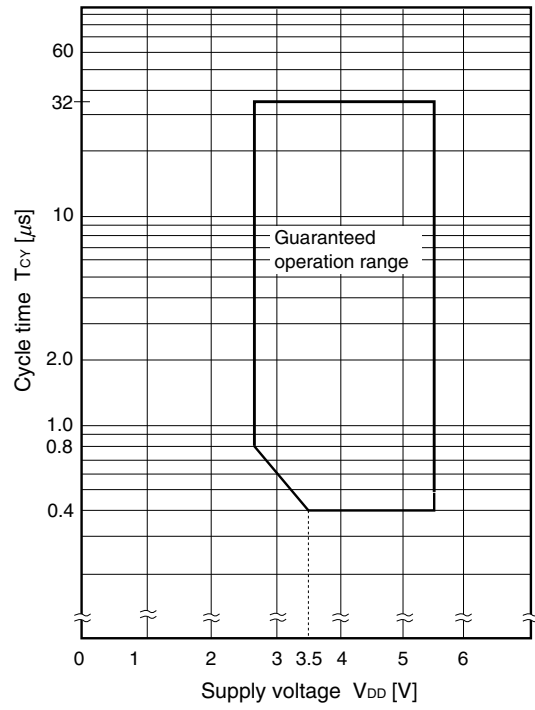
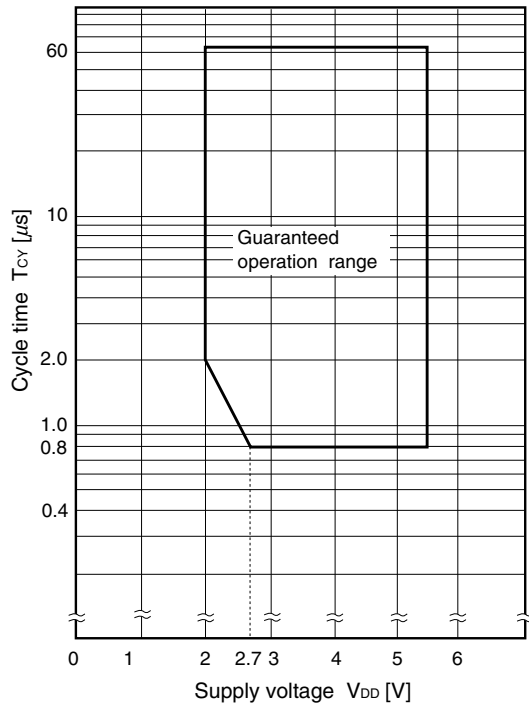
(1) Basic operation (T_A = -40 to +85°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Min. instruction execution time)	T _{CY}	Operating on main system clock	2.7 V ≤ V _{DD} ≤ 5.5 V	0.8		64	μs
		(f _{XX} = 2.5 MHz) ^{Note 1}	2.0 V ≤ V _{DD} < 2.7 V	2.0		64	μs
		Operating on main system clock	3.5 V ≤ V _{DD} ≤ 5.5 V	0.4		32	μs
		(f _{XX} = 5.0 MHz) ^{Note 2}	2.7 V ≤ V _{DD} < 3.5 V	0.8		32	μs
		Operating on subsystem clock		40 ^{Note 3}	122	125	μs
T100 input frequency	f _{T100}	t _{T100} = t _{TIH00} + t _{TIL00}	0		1/t _{T100}	MHz	
T100 input high-/ low-level width	t _{TIH00} , t _{TIL00}	3.5 V ≤ V _{DD} ≤ 5.5 V	2f _{sam} + 0.1 ^{Note 4}			μs	
		2.7 V ≤ V _{DD} < 3.5 V	2f _{sam} + 0.2 ^{Note 4}			μs	
		2.0 V ≤ V _{DD} < 2.7 V	2f _{sam} + 0.5 ^{Note 4}			μs	
T101 input frequency	f _{T101}	2.7 V ≤ V _{DD} ≤ 5.5 V	0		100	kHz	
		2.0 V ≤ V _{DD} < 2.7 V	0		50	kHz	
T101 input high-/ low-level width	t _{TIH01} , t _{TIL01}	2.7 V ≤ V _{DD} ≤ 5.5 V	10			μs	
		2.0 V ≤ V _{DD} < 2.7 V	20			μs	
T11, T12 input frequency	f _{T11}	4.5 V ≤ V _{DD} ≤ 5.5 V	0		4	MHz	
		2.0 V ≤ V _{DD} < 4.5 V	0		275	kHz	
T11, T12 input high-/ low-level width	t _{TIH1} , t _{TIL1}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns	
		2.0 V ≤ V _{DD} < 4.5 V	1.8			μs	
Interrupt request input high-/low- level width	t _{INTH} , t _{INTL}	INTP0	3.5 V ≤ V _{DD} ≤ 5.5 V	2f _{sam} + 0.1 ^{Note 4}			μs
			2.7 V ≤ V _{DD} < 3.5 V	2f _{sam} + 0.2 ^{Note 4}			μs
			2.0 V ≤ V _{DD} < 2.7 V	2f _{sam} + 0.5 ^{Note 4}			μs
		INTP1 to INTP5, P110 to P117	2.7 V ≤ V _{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V _{DD} < 2.7 V	20			μs
RESET low-level width	t _{RSL}	2.7 V ≤ V _{DD} ≤ 5.5 V	10			μs	
		2.0 V ≤ V _{DD} < 2.7 V	20			μs	

- Notes**
1. Main system clock f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H)
 2. Main system clock f_{XX} = f_X operation (when OSMS is set to 01H)
 3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.
 4. In combination with bits 0 (SCS0) and 1 (SCS1) of the sampling clock select register (SCS), selection of f_{sam} is possible between f_{XX}/2^N, f_{XX}/32, f_{XX}/64, and f_{XX}/128 (when N = 0 to 4).

T_{CY} vs. V_{DD} (at main system clock f_{XX} = f_X/2 operation)

T_{CY} vs. V_{DD} (at main system clock f_{XX} = f_X operation)



(2) Serial interface (T_A = -40 to +85°C, V_{DD} = 2.0 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY1}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH1} ,	4.5 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2 - 50			ns
	t _{KL1}	2.0 V ≤ V _{DD} < 4.5 V	t _{KCY1} /2 - 100			ns
SI0 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK1}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
		2.0 V ≤ V _{DD} < 2.7 V	300			ns
SI0 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI1}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}$ ↓	t _{KSO1}	C = 100 pF ^{Note}			300	ns

Note C is the load capacitance of $\overline{\text{SCK0}}$ and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY2}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH2} ,	4.5 V ≤ V _{DD} ≤ 5.5 V	400			ns
	t _{KL2}	2.7 V ≤ V _{DD} < 4.5 V	800			ns
		2.0 V ≤ V _{DD} < 2.7 V	1600			ns
SI0 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK2}		100			ns
SI0 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KSI2}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}$ ↓	t _{KSO2}	C = 100 pF ^{Note}			300	ns
$\overline{\text{SCK0}}$ rise, fall time	t _{R2} ,				1000	ns
	t _{F2}					

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{\text{SCK0}}$...internal clock output): μPD78P0308 only

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{CY3}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH3}},$ t_{KL3}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		$t_{\text{CY3}}/2 - 50$			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		$t_{\text{CY3}}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK3}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		100			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{SI3}			$t_{\text{CY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{SO3}	R = 1 kΩ, C = 100 pF ^{Note}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0		250	ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}\uparrow$	t_{KSB}			t_{CY3}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{CY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{CY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{CY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0, and SB1 output lines.

(iv) SBI mode ($\overline{\text{SCK0}}$...external clock input): μPD78P0308 only

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{CY4}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH4}},$ t_{KL4}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		400			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK4}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		100			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{SI4}			$t_{\text{CY4}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{SO4}	R = 1 kΩ, C = 100 pF ^{Note}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0		300	ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}\uparrow$	t_{KSB}			t_{CY4}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{CY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{CY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{CY4}			ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R4}},$ t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF ^{Note}	2.7 V ≤ V _{DD} ≤ 5.5 V	1600		ns
			2.0 V ≤ V _{DD} < 2.7 V	3200		ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		2.7 V ≤ V _{DD} ≤ 5.5 V	$t_{\text{KCY5}}/2 - 160$		ns
			2.0 V ≤ V _{DD} < 2.7 V	$t_{\text{KCY5}}/2 - 190$		ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		4.5 V ≤ V _{DD} ≤ 5.5 V	$t_{\text{KCY5}}/2 - 50$		ns
			2.0 V ≤ V _{DD} < 4.5 V	$t_{\text{KCY5}}/2 - 100$		ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK5}		4.5 V ≤ V _{DD} ≤ 5.5 V	300		ns
			2.7 V ≤ V _{DD} < 4.5 V	350		ns
			2.0 V ≤ V _{DD} < 2.7 V	400		ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI5}		600		ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO5}				300	ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0, and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}	2.7 V ≤ V _{DD} ≤ 5.5 V	1600		ns	
		2.0 V ≤ V _{DD} < 2.7 V	3200		ns	
$\overline{\text{SCK0}}$ high-level width	t_{KH6}	2.7 V ≤ V _{DD} ≤ 5.5 V	650		ns	
		2.0 V ≤ V _{DD} < 2.7 V	1300		ns	
$\overline{\text{SCK0}}$ low-level width	t_{KL6}	2.7 V ≤ V _{DD} ≤ 5.5 V	800		ns	
		2.0 V ≤ V _{DD} < 2.7 V	1600		ns	
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK6}		100		ns	
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI6}		$t_{\text{KCY6}}/2$		ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO6}	R = 1 kΩ, C = 100 pF ^{Note}	4.5 V ≤ V _{DD} ≤ 5.5 V	0	300	ns
			2.0 V ≤ V _{DD} < 4.5 V	0	500	ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R6}				1000	ns
	t_{F6}					ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I²C bus mode (SCL...internal clock output): μPD78P0308Y only

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t _{KCY7}	R = 1 kΩ, C = 100 pF ^{Note}	2.7 V ≤ V _{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V _{DD} < 2.7 V	20			μs
SCL high-level width	t _{KH7}		2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY7} - 160			ns
			2.0 V ≤ V _{DD} < 2.7 V	t _{KCY7} - 190			ns
SCL low-level width	t _{KL7}		4.5 V ≤ V _{DD} ≤ 5.5 V	t _{KCY7} - 50			ns
			2.0 V ≤ V _{DD} < 4.5 V	t _{KCY7} - 100			ns
SDA0, SDA1 setup time (to SCL↑)	t _{SIK7}		2.7 V ≤ V _{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V _{DD} < 2.7 V	300			ns
SDA0, SDA1 hold time (from SCL↓)	t _{KSI7}			0			ns
SDA0, SDA1 output delay time from SCL↓	t _{KSO7}		4.5 V ≤ V _{DD} ≤ 5.5 V	0		300	ns
		2.0 V ≤ V _{DD} < 4.5 V	0		500	ns	
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t _{KSB}		200			ns	
SCL↓ from SDA0, SDA1↓	t _{SBK}		400			ns	
SDA0, SDA1 high-level width	t _{SBH}		500			ns	

Note R and C are the load resistance and load capacitance of SCL, SDA0, and SDA1 output lines.

(viii) I²C bus mode (SCL...external clock input): μPD78P0308Y only

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t _{KCY8}			1000			ns
SCL high-/low-level width	t _{KH8} , t _{KL8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t _{SIK8}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t _{KSI8}			0			ns
SDA0, SDA1 output delay time from SCL↓	t _{KSO8}	R = 1 kΩ, C = 100 pF ^{Note}	4.5 V ≤ V _{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V _{DD} < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t _{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t _{SBK}			400			ns
SDA0, SDA1 high-level width	t _{SBH}			500			ns
SCL rise, fall time	t _{RS} , t _{FS}					1000	ns

Note R and C are the load resistance and load capacitance of SDA0 and SDA1 output lines.

(b) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
$\overline{\text{SCK2}}$ high-/low-level width	t_{KH9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	t_{KL9}	$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY9}}/2 - 100$			ns
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{SI9}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO9}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

Note C is the load capacitance of $\overline{\text{SCK2}}$ and SO2 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
$\overline{\text{SCK2}}$ high-/low-level width	t_{KH10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
	t_{KL10}	$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1600			ns
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK10}		100			ns
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{SI10}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO10}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK2}}$ rise, fall time	t_{R10}				1000	ns
	t_{F10}					

Note C is the load capacitance of SO2 output line.

(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			78125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39063	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			19531	bps

(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY11}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
ASCK high-/low-level width	$t_{KH11},$ t_{KL11}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1600			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19531	bps
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			9766	bps
ASCK rise, fall time	$t_{R11},$ t_{F11}				1000	ns

(c) Serial interface channel 3

(i) 3-wire serial I/O mode ($\overline{\text{SCK3}}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t_{KCY12}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
$\overline{\text{SCK3}}$ high-/low-level width	$t_{\text{KH12}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY12}}/2 - 50$			ns
	t_{KL12}	$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY12}}/2 - 100$			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t_{SIK12}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t_{SI12}		400			ns
SO3 output delay time from $\overline{\text{SCK3}}\downarrow$	t_{KS012}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

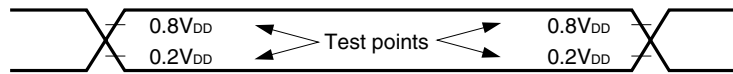
Note C is the load capacitance of $\overline{\text{SCK3}}$ and SO3 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK3}}$...external clock input)

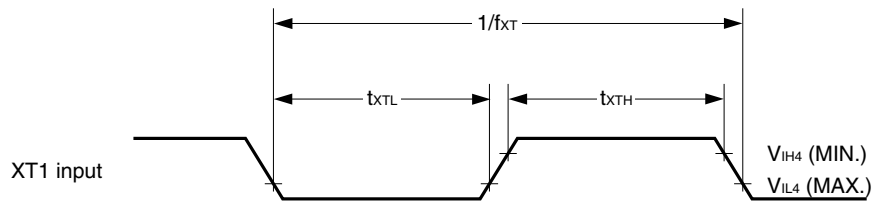
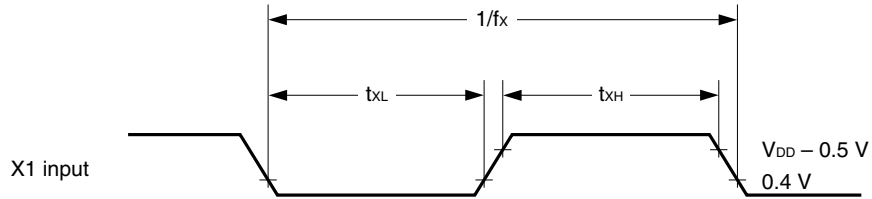
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t_{KCY13}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
$\overline{\text{SCK3}}$ high-/low-level width	$t_{\text{KH13}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
		t_{KL13}	$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800		ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1600			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t_{SIK13}		100			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t_{SI13}		400			ns
SO3 output delay time from $\overline{\text{SCK3}}\downarrow$	t_{KS013}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK3}}$ rise, fall time	$t_{\text{R13}},$				1000	ns

Note C is the load capacitance of SO3 output line.

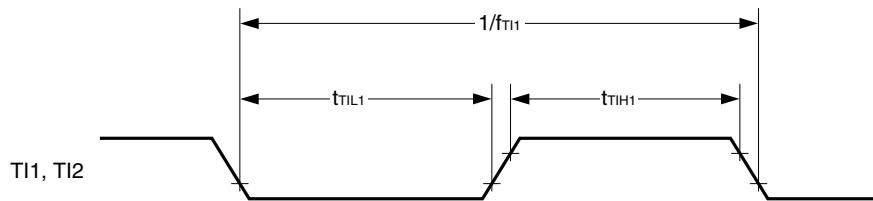
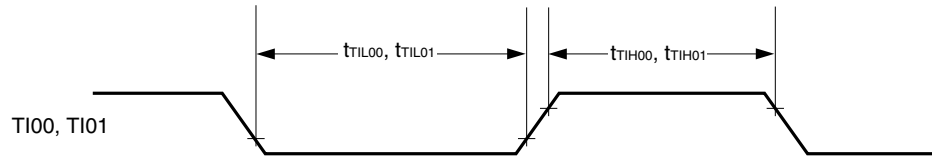
AC Timing Test Points (Excluding X1, XT1 Inputs)



Clock Timing

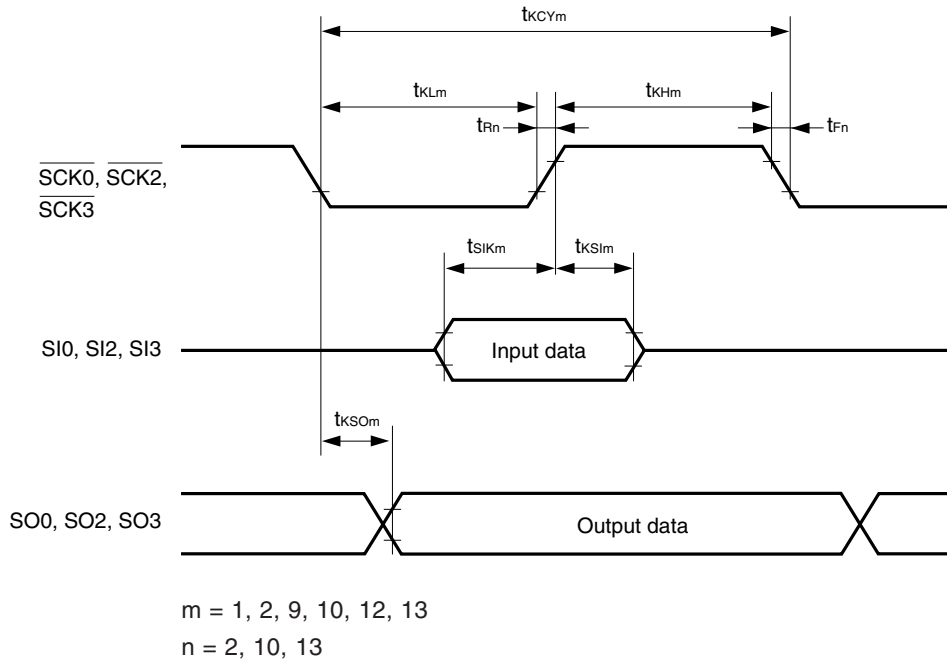


TI Timing

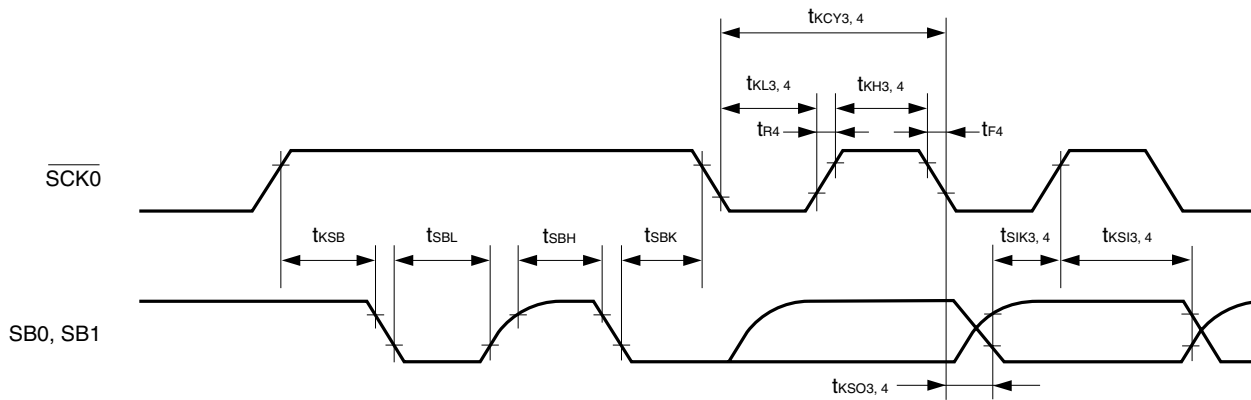


Serial Transfer Timing

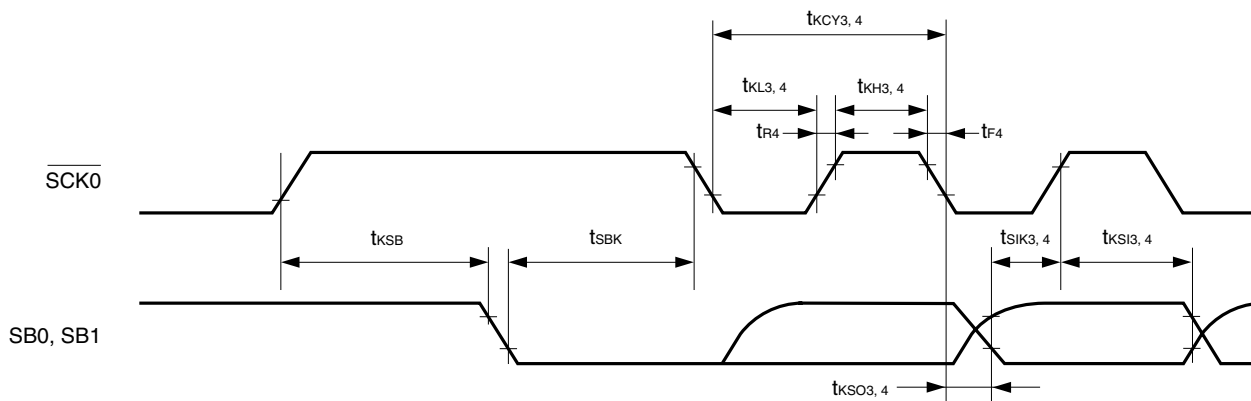
3-wire serial I/O mode:



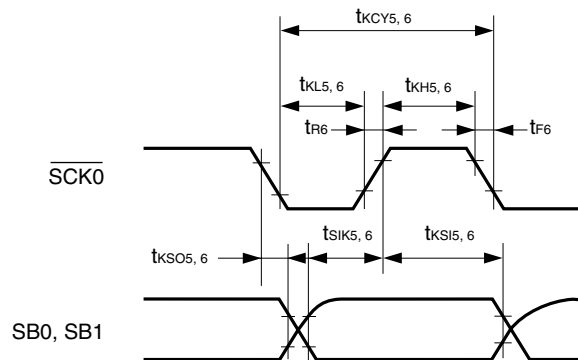
SBI mode (bus release signal transfer, μ PD78P0308 only):



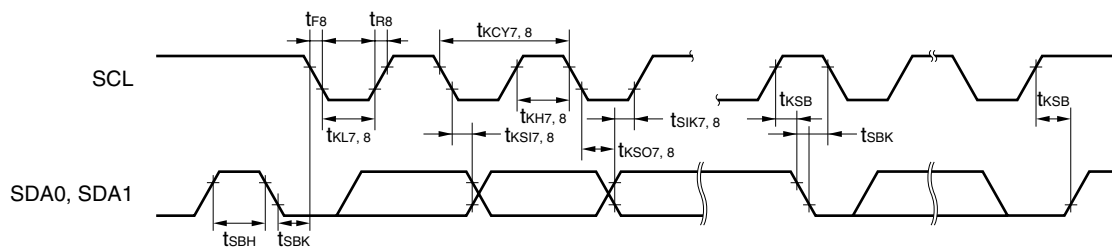
SBI mode (command signal transfer, μ PD78P0308 only):



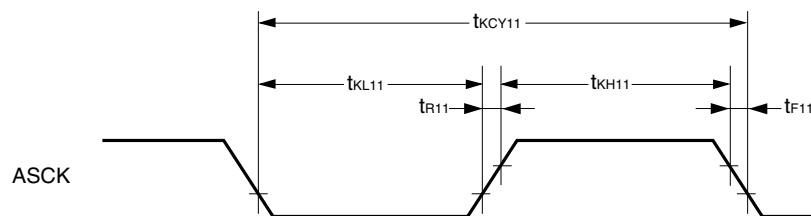
2-wire serial I/O mode:



I²C bus mode (μ PD78P0308Y only):



UART mode:



A/D Converter Characteristics (T_A = -40 to +85°C, V_{DD} = 2.2 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error ^{Note 1}		2.7 V ≤ AV _{REF} ≤ 5.5 V			±0.6	%FSR
		2.2 V ≤ AV _{REF} < 2.7 V			±1.4	%FSR
Conversion time	t _{CONV}	2.7 V ≤ AV _{REF} ≤ 5.5 V	19.1		200	μs
		2.2 V ≤ AV _{REF} < 2.7 V	38.2		200	μs
Sampling time	t _{SAMP}		24/t _{XX}			μs
Analog input voltage	V _{IAN}		AV _{SS}		AV _{REF}	V
Reference voltage	AV _{REF}		2.2		V _{DD}	V
AV _{REF} -AV _{SS} resistance	R _{AIREF}	When A/D conversion not operating	4	14		kΩ
AV _{REF} current	AI _{REF}	When A/D conversion operating ^{Note 2}		2.5	5.0	mA
		When A/D conversion not operating ^{Note 3}		0.5	1.5	mA

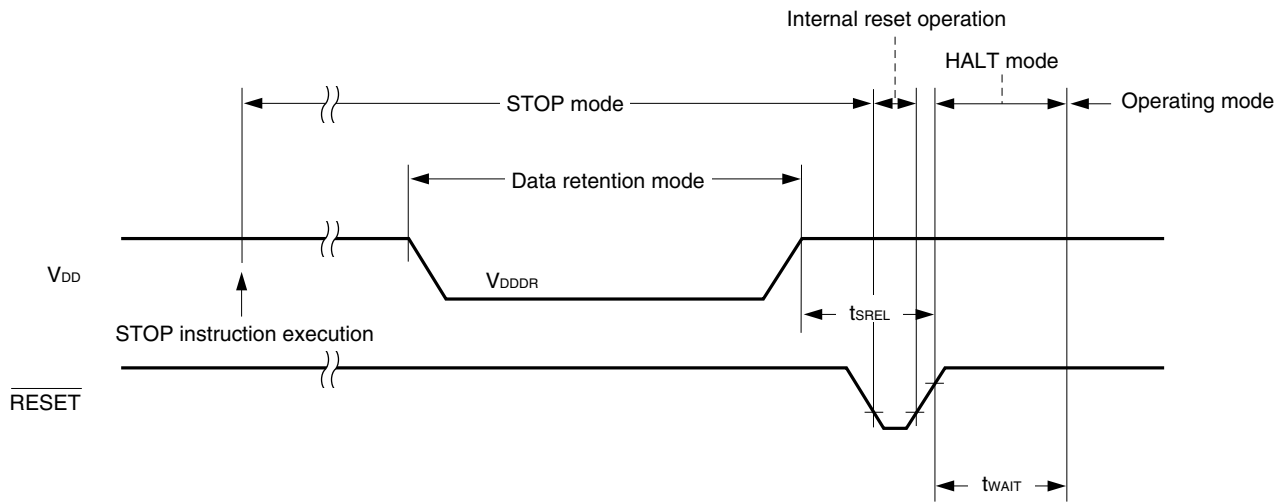
- Notes**
1. Quantization error (±1/2 LSB) is not included. This is expressed as a percentage (%FSR) to the full-scale value.
 2. Indicates current flowing to AV_{REF} pin when the CS bit of the A/D converter mode register (ADM) is 1.
 3. Indicates current flowing to AV_{REF} pin when the CS bit of ADM is 0.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (TA = -40 to +85°C)

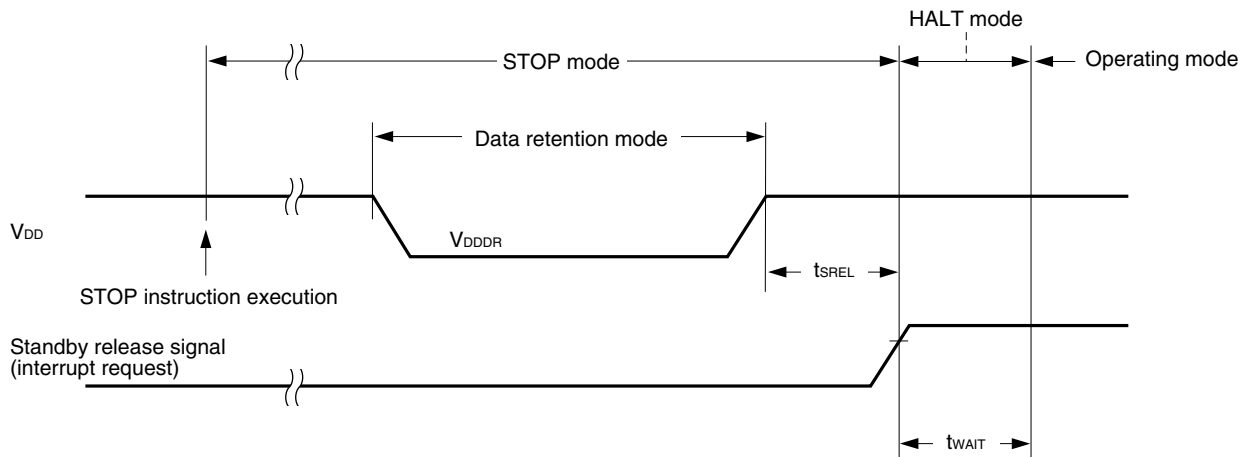
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.6		5.5	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.6 V Subsystem clock stop and feedback resistor disconnected.		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /fx		s
		Release by interrupt request		Note		s

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS), selection of 2¹²/fx and 2¹⁴/fx to 2¹⁷/fx is possible.

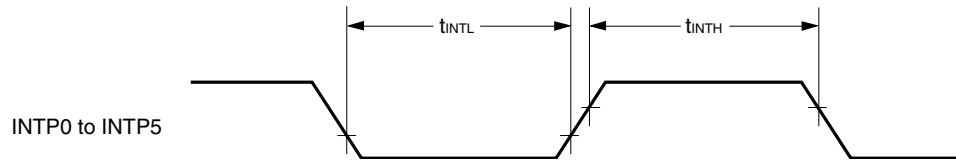
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



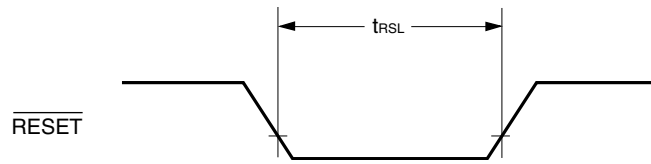
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM Programming Characteristics

DC Characteristics

(1) PROM write mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Output voltage, low	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	$\overline{PGM} = V_{IL}$			50	mA
V_{DD} supply current	I_{DD}				50	mA

(2) PROM read mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5\text{ V}$, $V_{PP} = V_{DD} \pm 0.6\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH1}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
	V_{OH2}	$I_{OH} = -100\ \mu\text{A}$	$V_{DD} - 0.5$			V
Output voltage, low	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
Output leakage current	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE} = V_{IH}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}		$V_{DD} - 0.6$	V_{DD}	$V_{DD} + 0.6$	V
V_{DD} supply voltage	V_{DD}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

AC Characteristics

(1) PROM write mode

(a) Page program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{OE}}\downarrow$)	t_{AS}		2			μs
$\overline{\text{OE}}$ setup time	t_{OES}		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{OE}}\downarrow$)	t_{CES}		2			μs
Input data setup time (to $\overline{\text{OE}}\downarrow$)	t_{DS}		2			μs
Address hold time (from $\overline{\text{OE}}\uparrow$)	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time (from $\overline{\text{OE}}\uparrow$)	t_{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{\text{OE}}\downarrow$)	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{\text{OE}}\downarrow$)	t_{VDS}		1.0		250	ms
Program pulse width	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	t_{OE}				1	μs
$\overline{\text{OE}}$ pulse width during data latching	t_{LW}		1			μs
$\overline{\text{PGM}}$ setup time	t_{PGMS}		2			μs
$\overline{\text{CE}}$ hold time	t_{CEH}		2			μs
$\overline{\text{OE}}$ hold time	t_{OEH}		2			μs

(b) Byte program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{PGM}}\downarrow$)	t_{AS}		2			μs
$\overline{\text{OE}}$ setup time	t_{OES}		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{PGM}}\downarrow$)	t_{CES}		2			μs
Input data setup time (to $\overline{\text{PGM}}\downarrow$)	t_{DS}		2			μs
Address hold time (from $\overline{\text{OE}}\uparrow$)	t_{AH}		2			μs
Input data hold time (from $\overline{\text{PGM}}\uparrow$)	t_{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{\text{PGM}}\downarrow$)	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{\text{PGM}}\downarrow$)	t_{VDS}		1.0			ms
Program pulse width	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	t_{OE}				1	μs
$\overline{\text{OE}}$ hold time	t_{OEH}		2			μs

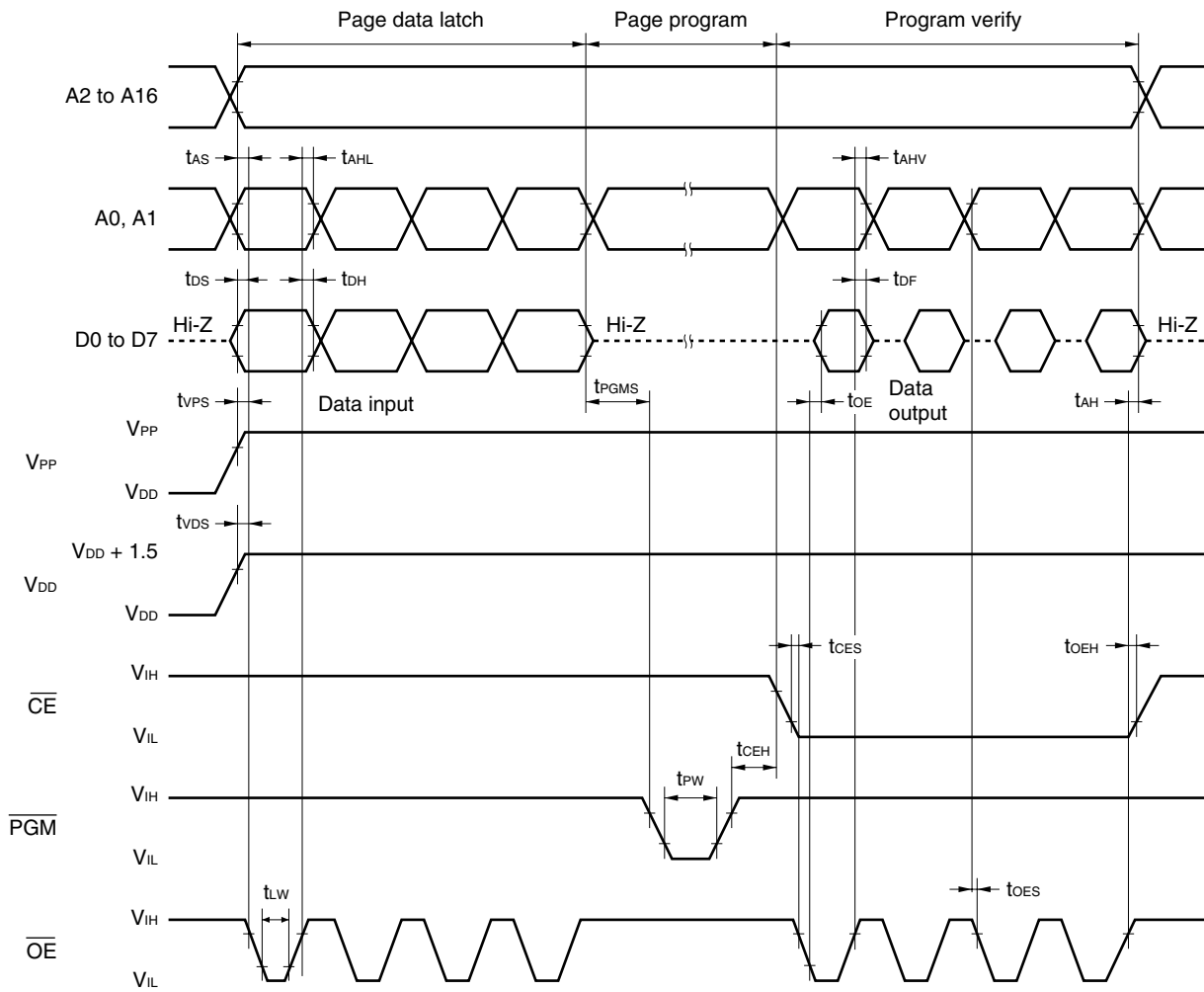
(2) PROM read mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5 \text{ V}$, $V_{PP} = V_{DD} \pm 0.6 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{CE}\downarrow$	t_{CE}	$\overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{OE}\downarrow$	t_{OE}	$\overline{CE} = V_{IL}$			200	ns
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Data hold time from address	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

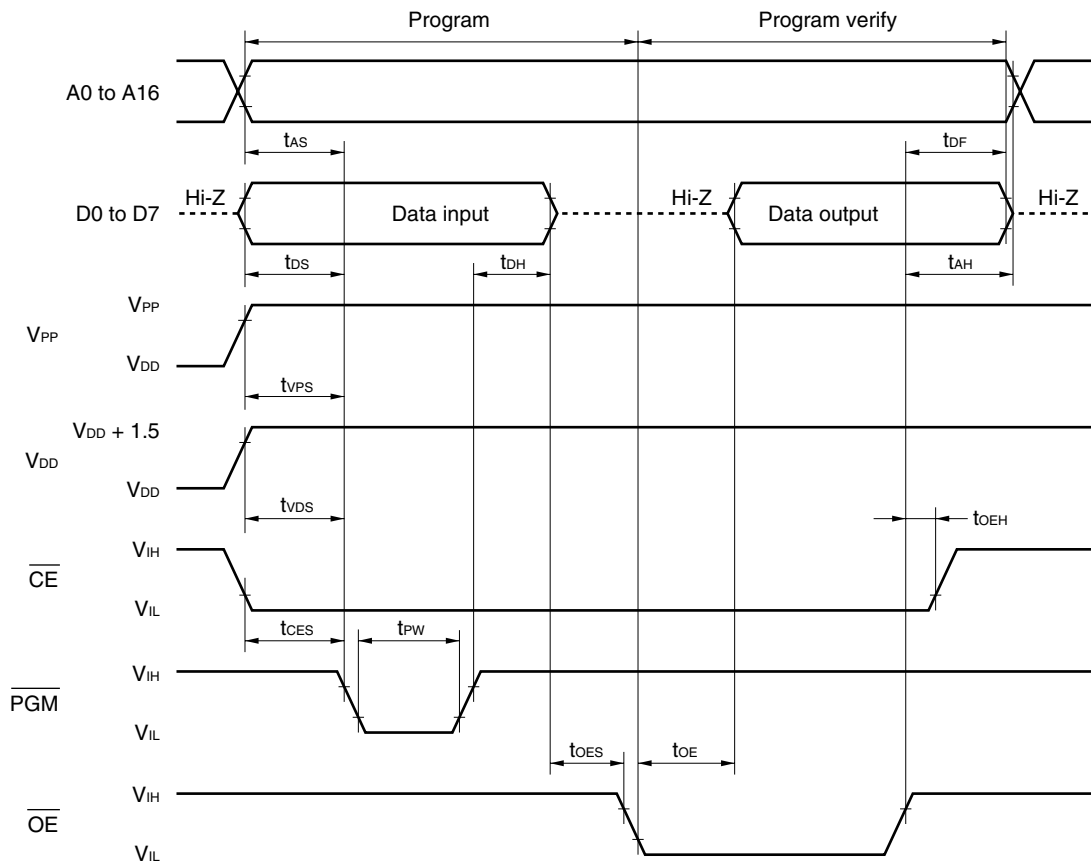
(3) PROM programming mode setting ($T_A = 25^\circ\text{C}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (Page Program Mode)

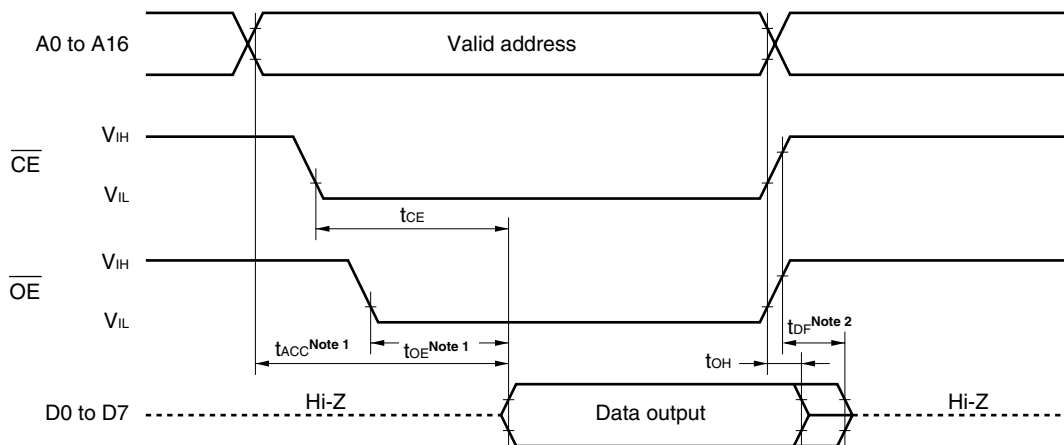


PROM Write Mode Timing (Byte Program Mode)



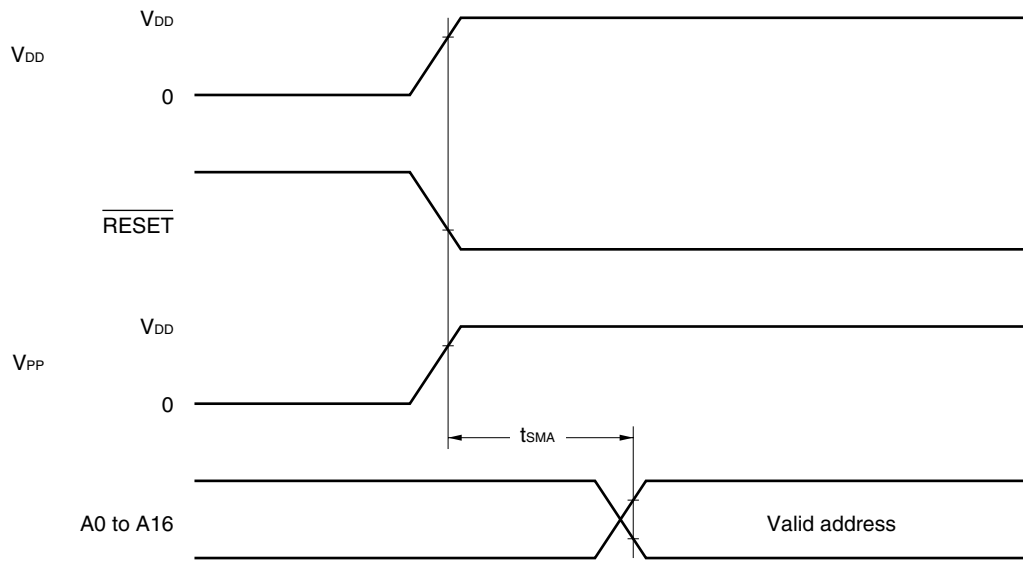
- Cautions**
1. V_{DD} should be applied before V_{PP} , and cut after V_{PP} .
 2. V_{PP} should not exceed +13.5 V, including overshoot.
 3. Disconnection during application of 12.5 V may have an adverse effect on reliability.

PROM Read Mode Timing



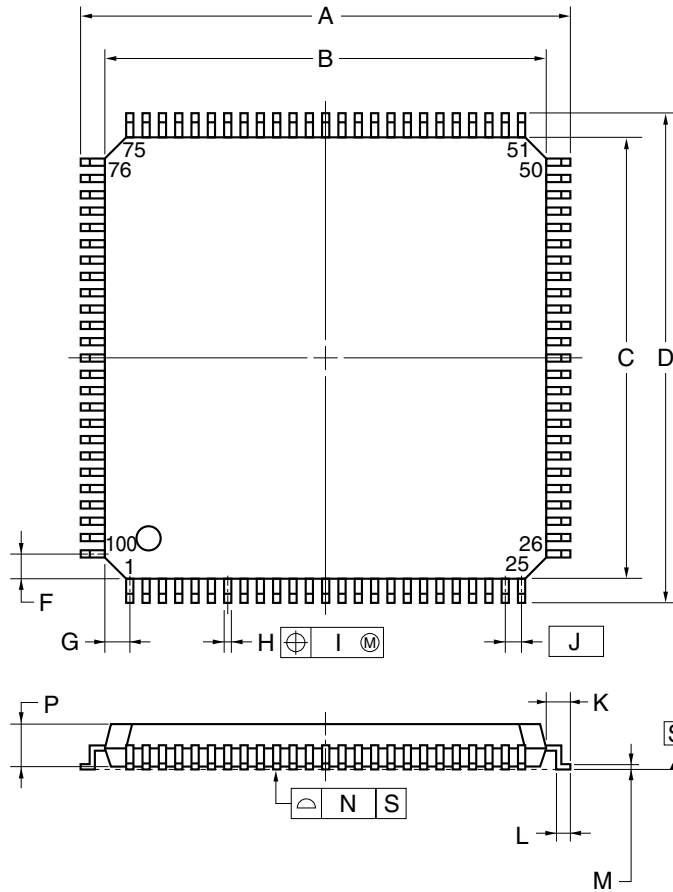
- Notes**
1. If you want to read within the t_{ACC} range, make the \overline{OE} input delay time from the fall of \overline{CE} the maximum of $t_{ACC} - t_{OE}$.
 2. t_{DF} is the time from when either \overline{OE} or \overline{CE} first reaches V_{IH} .

PROM Programming Mode Setting Timing

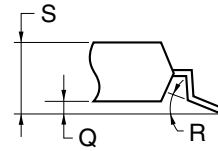


8. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



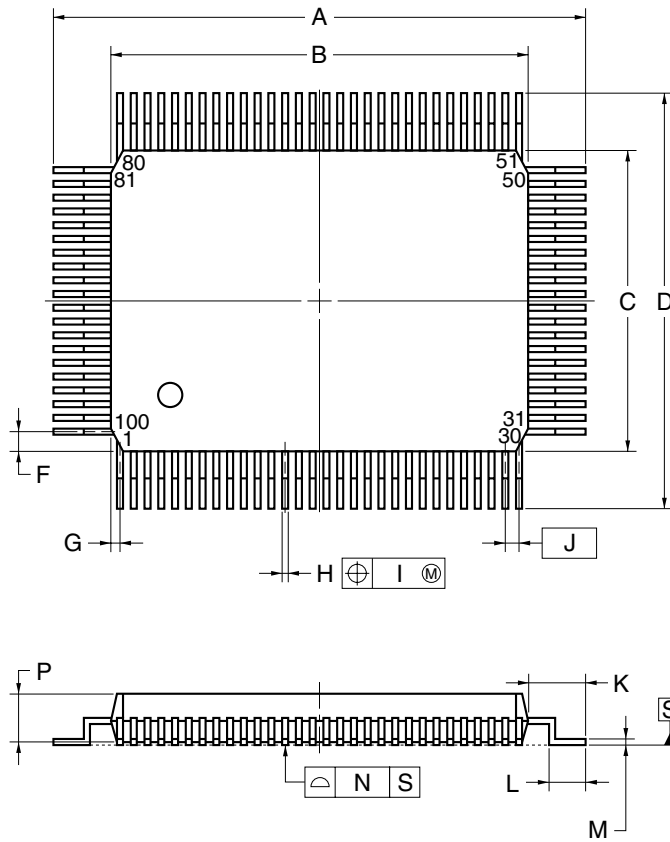
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

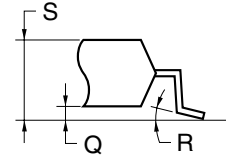
ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 ^{+0.05} _{-0.04}
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} _{-3°}
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

100-PIN PLASTIC QFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	0.15 ^{+0.10} _{-0.05}
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

★ 9. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Table 9-1. Surface Mounting Type Soldering Conditions

(1) 100-pin plastic QFP (14 × 20)

μPD78P0308GF-3BA, 78P0308YGF-3BA

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

(2) 100-pin plastic LQFP (fine pitch) (14 × 14)

μPD78P0308GC-8EU, 78P0308YGC-8EU

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD78P0308 and 78P0308Y. Also refer to (6) **Precautions When Using Development Tools**.

★ **(1) Software Package**

SP78K0	CD-ROM in which development tools (software) common to 78K/0 Series products are integrated in one package
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(2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series products
CC78K0	C compiler package common to 78K/0 Series products
DF780308	Device file for μPD780308 and 780308Y Subseries products (part number: μSxxxxDF78064)
CC78K0-L	C compiler library source file common to 78K/0 Series products

(3) PROM Write Tools

PG-1500	PROM programmer
PA-78P0308GC PA-78P0308GF	Programmer adapter connected to the PG-1500
PG-1500 controller	Control program for the PG-1500

★ **(4) Debugging Tools**

• **When using IE-78K0-NS or IE-78K0-NS-A as in-circuit emulator**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series products
IE-78K0-NS-PA	Performance board to enhance/expand functions of IE-78K0-NS
IE-78K0-NS-A	Combination of IE-78K0-NS and IE-78K0-NS-PA
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Adapter required when using a PC-9800 series (excluding notebook-type PCs) as the host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable required when using a notebook type PC as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when using an IBM PC/AT™ compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using a PC with an on-chip PCI bus as the host machine
IE-780308-NS-EM1	Emulation board to emulate μPD780308 and 780308Y Subseries products
NP-100GC NP-H100GC-TQ	Emulation probe for a 100-pin plastic LQFP (GC-8EU type)
NP-100GF NP-100GF-TQ NP-H100GF-TQ	Emulation probe for a 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC or NP-H100GC-TQ and a target system board made to be mounted on a 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Conversion socket to connect the NP-100GF and a target system board made to be mounted on a 100-pin plastic QFP (GF-3BA type)
TGF-100RBP	Conversion socket to connect the NP-100GF-TQ or NP-H100GF-TQ and a target system board made to be mounted on a 100-pin plastic QFP (GF-3BA type)
ID78K0-NS	Integrated debugger for the IE-78K0-NS and IE-78K0-NS-A
SM78K0	System simulator common to 78K/0 Series products
DF780308	Device file for μPD780308 and 780308Y Subseries products (part number: μSxxxxDF78064)

• When using IE-78001-R-A as in-circuit emulator

IE-78001-R-A ^{Note}	In-circuit emulator common to 78K/0 Series products
IE-70000-98-IF-C	Adapter required when using a PC-9800 series (excluding notebook-type PCs) as the host machine (C bus supported)
IE-70000-PC-IF-C	Adapter required when using an IBM PC/AT compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using a PC with an on-chip PCI bus as the host machine
IE-780308-R-EM ^{Note}	Emulation board to emulate μPD780308 and 780308Y Subseries products
EP-78064GC-R	Emulation probe for a 100-pin plastic LQFP (GC-8EU type)
EP-78064GF-R	Emulation probe for a 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the EP-78064GC-R and a target system board made to be mounted on a 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Conversion socket to connect the EP-78064GF-R and a target system board made to be mounted on a 100-pin plastic QFP (GF-3BA type)
ID78K0	Integrated debugger for the IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series products
DF780308	Device file for μPD780308 and 780308Y Subseries products (part number: μS××××DF78064)

Note Maintenance product

★ (5) Real-Time OS

RX78K0	Real-time OS for 78K/0 Series products
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★ (6) Precautions When Using Development Tools

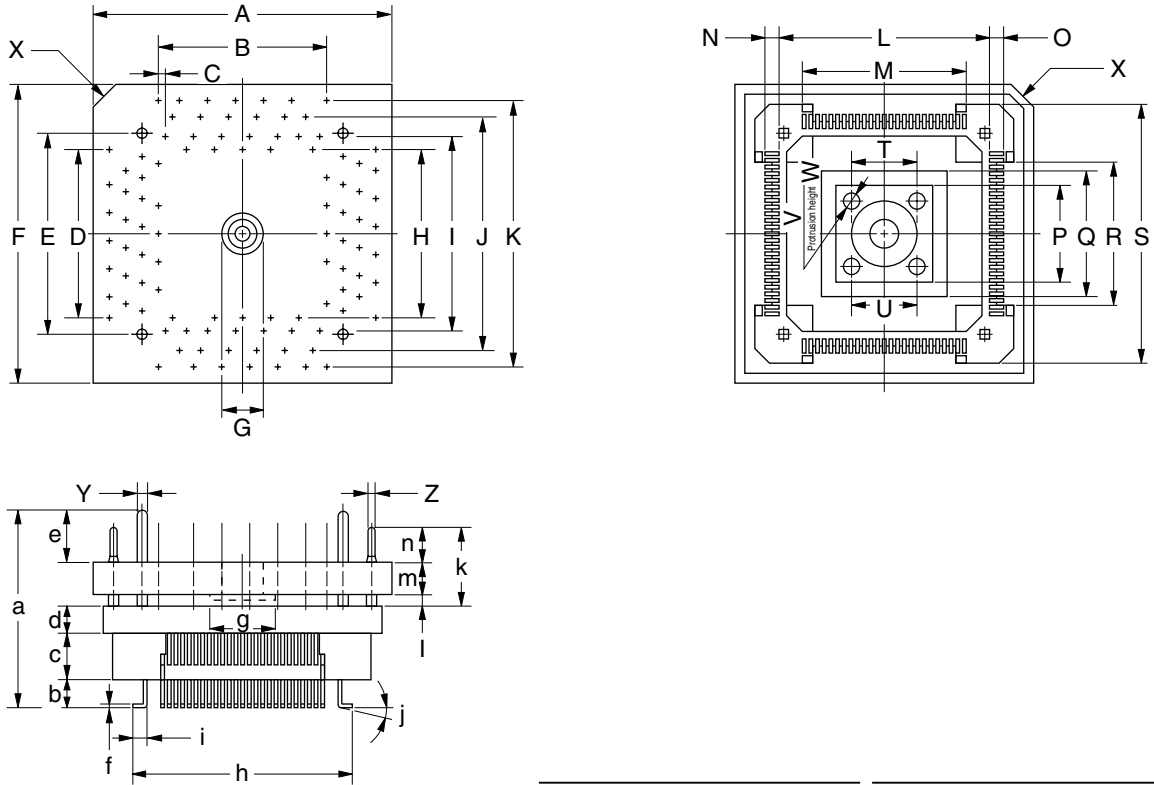
- The package name of the DF780308 is DF78064.
- Use the ID78K0-NS, ID78K0, and SM78K0 in combination with the DF780308.
- Use the CC78K0 and RX78K0 in combination with the RA78K0 and DF780308.
- The NP-100GC, NP-H100GC-TQ, NP-100GF, NP-100GF-TQ, and NP-H100GF-TQ are products of Naito Densai Machida Mfg. Co., Ltd. (tel: +81-45-475-4191).
- The TGC-100SDW and TGF-100RBP are products of TOKYO ELETECH CORPORATION.
 Contact: Daimaru Kogyo, Ltd. Tokyo Electronics Department (tel: +81-3-3820-7112)
 Osaka Electronics Department (tel: +81-6-6244-6672)
- Please refer to **Single-Chip Microcontroller Development Tools Selection Guide (U11069E)** for information on the third party development tools.
- The following table shows the software supported by each host machine and OS.

Host machine [OS]	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
Software		
RA78K0	√ ^{Note}	√
CC78K0	√ ^{Note}	√
PG-1500 controller	√ ^{Note}	—
ID78K0-NS	√	—
ID78K0	√	—
SM78K0	√	—
RX78K0	√ ^{Note}	√

Note DOS-based software

Drawing of Conversion Adapter (TGC-100SDW)

Figure A-1. Drawing of TGC-100SDW (for Reference Only)

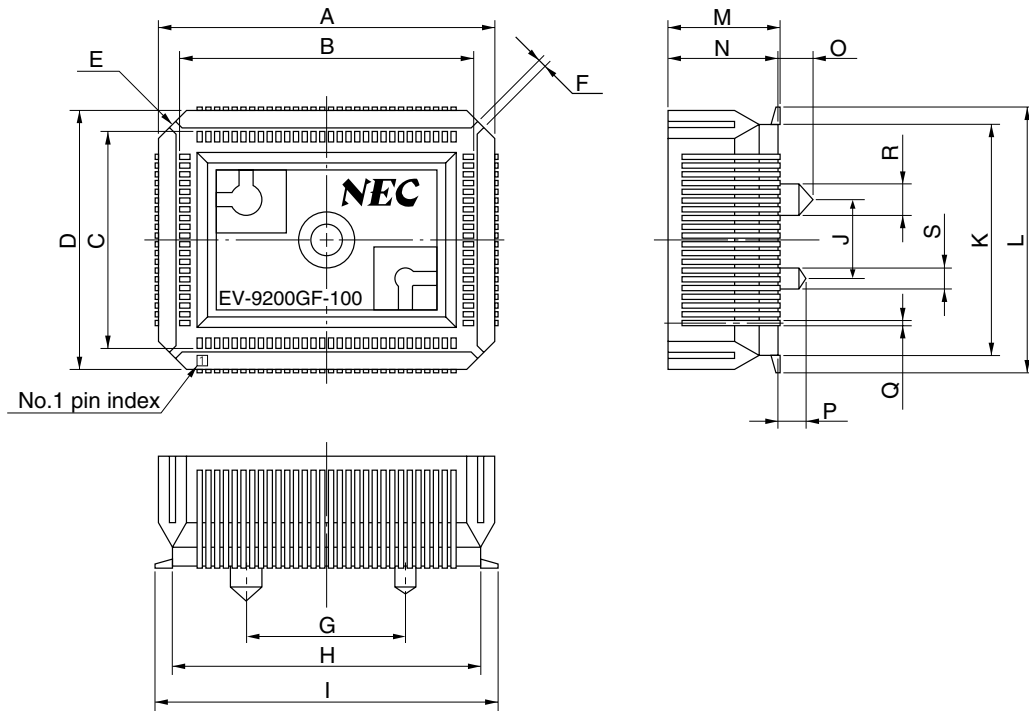


ITEM	MILLIMETERS	INCHES	ITEM	MILLIMETERS	INCHES
A	21.55	0.848	a	14.45	0.569
B	0.5x24=12	0.020x0.945=0.472	b	1.85±0.25	0.073±0.010
C	0.5	0.020	c	3.5	0.138
D	0.5x24=12	0.020x0.945=0.472	d	2.0	0.079
E	15.0	0.591	e	3.9	0.154
F	21.55	0.848	f	0.25	0.010
G	φ3.55	φ0.140	g	φ4.5	φ0.177
H	10.9	0.429	h	16.0	0.630
I	13.3	0.524	i	1.125±0.3	0.044±0.012
J	15.7	0.618	j	0-5°	0.000-0.197°
K	18.1	0.713	k	5.9	0.232
L	13.75	0.541	l	0.8	0.031
M	0.5x24=12.0	0.020x0.945=0.472	m	2.4	0.094
N	1.125±0.3	0.044±0.012	n	2.7	0.106
O	1.125±0.2	0.044±0.008			
P	7.5	0.295	TGC-100SDW-G1E		
Q	10.0	0.394			
R	11.3	0.445			
S	18.1	0.713			
T	φ5.0	φ0.197			
U	5.0	0.197			
V	4-φ1.3	4-φ0.051			
W	1.8	0.071			
X	C 2.0	C 0.079			
Y	φ0.9	φ0.035			
Z	φ0.3	φ0.012			

note: Product of TOKYO ELETECH CORPORATION.

Drawings of Conversion Socket (EV-9200GF-100) and Recommended Footprints

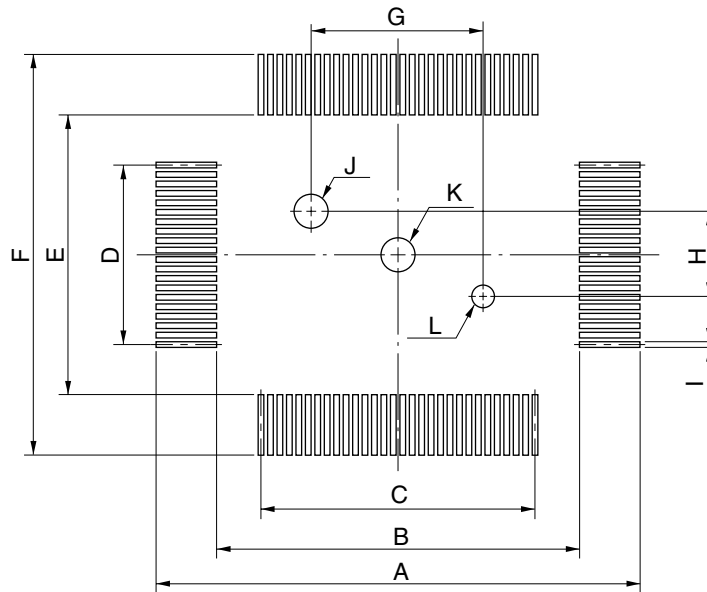
Figure A-2. Drawing of EV-9200GF-100 (for Reference Only)



EV-9200GF-100-G0E

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-3. Recommended Footprints of EV-9200GF-100 (for Reference Only)



EV-9200GF-100-P1E

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65 \pm 0.02 \times 29 = 18.85 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNT MANUAL" website (<http://www.necel.com/pkg/en/mount/index.html>).

★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name		Document No.
μPD780308, 780308Y Subseries User's Manual		U11377E
μPD780306, 780308 Data Sheet		U11105E
μPD780306Y, 780308Y Data Sheet		U12251E
μPD78P0308, 78P0308Y Data Sheet		This document
78K/0 Series Instructions User's Manual		U12326E
78K/0 Series Application Note	Basic (III)	U10182E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K Series System Simulator Ver.2.30 or Later	Operation (Windows Based)	U15373E
	External Part User Open Interface Specifications	U15802E
ID78K Series Integrated Debugger Ver.2.30 or Later	Operation (Windows Based)	U15185E
RX78K0 Real-Time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver.3.12 or Later (Windows Based)		U14610E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name		Document No.
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78K0-NS-A In-Circuit Emulator		U14889E
IE-78K0-NS-PA Performance Board		To be prepared
IE-780308-NS-EM1 Emulation Board		U13304E
IE-78001-R-A In-Circuit Emulator		U14142E
IE-780308-R-EM Emulation Board		U11362E

Documents Related to PROM Programming (User's Manuals)

Document Name		Document No.
PG-1500 PROM Programmer		U11940E
PG-1500 Controller	PC-9800 series (MS-DOS™) Based	EEU-1291
	IBM PC series (PC DOS™) Based	U10540E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Products and Packages –	X13769X
Semiconductor Device Mount Manual	Note
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (<http://www.necel.com/pkg/en/mount/index.html>).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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800-366-9782

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"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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