

Introduction



The HFA3724 is a highly integrated IF strip and baseband converter for half duplex wireless data applications. It features all the necessary blocks for baseband demodulation and

modulation of "I" and "Q" quadrature multiplexing signals. It targets applications using all phase shift types of modulation (PSK) due to its limiting receiving front end. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. Figure 1 depicts the simplified block diagram of the HFA3724.

The HFA3724 has a two stage integrated limiting IF amplifier with frequency response to 400MHz. These amplifiers exhibit a -84dBm, -3dB cascaded limiting sensitivity with a built in Receive Signal Strength Indicator (RSSI) covering 60dB of dynamic range with excellent linearity. An up conversion and down conversion pair of quadrature doubly balanced mixers are available for "I" and "Q" baseband IF processing. These converters are driven by an internal quadrature LO generator which exhibits a broadband response with excellent quadrature properties. For broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for

modulation/demodulation. A buffered, divide by 2, LO single ended 50Ω selectable output is provided for convenience of PLL designs. The receive down converter mixers "I" and "Q" outputs have a frequency response up to 30MHz for Baseband signals and the transmit mixers outputs are summed and amplified to a single ended open collector output with frequency response up to 400MHz.

Multiplexed or half duplex baseband 5th order Butterworth low pass filters are also included in the design. The "I" and "Q" filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or analog to digital conversion in the receive channel. During transmission, the filters are used for pulse shaping and control of spectral mask.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected and can be fine tuned for optimization of spectrum output responses.

Ordering Information

PART NUMBER	PKG. NO.
HFA3724EVAL	Evaluation Kit

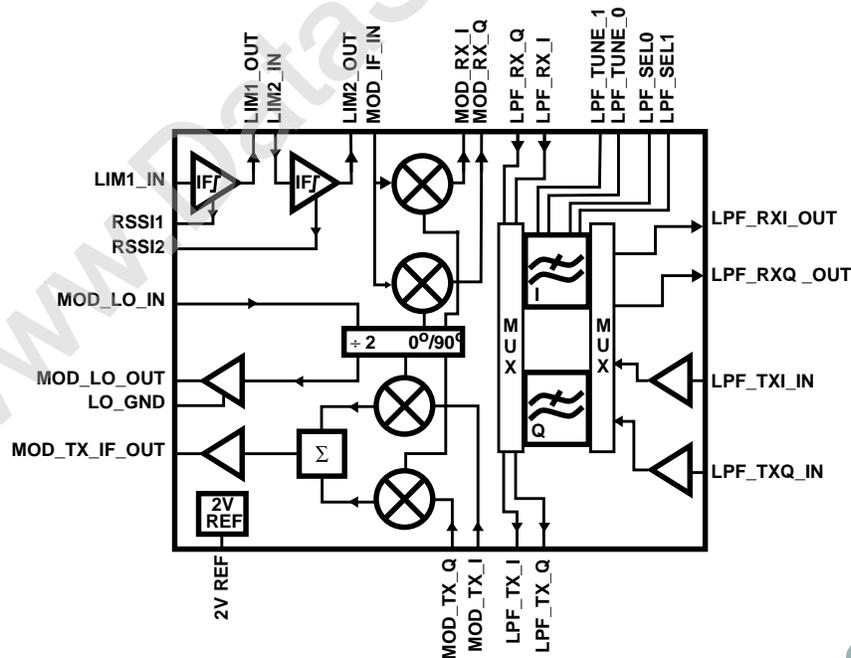
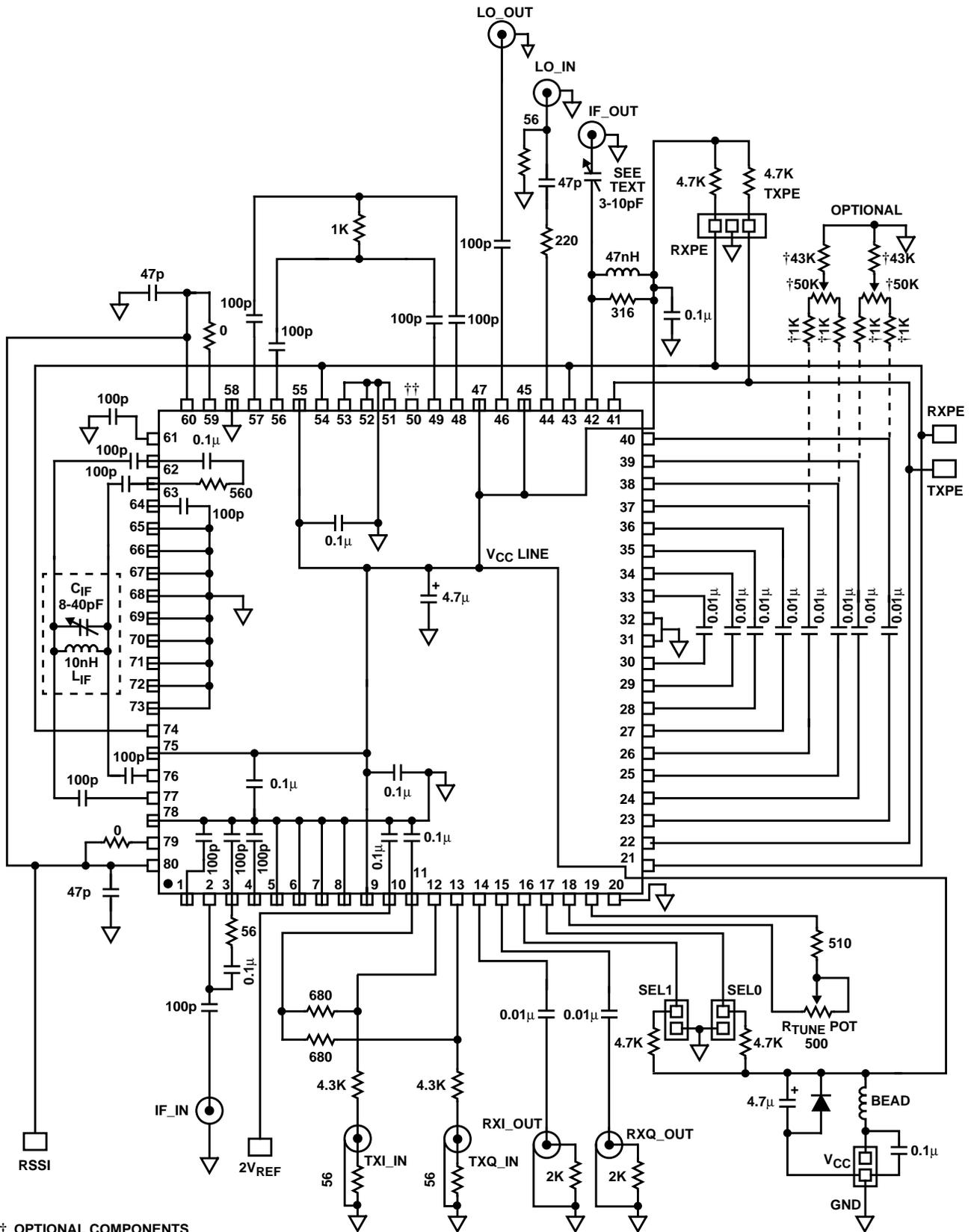


FIGURE 1. BLOCK DIAGRAM



† OPTIONAL COMPONENTS
 †† CONNECT TO GND TO ENABLE LO_OUT
 CAPACITORS MEASURED IN FARADS
 RESISTORS MEASURED IN Ω

□ = FLAT CABLE CONNECTOR

FIGURE 2. EVALUATION BOARD SCHEMATICS (VER. 5)

Board Description

An electrical schematic of the evaluation board is shown on Figure 2. The typical test diagram shown on page 13 of the HFA3724 Data Sheet has been implemented with few modifications to aid to the evaluation of the device in typical applications.

Pull up resistors to V_{CC} of 4.7K have been added to the control pins together with shorting jumpers to ground to facilitate setting up the device into transmit and receive modes as well as the programmable Low Pass Filters.

The IF input to the Limiters is resistively terminated in 50 Ω . This simplifies the matching at the expense of limiter Noise Figure. The NF is approximately 9dB in this configuration as opposed to 6dB in a 250 Ω environment, such as shown in the Typical Application Diagram in the data sheet.

The interstage limiter filter is adjusted to a center frequency of 280MHz by means of an adjustable capacitor.

The receive I/Q outputs are terminated on board with 2k Ω resistors.

The transmit Digital (TTL) I/Q inputs are terminated on board with 50 Ω . A 4.3K and 680 Ω attenuator is built in the evaluation board in case the transmit inputs need to interface with a TTL drive signal with no 50 Ω load capabilities. The 50 Ω chip resistors need to be removed in this case.

The transmit IF output is conveniently matched to 50 Ω at 280MHz with a network with an adjustable capacitor.

Provision has been made to add potentiometers to reduce carrier suppression. These components are not installed.

A potentiometer and a resistor totalling 1k Ω have been added to the Low Pass Filter fine tuning pins for convenience of the evaluation. The boards have been adjusted for a -35dBc main lobe to side lobe difference by using the selectable 8.8MHz filter tuned low (R_{TUNE} value is approximately 900 Ω).

Version 5 layout addresses an option to connect pin 50 (LO_GND) to ground. This pin has been left disconnected from ground in the present layout. A solder bridge must be placed from pin 50 to pin 51 when the LO_OUT signal is required.

A flat cable connector is provided when interfacing with the Intersil HSP3824 Baseband processor. The RSSI output can be monitored at its respective pin.

Figure 19 and Figure 20 show the access and adjustment points for the evaluation board.

Evaluation Notes (Version 5)

Proper antistatic procedures must be used when handling the HFA3724 evaluation board.

When testing the receive demodulator sensitivity please remove the transmit baseband digital signals to avoid crosstalk.

Please terminate the LO_OUT output port into 50 Ω when enabling the LO_OUT output. Leaving this port mismatched reduces the carrier suppression of the transmit signal.

When evaluating power consumption in stand by mode, please remember that most of the jumpers are pull up resistors which can add up to the total I_{CC} when jumpers are placed to ground.

Do not add significant external capacitive loading to the I/Q receive ports. Measure these ports with low capacitance scope probe adapters or high impedance low capacitance vector voltmeter probes. High impedance low capacitance active probes for network analyzers can also be used.

Proper TTL driving capability and rise and fall time balance is important for code leakage evaluation of spread spectrum signals. Make sure that the TTL data inputs are below V_{CC} .

When interfacing with a HSP3824 evaluation board, make sure that the available HSP3824 board version can provide transmit signals with 50 Ω capability, otherwise remove the two termination resistors from this evaluation board (HFA3724EVAL).

The pot R_{TUNE} can assume very low values when evaluating the tuning range. It is advisable to contain this value within a $\pm 30\%$ of the center value. Too low values can cause power up problems to the LPF biasing scheme. The resistance value can be read with an ohmmeter when the device is turned off.

Evaluation Description

Demodulator Tests

DEMODULATOR SENSITIVITY TESTS

Please refer to Figure 5A and Figure 5B for a simplified block diagram and typical test set up. The evaluation board is set to Receive by placing a shorting jumper to the RX pins. The LPF filter setting (SEL0, SEL1) is to be set according to the desired baseband frequency of operation as explained below.

A signal generator is connected to the IF_IN SMA input and set to a CW frequency of 280MHz. This generator is used to provide a simulated IF input signal to the device. In case the generator is not capable of accurate low RF output levels, a step attenuator can be used at its input in order to accurately provide very small RF levels to the HFA3724 IF input. Note that the IF input frequency is set to the center of the intermediate bandpass filter frequency set in the evaluation board by L_{IF} and C_{IF} as in the board schematics, Figure 2.

A second signal generator is connected to the LO_IN port to provide the local oscillator frequency. This input frequency must be always twice the reference LO frequency and will be referred as 2XLO for most of this document. As the "I" and "Q" baseband outputs frequency is dependent on the difference in frequency of the ref LO and the IF input, the user can choose any desired 2XLO frequency such that

absolute difference in frequency between the ref LO and the IF input is within the baseband of the LPF filter.

Because the 2XLO input port is broad band (10MHz to in excess of 820MHz), all LPF filter settings can be evaluated. As in the example of Figure 5B, the LO input frequency has been chosen to be of 286MHz (2XLO of 572MHz) as high-side injection (LO higher than the IF frequency) and the “I” and “Q” outputs frequency is of 6MHz. A LPF setting of 8.8MHz (SEL1 = High - no jumper and SEL0 = Low - shorting jumper) can then be used.

LIMITER OUTPUT TEST: OPTIONAL

One of the features of the high gain IF limiter chain is its stability and spur free spectrum. The limiter chain output can be tested by probing one of the outputs of the second limiter (pin 56 or 57) by using a high frequency very low capacitance AC coupled resistive probe like a HP54006A. The evaluation board itself does not provide a simpler hook up for this test as degradation of signal could occur.

The probe resistive impedance is of 1kΩ and can be connected to a spectrum analyzer for evaluation of spectrum purity and sensitivity. Figure 3A and Figure 3B show typical spectrum responses of the limiter amplifier chain with input signals of -90dBm, -70dBm and -50dBm at 280MHz respectively. Notice the “bump” created by a bandpass action of the intermediate band pass filter (L_{IF}, C_{IF}) and resulting noise bandwidth amplification. As limiting starts to occur as in Figure 3B, the noise floor level is decreased accordingly (Limiter action on noise).

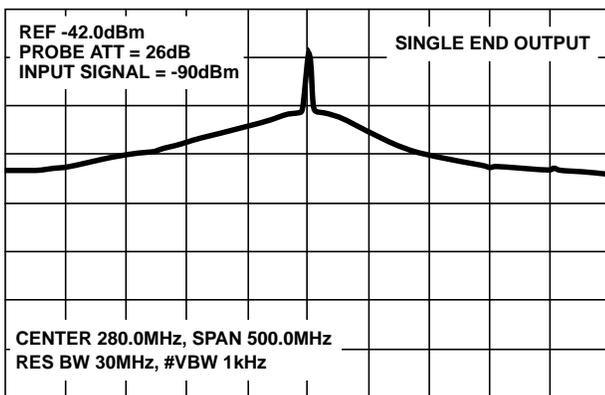


FIGURE 3A. LIMITER OUTPUT SPECTRUM IF = -90dBm

DEMODULATOR SENSITIVITY TESTS

With an “I” and “Q” output frequency of 6MHz and a LPF setting of 8.8MHz, the user can start with a IF signal of -30dBm at 280MHz and observe both “I” and “Q” outputs with a oscilloscope or spectrum analyzer with a high impedance probe. The output signals must be in quadrature, (90 degrees apart) and with a level of approximately 500mV_{P-P}. When decreasing the IF input signal, to -50, and -70dBm, these “I” and “Q” signals must keep the same amplitude due to the limiting action of the IF limiting amplifiers. Further reduction of

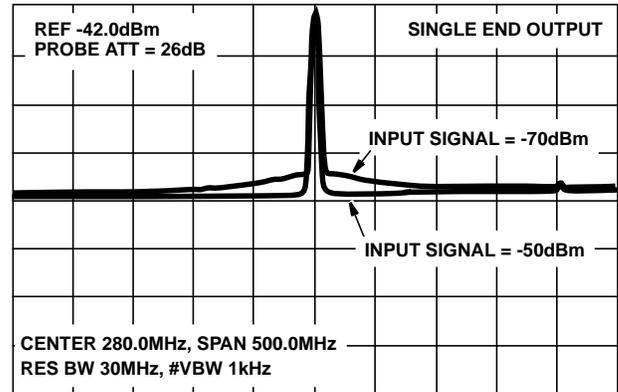


FIGURE 3B. LIMITER OUTPUT SPECTRUM IF = -70dBm, -50dBm

the IF input will show some decrease in the “I” and “Q” amplitudes up to the -3dB point where the 3dB sensitivity occurs. It is important to note that at very low level IF input signals these outputs will show a little smearing as observed in a oscilloscope. The use of a spectrum analyzer will improve the -3dB sensitivity measurement. It is also important to note that because the intermediate IF filters are set as wide band, (approximately 47MHz) some output noise energy starts to propagate to the “I” and “Q” outputs during this sensitivity evaluation.

DEMODULATOR QUADRATURE TESTS

As in the sensitivity test, the “I” and “Q” outputs as observed in a oscilloscope, or a vector voltmeter, will be in quadrature (where their phase relationship is of 90 degrees) with any reasonable IF input levels beyond sensitivity.

NOTE: For High-Side injection (ref LO higher than the IF frequency) the “I” channel leads the “Q” channel by 90 degrees. For Low-Side injection (548MHz 2XLO or 274MHz ref LO as in our example), the “I” channel lags the “Q” channel by 90 degrees.

A vector voltmeter can be used to evaluate the phase difference or phase balance as well as the amplitude balance of the “I” and “Q” channels for various IF input levels.

When performing these tests and moving the LO frequency for different “I” and “Q” output frequencies, the user will observe what seems to be a distortion in the output signals when these frequencies are well below the 3dB roll off characteristics of the HFA3724 LPF filters. This apparent distortion is a result of the LPF response to a limited output which resembles a square wave (hyperbolic tangent function). In our example of a 6MHz output and a LPF filter setting of 8.8MHz, the outputs look sinusoidal.

LOW PASS FILTER TESTS

These tests shall be performed by using a vector voltmeter or a spectrum analyzer. Both instruments lock in the fundamental frequency of the “I” and “Q” outputs where accurate 3dB roll off characteristics must be tested.

All LPF settings can be tested by varying the 2XLO frequency generator accordingly. The user need to use caution for very low frequency “I” and “Q” signals because of the use of coupling capacitors in the evaluation board from the down converter mixers to the LPF input and from the LPF output to the on board 2kΩ resistor load. These components create a high pass filter action with a 3dB point of approximately 15kHz for 0.01μF decoupling capacitors.

An indirect method of the 3dB LPF filter evaluation is by setting a reference signal to the vector voltmeter at 1MHz for example (562MHz 2XLO as in our example). This level corresponds to a 0dB when this reference signal is saved in the voltmeter. Increasing the 2XLO frequency in fine steps will start moving the reference down until the vector voltmeter reads -3dB. This frequency setting (2XLO) is divided by 2 and subtracted from the IF frequency of 280MHz (for example) to find the 3dB point of the LPF filter. Note: Some vector voltmeters cannot scan or keep probe amplitude calibration for different frequencies and errors can occur.

As all LPF filter settings (2.2, 4.4, 8.8 and 17.6MHz) are slightly different from each other, it is suggested to calibrate a new reference 1MHz signal for each of the desired settings.

Another method of low pass characteristics evaluation is by using a network analyzer. Although a little more complicated, this method is useful to evaluate the overall group delay characteristics of the Demodulator at all LPF settings and will be explained later in this section.

RSSI TESTS

The RSSI characteristics of the HFA3724 can be evaluated by monitoring the voltage level at the RSSI output pin available in the evaluation board. This pin is located and labelled in a flat cable connector used to interface with the Intersil HSP3824 Base Band Processor.

The CW IF input level is varied from -90dBm to 0dBm for example, in steps, and the corresponding voltages in the RSSI output can be monitored and recorded. A typical RSSI output curve is depicted in Figure 4.

The RSSI output pin is sensitive to long wire loops as it can generate signal feedback to the IF input. This situation can lead to possible oscillation or increase in spurs from the IF amplifier outputs. Use caution when using long lead voltmeter probes at this pin. When performing the limiter output spectrum check earlier in this section, the user can make an assessment of the sensitivity of the RSSI line by placing and removing lead voltmeter wires at the RSSI test point.

The HFA3724 RSSI outputs are a sum of the two current outputs of each of the limiters. These current sources have been summed together through two on chip 6kΩ resistor in parallel. Zero ohm resistors have been added to feed the current outputs to the respective resistor pins (pins 60 and 80).

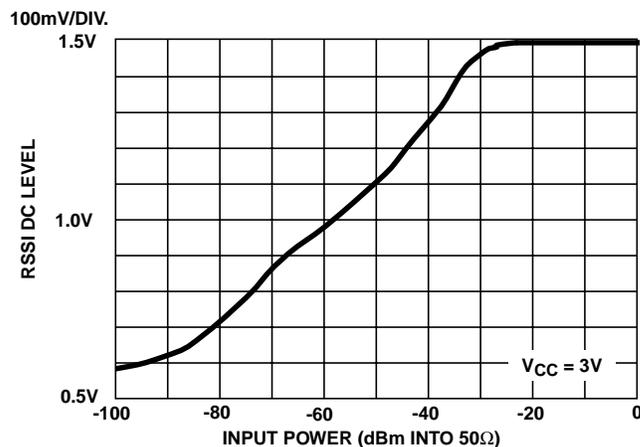


FIGURE 4. TYPICAL RSSI RESPONSE

The user can modify the voltage range when required, by having the two current outputs summed through a different resistor value.

Demodulator Group Delay Characteristics

Group delay and filter passband characteristics can be evaluated by a network analyzer by using a set up as in Figure 6.

The network analyzer generator sweep baseband signal is upconverted to an IF signal by a doubly balanced mixer. The IF signal is a double side band suppressed carrier signal contrary to a CW signal as in the previous sensitivity tests paragraphs. This DSB signal can be conveniently used for the “I” and “Q” evaluation individually when a proper phase shift technique is used. The doubly balanced mixer must have a reasonably RF input frequency response down to a few hundreds of kilohertz and good passband characteristics across a 40MHz bandwidth which is very common for broad band diode mixers. The network analyzer generator output is split between its reference input “R” and the RF port of the mixer. A 280MHz signal generator is used for the LO input of the mixer and also as a reference LO for the HFA3724. The 2XLO signal for the LO_IN input of the device is generated by an off the shelf frequency doubler (a second generator locked to the 280MHz generator is not suggested unless they have very good phase lock characteristics). The output of the frequency doubler is routed through a line stretcher for phase shift control.

Mathematical manipulation of a double side band input signal and the response of a quadrature demodulator suggests a phase relationship between the LO and the input signal such that one and only one of the outputs “I” and “Q” signals is present. The line stretcher is used to cancel the channel not being evaluated.

The outputs “I” and “Q” result from the following trigonometric equations:

$$I = 1/2\cos(\omega_m t - \theta) + 1/2\cos(\omega_m t + \theta) \text{ and}$$

$$Q = 1/2\sin(\omega_m t - \theta) - 1/2\sin(\omega_m t + \theta)$$

Where ω_m is the network analyzer frequency in radians and Θ is the phase shift between the IF input and the LO signal. In the case of a full "I" signal, the phase Θ needs to be zero. For a full "Q" signal, the phase Θ needs to be of -180 degrees.

The "T" channel of the network analyzer is used to monitor the "I" or the "Q" channel output. The analyzer T/R ratio for magnitude and phase responses from 500kHz to beyond the 3dB points can be displayed. Some network analyzers can also compute the group delay automatically. A typical Group delay and frequency response characteristic is depicted in Figure 7A and Figure 7B.

Group delay and 3dB response balance between "I" and "Q" output signals can also be evaluated when desired.

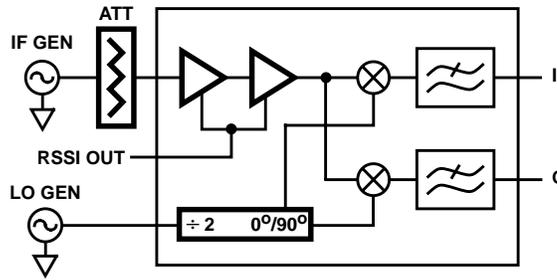


FIGURE 5A. SIMPLIFIED DEMODULATOR BLOCK DIAGRAM

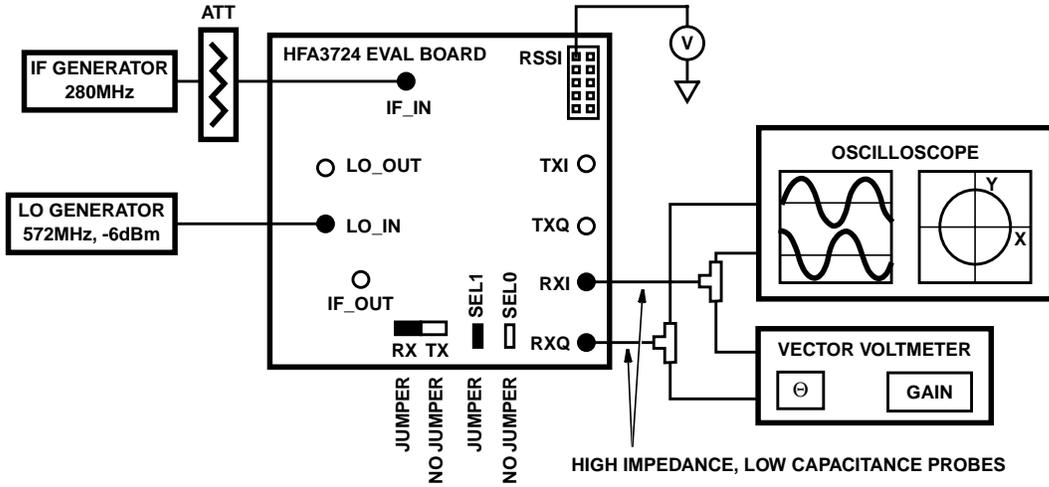


FIGURE 5B. TYPICAL TEST SETUP

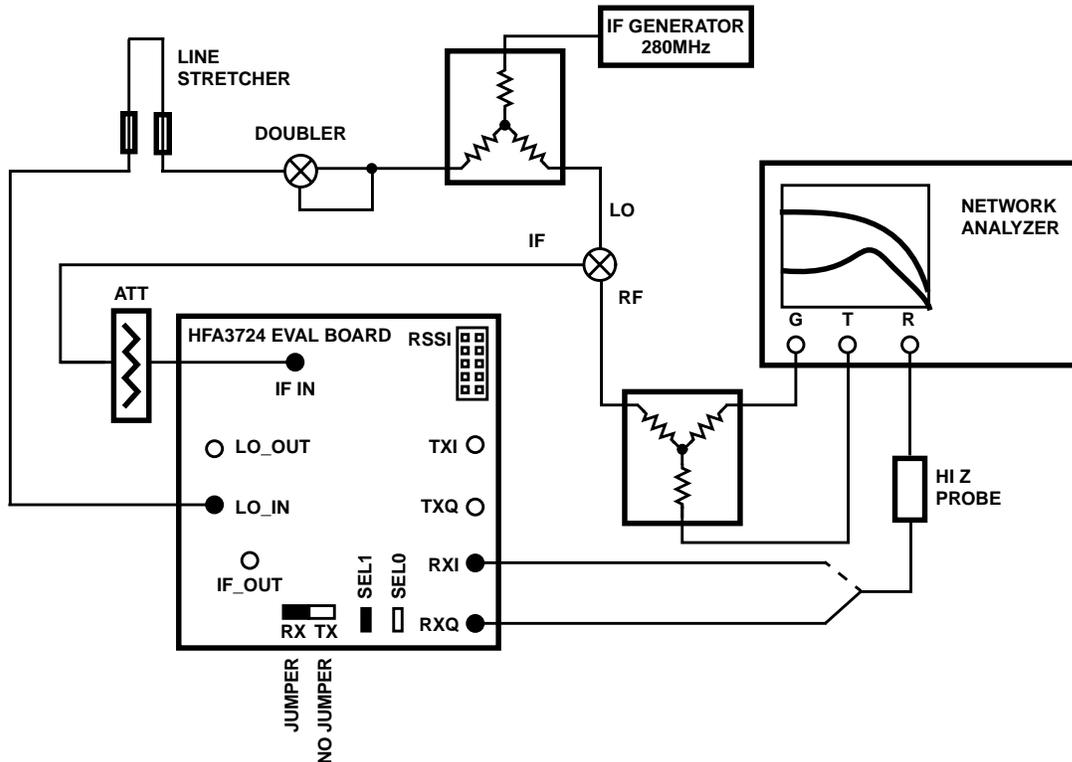


FIGURE 6. EVALUATING DEMODULATOR LPF CHARACTERISTICS AND GROUP DELAY

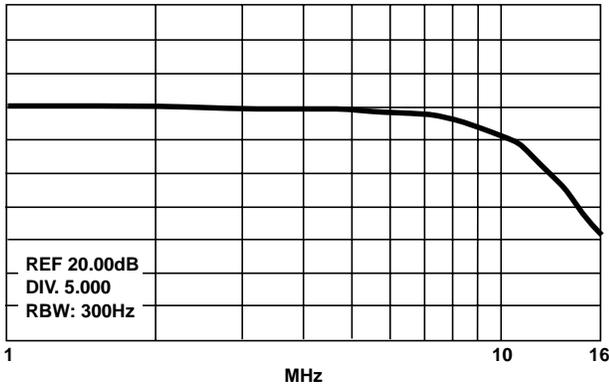


FIGURE 7A. TYPICAL LPF AMPLITUDE RESPONSE AT 8MHz

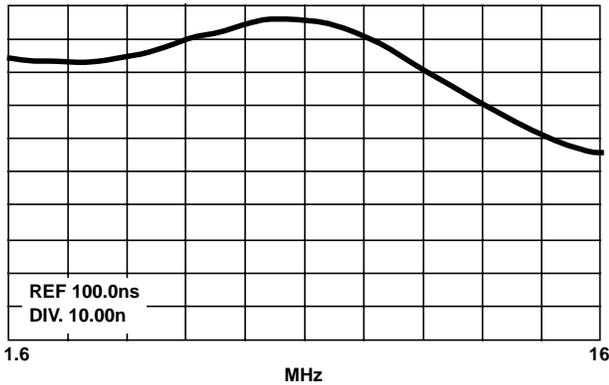


FIGURE 7B. TYPICAL DEMODULATOR GROUP DELAY AT 8MHz

Modulator Tests

SINGLE SIDE BAND CHARACTERISTICS

Please refer to Figure 9A and Figure 9B for a simplified block diagram and a typical test set up. The evaluation board is set to Transmit by placing a shorting jumper to the TX pins. The LPF filter setting (SEL0, SEL1) is to be set according to the desired baseband frequency of operation.

One of the figures of merit of a Vector or Quadrature Modulator is its the SSB characteristics. Phase and amplitude balance characteristics of this type of modulator are combined and are reflected directly into how good a sideband is suppressed. By using two accurate 90 degrees apart (cosine and sine) input signals into the “I” and “Q” baseband inputs, a quadrature modulator will output a single side band signal. Simple trigonometric mathematical manipulation of these signals (Baseband and Carrier or LO) yield a suppressed side band from the classical dual side band signal generated by multiplication, in a single mixer, of a Carrier (LO) and a modulating signal. The same concept can be used to prove that if the baseband signals are in phase, a dual side band, suppressed carrier output signal is generated by a quadrature modulator.

Another important consideration is carrier suppression, which is often referred as LO leakage. This parameter does not depend on amplitude and phase characteristics of a quadrature modulator but is a result of how well balanced

are the upconverter mixers. This check is also carried out during the SSB tests.

The HFA3724 Modulator “I” and “Q” baseband inputs are TTL compatible i.e., they are equivalent to comparator inputs which output square waves before any filtering takes place. In other words, the baseband signals for testing the device have to be TTL compatible. 90 degrees apart TTL signals with a very accurate phase relationship must be generated in order to evaluate the device for single side band characteristics. As square waves are composed of the fundamental and odd harmonics, all previous math concepts are still valid for square wave signals.

CHOICE OF LPF

The transmit low pass filters are used to preshape the comparator output square waves as desired by the user, therefore bandlimiting the output signal due to the frequency translation during upconversion. The LO signal, now referred as a “Carrier” is also generated by the 2XLO input. The choice of the LPF is made based upon which baseband frequency is to be upconverted such that a desired pre shaping takes place. Figure 8A and Figure 8B show a typical SSB output for two 90 degrees apart 5MHz square wave signals. Only the fundamental of the square wave signal is depicted in Figure 8A as the LPF filters take care of attenuating their harmonics.

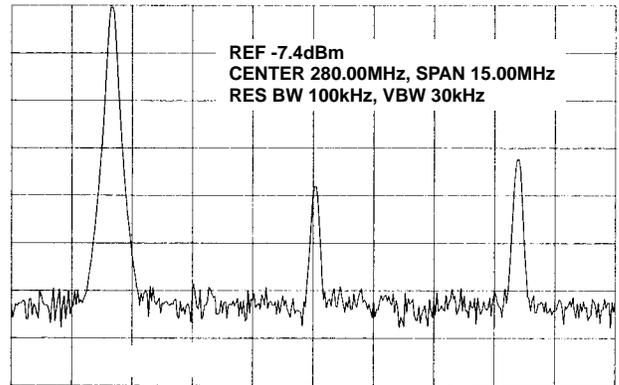


FIGURE 8A. NARROW SPAN SSB CHARACTERISTICS

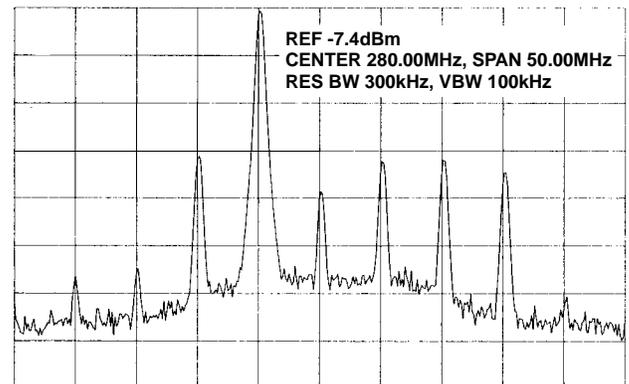


FIGURE 8B. WIDE SPAN SSB CHARACTERISTICS

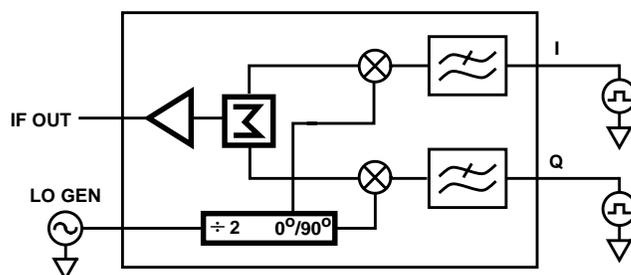


FIGURE 9A. SIMPLIFIED MODULATOR BLOCK DIAGRAM

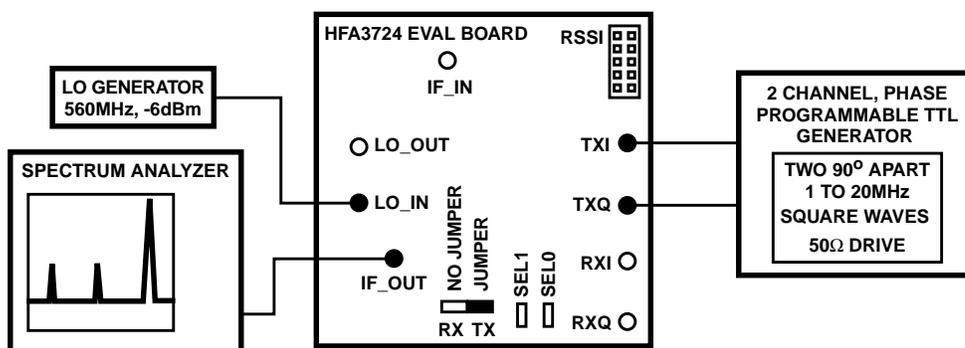


FIGURE 9B. TYPICAL MODULATOR TEST SET UP

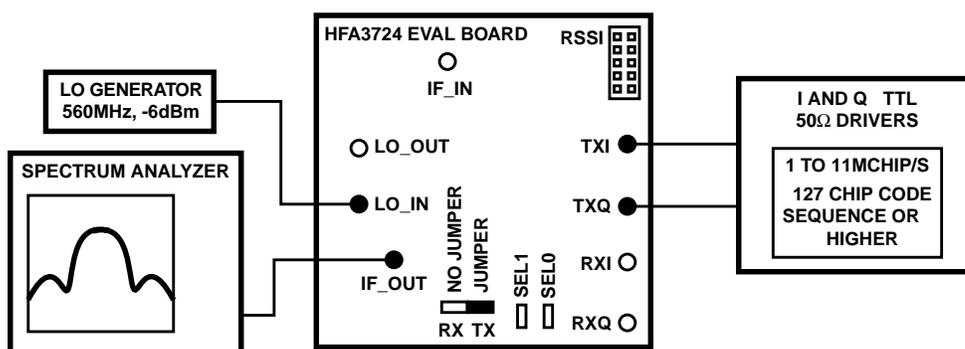


FIGURE 10. SPREAD SPECTRUM CHARACTERISTICS TEST SET UP

Carrier suppression as in Figure 8A is typically better than Figure 13 of the data sheet as the evaluation board does not make use of the LO buffer (Pin 50 is left floating). The built-in capability of the buffer causes a little carrier suppression degradation due to the high currents involved driving a 50Ω load.

NOTE: The HFA3724 modulator generates a lower sideband signal when the “I” input LEADS the “Q” input by 90 degrees.

During the SSB evaluation the user can change the square wave frequency and LPF filters setting, and observe the spectrum showing the typical bandpass filtering actions by a change in the “plateau” of noise floor. The user can also observe the attenuation of the harmonically related spectrum lines generated by a square wave when the fundamental lies within a desired passband (Figure 8B).

TRANSMIT LPF EVALUATION BY SPREAD SPECTRUM SIGNALS

The spread signal test set up is depicted in Figure 10.

The LPF filter characteristics can also be evaluated by a network analyzer with a test set up to be explained later. As the LPF filters are multiplexed between Transmit and Receive, most of the data like 3dB points and group delay characteristics are similar when compared by the tests performed for the Receive section.

In transmission applications, modulators and shaping filters need to be evaluated by the spectral response or spectrum shaping characteristics which include any nonlinear behavior across the transmitting chain. In the case of the HFA3724, non linearities of both the LPF filters and the Up conversion mixers responses can be evaluated by using a spread

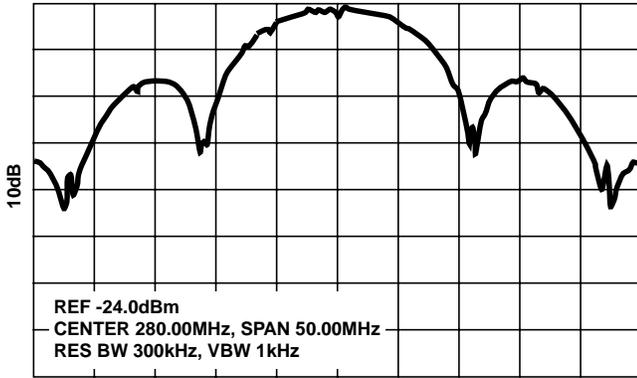


FIGURE 11A. SPREAD SPECTRUM RESPONSE AT LPF17.6 FOR AN 11MCHIPS/S BASEBAND SIGNAL

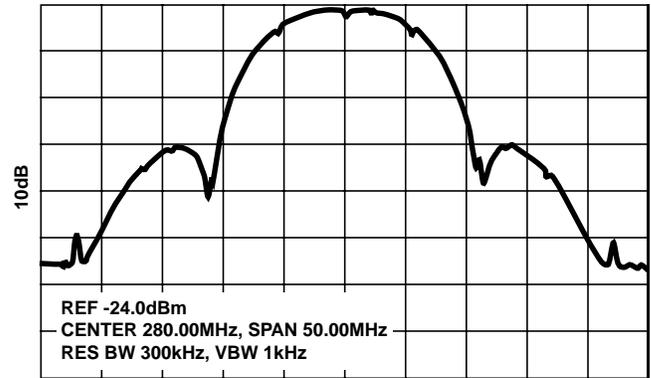


FIGURE 11B. RESPONSE AT LPF8.8, R_{TUNE} TUNED LOW (11MCHIPS/S)

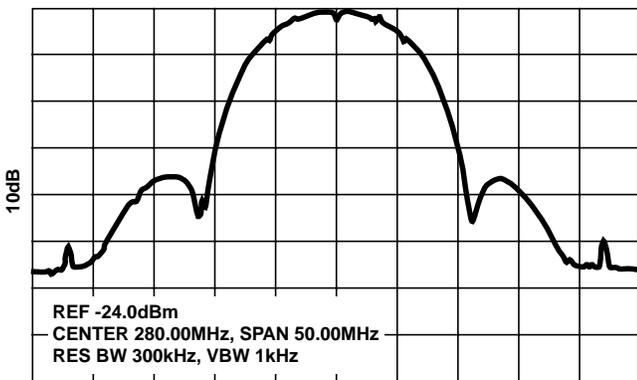


FIGURE 11C. RESPONSE AT LPF8.8, R_{TUNE} TUNED HIGH (11MCHIPS/S)

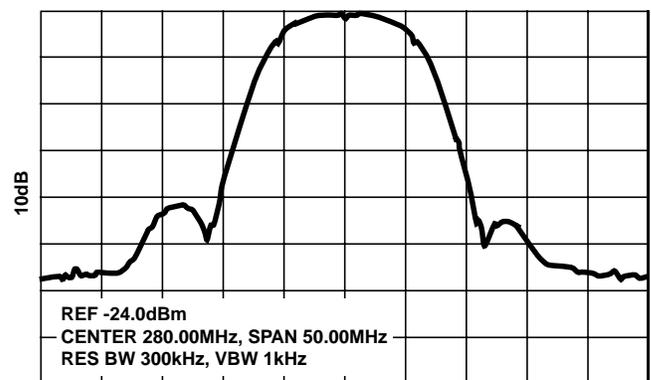


FIGURE 11D. RESPONSE AT LPF4.4, R_{TUNE} TUNED HIGH (11MCHIPS/S)

sequence input which shows any abnormal spectral regrowth and expected pulse shaping characteristics. Band limiting action and related spectrum shaping tunability can be exercised during these tests.

A long length spread sequence TTL I/Q generator, higher than $2^{11}-1$ or 2047 in length can be used to display a good spread characteristic when observed by a spectrum analyzer. The side lobe to main lobe attenuation resulting from the LPF shaping can then be monitored. The user have the option here to use the Intersil HSP3824 evaluation board as a suitable I/Q generator without any data at its input as the scrambler and the coding Barker sequence will spread the signal accordingly (the Spectrum shape looks just a little different than the ones depicted by Figure 11). Please refer to the HSP3824 Evaluation board application note.

The main lobe width of this signal is always twice the baseband frequency used for the “I” or “Q” signals whether they are in phase (same signal) or independent from each other as in quadrature input signals. The expected next upper and lower side lobes have a width of exactly the frequency of the baseband signals and have its peak dependent of the LPF characteristics and any nonlinearity in the chain. The LPF fine

tuning characteristics can be evaluated by changing the value of R_{TUNE} from $\pm 20\%$ from its nominal value.

Figure 11 shows a typical 11Mchips/s (11MHz) “I” and “Q” signal spread signal output spectrum and the spectrum shape variation when both LPF settings and R_{TUNE} are changed. Figure 11A shows the output spectrum of this signal with the highest setting of 17.6MHz (LPF17.6). Notice that little or no pre-shaping is taking place at that frequency and the spectrum resembles closely a sinc/x response. Figure 11B and Figure 11C show the variation of the sidelobe to main lobe characteristic for a R_{TUNE} variation of $\pm 10\%$ with the nominal setting of 8.8MHz (LPF8.8). Figure 11D shows the spectrum shape in case the 4.4MHz setting is used and R_{TUNE} is set for a frequency higher than 4.4MHz.

TRANSMIT LPF CHARACTERIZATION BY A NETWORK ANALYZER

Because the “I” and “Q” filtered transmit baseband signals are not readily available to be tested in the evaluation board unless a differential probe is used at the output of the LPF filters, an indirect method as depicted in Figure 14 can be used. The TTL signal need to be generated by a comparator/buffer combination circuit that is fed by the

network analyzer generator. This TTL signal will sweep as desired by the user. Only one of the channels must be evaluated at the time due to the summing of the upconverted "I" and "Q" signals. It is important to note that the input of a baseband signal of either "I" or "Q" by itself will generate a dual side band signal at the HFA3724 output. This dual side band signal is down converted back to the baseband by an external broad band doubly balanced mixer. The main restriction for the external mixer is its IF output frequency response which should cover from 500kHz and up. The external mixer receives its LO input from a 280MHz CW signal generator. The HFA3724 output signal is mixed down by this external mixer yielding a baseband signal to be monitored by the network analyzer. The HFA3724 2XLO is also generated by a doubler from the same 280MHz CW generator. Again, proper phase shift between the external 2XLO signal and the external mixer LO is required for proper operation of the down conversion process from a dual side band signal. A line stretcher is used and adjusted after the frequency doubler for maximum reading of the external mixer IF output.

Other Test Setups

Although most of the test set ups described earlier can evaluate the performance of the HFA3724, the reader is welcome to evaluate the device in a more system oriented manner with the common test procedures that follow:

Figure 15 depicts a common QPSK demodulation test set up for the HFA3724 using a Vector Signal Generator at a 280MHz carrier frequency, modulated by a spread digital sequence (Again, the HSP3824 evaluation board is more than suitable for this data generation). Coherence between the Carrier generator and the HFA3724 is done by the use of a line stretcher for the 2XLO signal and by tying the reference 10MHz signals often offered by these equipments. A modulation analyzer can be used for displaying the constellation characteristics and eye diagram results of the demodulation process. Figure 12 shows a typical Baseband QPSK constellation (Vector States) as the input to the Vector modulator used in Figure 15.

Figure 13A and Figure 13B depicts the constellation and eye diagram of the device for a 11MHz symbol rate with the LPF8.8 filter setting at 8MHz. The Carrier generator output signal has been set to -60dBm.

Another method, more realistic, which accounts for prefiltering before transmission (spectrum shaping) is using a second HFA3724 evaluation board as the generating signal carrier (The reader may ask "Why not use the same board in analog loop back mode?" As the LPF filters are multiplexed between Transmit and Receive and the ref LO is the same, this application is not possible).

Figure 16A shows a Modulation/Demodulation test setup. Figure 16B depicts the same set up by using the HSP3824 evaluation board as the baseband generator. Again, synchronization or coherence is needed for proper evaluation.

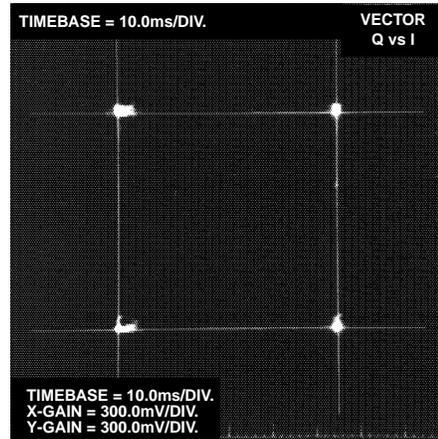


FIGURE 12. TYPICAL 11MHz QPSK BASEBAND CONSTELLATION

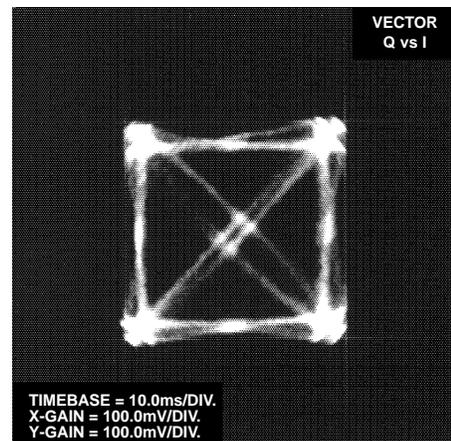


FIGURE 13A. HFA3724 DEMODULATOR OUTPUT CONSTELLATION

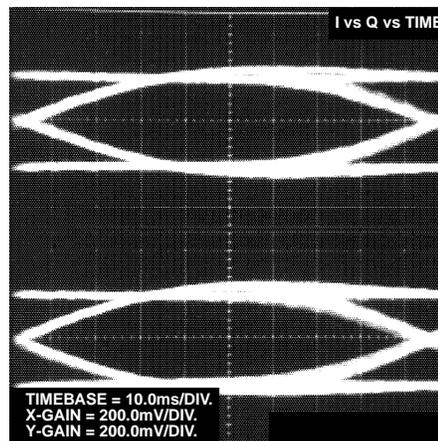


FIGURE 13B. HFA3724 DEMODULATOR EYE PATTERN

Contrary to a vector generator, which can have its output level well controlled, it is necessary to provide an attenuation path (attenuator) from the output of the HFA3724 transmitting board to the IF input of the receiving board for sensitivity level evaluation. (The output signal is approximately -7dBm.)

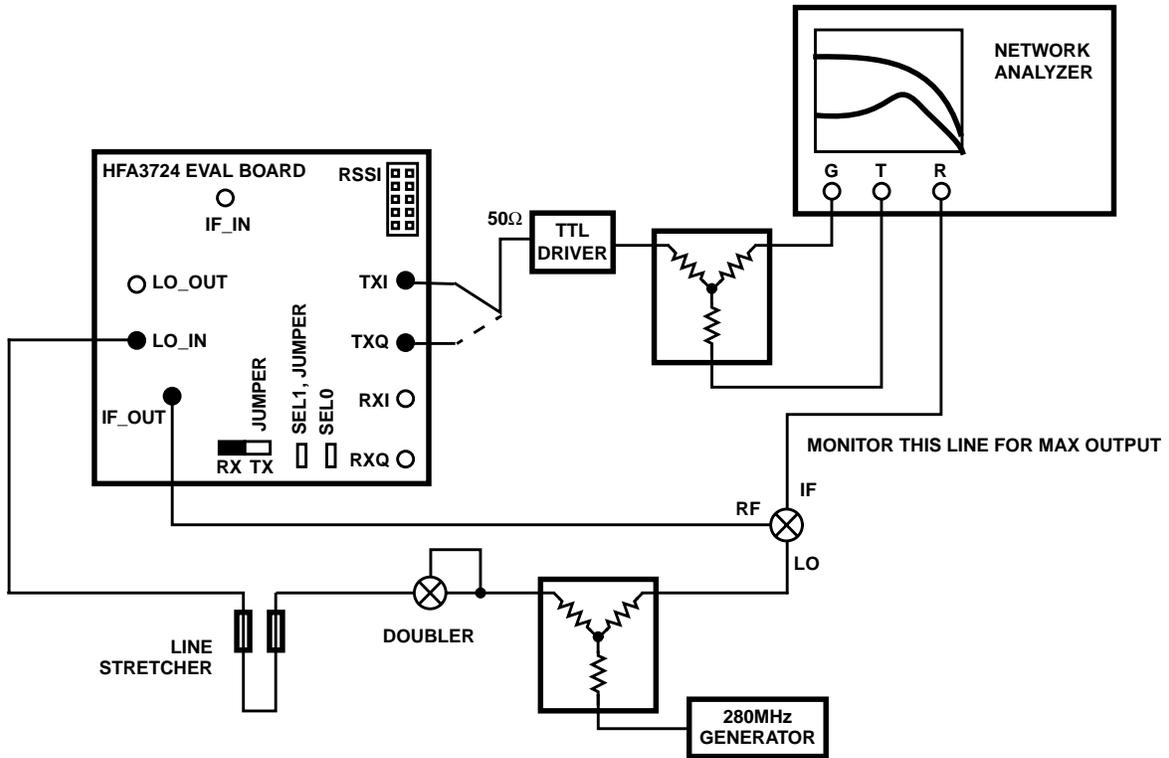


FIGURE 14. EVALUATING MODULATOR LPF CHARACTERISTICS AND GROUP DELAY

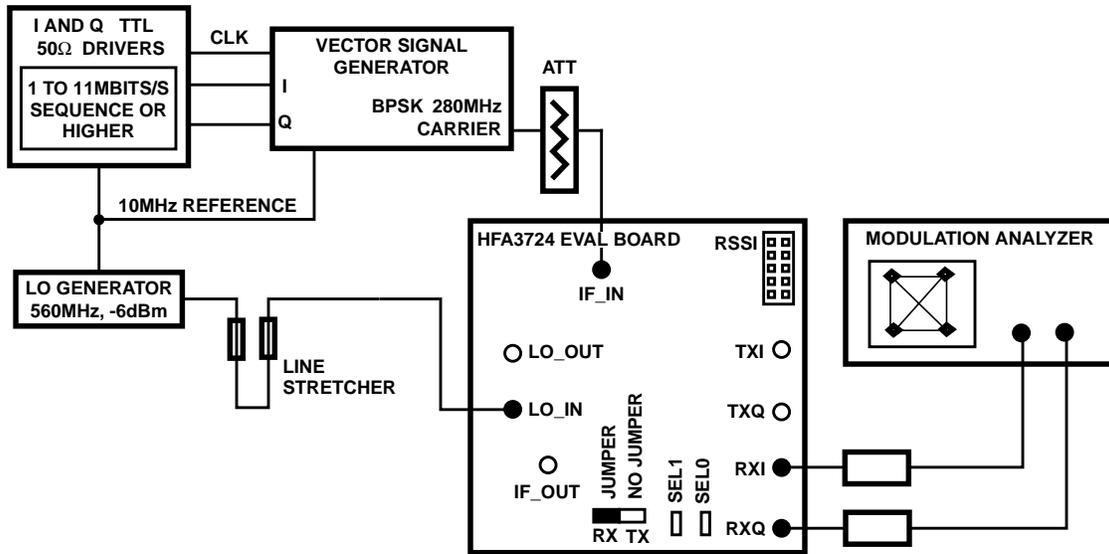


FIGURE 15. HFA3724 DEMODULATOR TEST SETUP

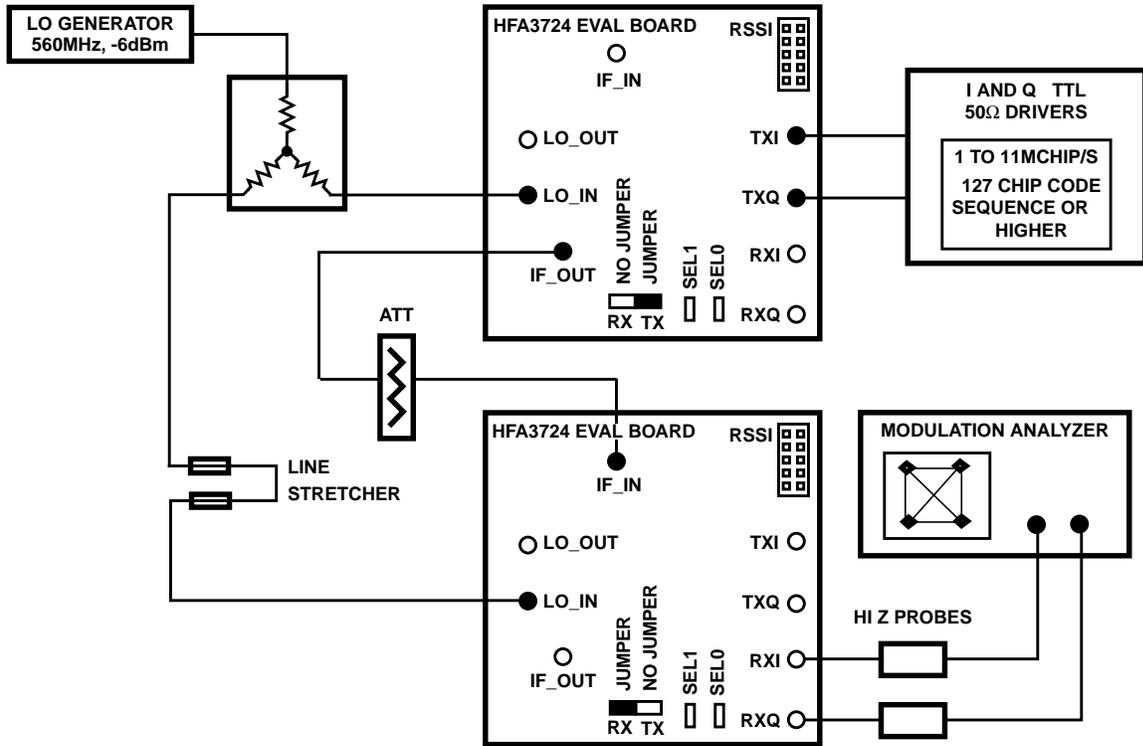


FIGURE 16A. MODULATION/DEMODULATION TEST SETUP

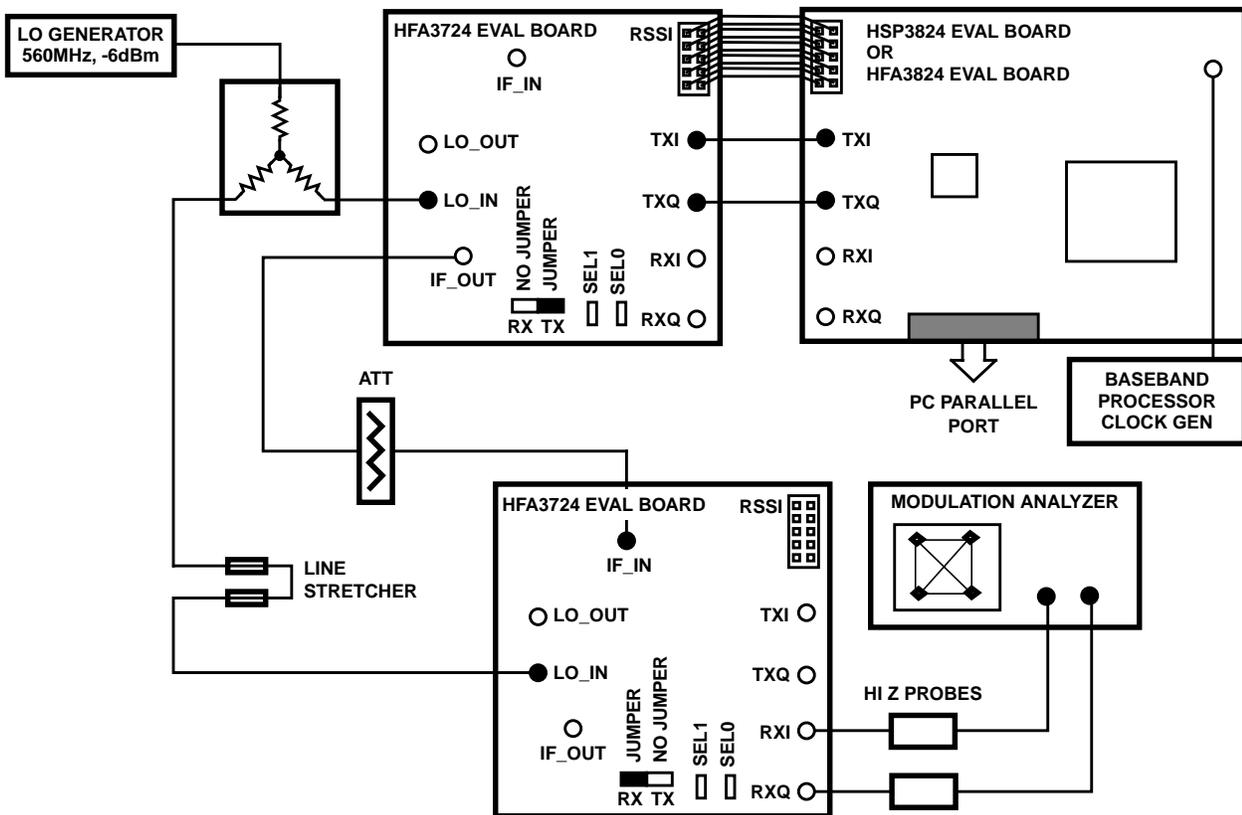


FIGURE 16B. ALTERNATIVE DEMODULATION TEST SET UP

Figures 17A and 17B show the Constellation and Eye diagram for the set up of Figure 16A at 11MHz symbol rate (QPSK). Notice the impact on both diagrams when spectral shaping is required at the transmit output.

Figure 18 setup is used for BER testing using two HFA3724 evaluation boards and one full duplex HSP3824 evaluation board.

The output signal from the Transmitting board can be summed with noise and bandlimited for proper E_b/N_0 or C/N evaluation versus BER. Please refer to the HSP3824 application notes.

Final Comments

The HFA3724 evaluation board is shipped and tuned for an IF of 280MHz at the output of the Modulator. The interstage

limiter band pass filter has also been tuned for a 280MHz center frequency and 47MHz of bandwidth. Modifications to the evaluation board for different IF frequencies and bandwidths are very straightforward (Please refer to the HFA3724 data sheet for IF bandlimiting component calculations and S22 data for the IF modulator output). Data rates and data formats must be carefully analyzed when dealing with coupling capacitors between each one of the HFA3724 stages. A compromise of TX/RX switching times and high pass characteristics of these coupling schemes need to be assessed for proper operation of the device depending on the final application. High value coupling capacitors are used for low data rates with the expense of switching times although the HFA3724 has keep alive circuits to hold fixed DC levels to both ends of the coupling capacitors.

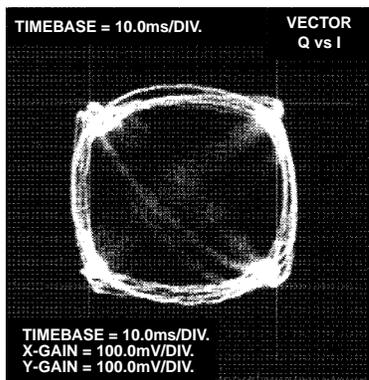


FIGURE 17A. CONSTELLATION DIAGRAM, SETUP OF FIGURE 16A

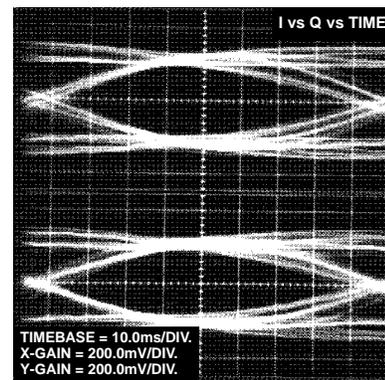


FIGURE 17B. CONSTELLATION DIAGRAM, SETUP OF FIGURE 16A

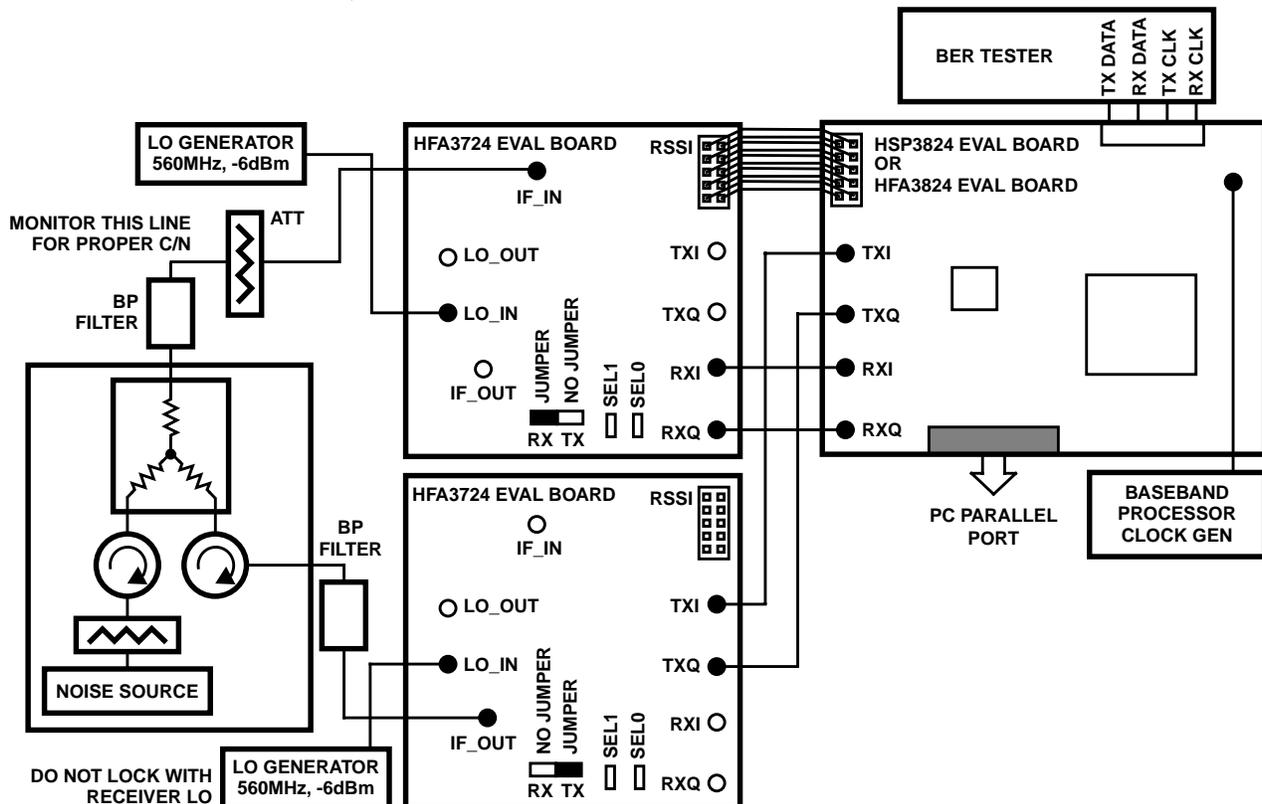


FIGURE 18. BER vs E_b/N_0 TEST SETUP

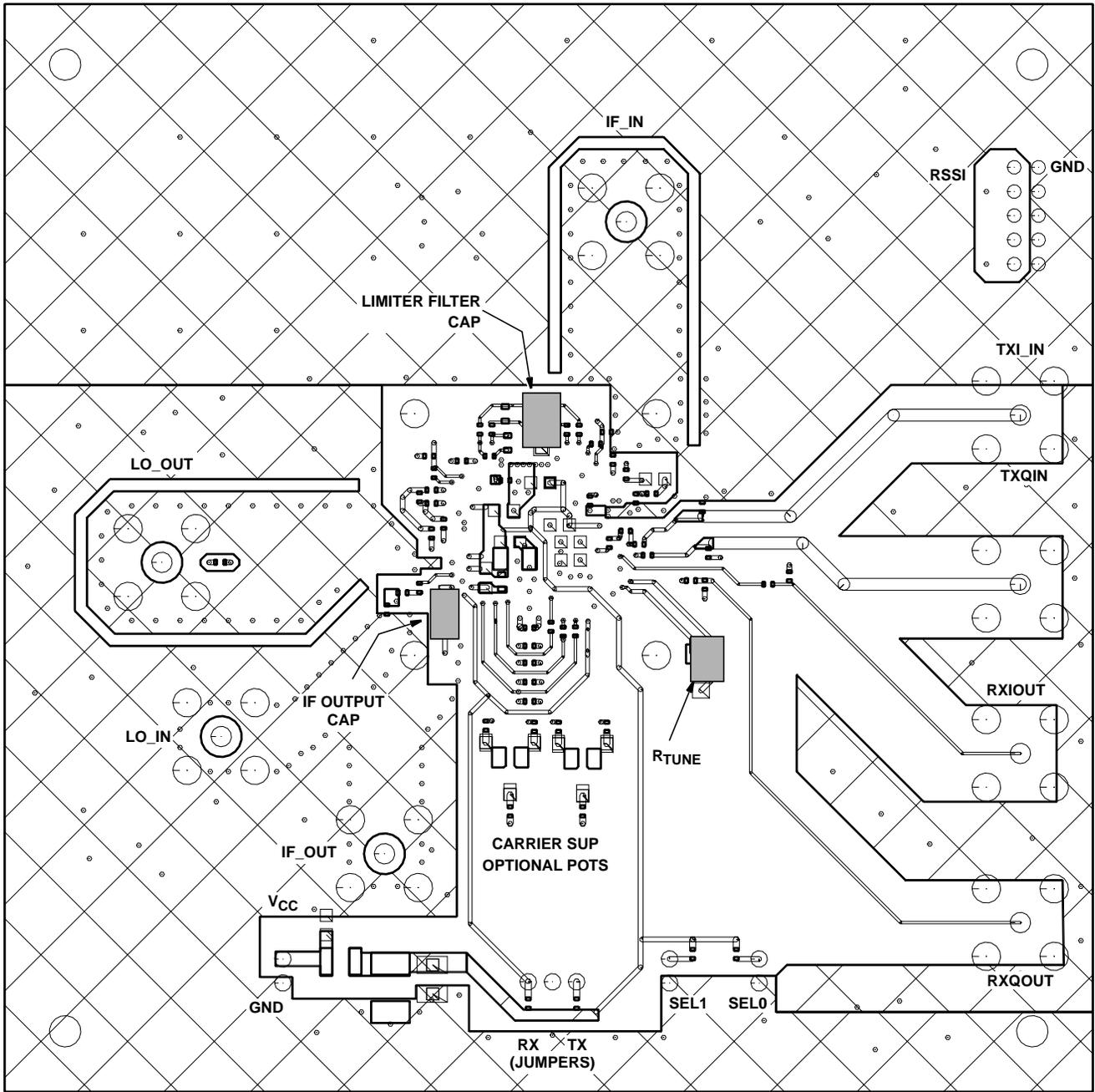


FIGURE 19. HFA3724 EVALUATION BOARD COMPONENT SIDE. USER ACCESS TO ALL PORTS AND ADJUSTMENTS

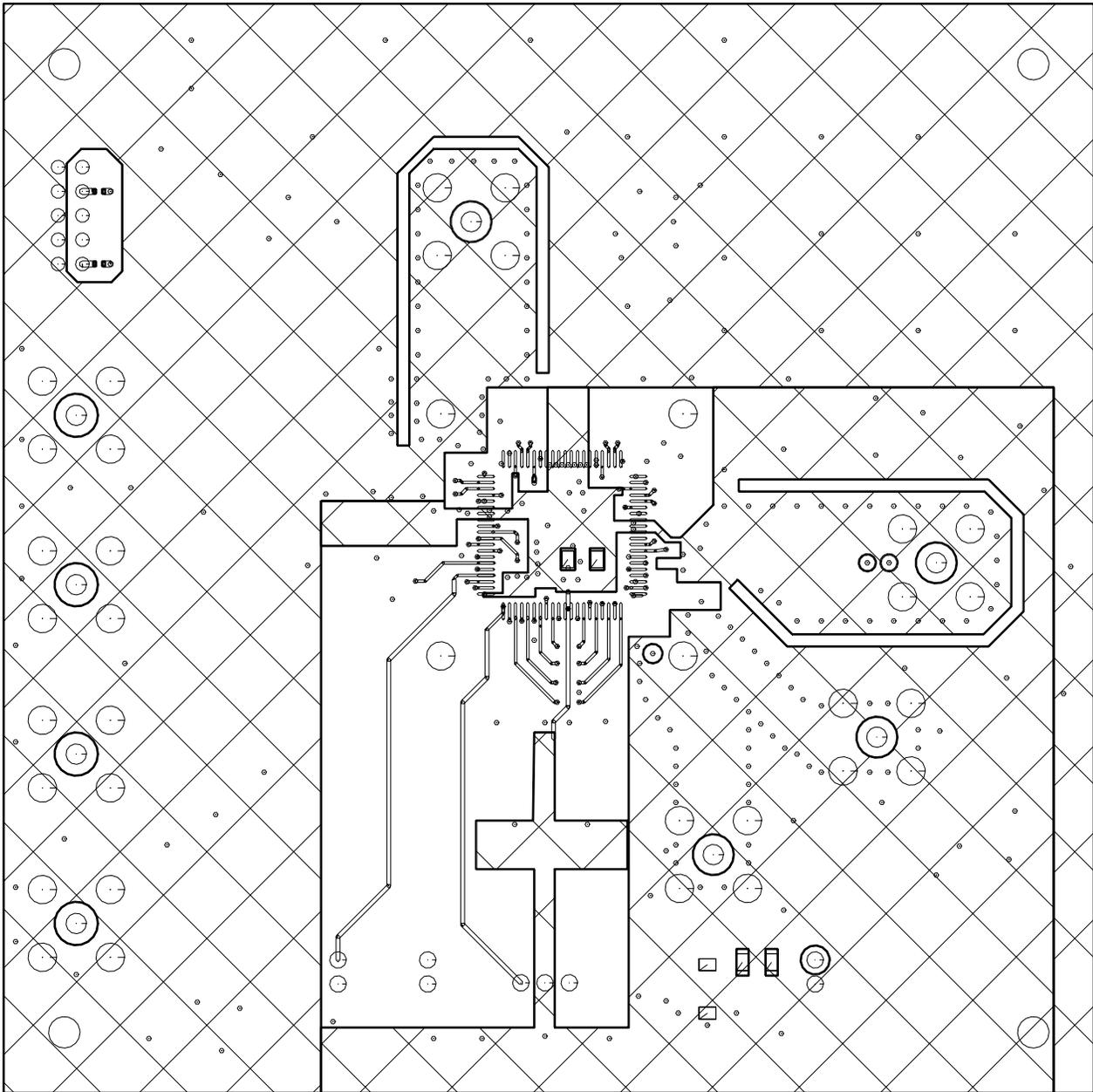


FIGURE 20. HFA3724 IC SIDE

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HFA3724 VER. 5 EVALUATION BOARD PARTS LIST - 6/1/96

PART NUMBER	DESCRIPTION	MFG/VENDOR	TOTAL
PCC470CQCT-ND (0402)	CAP, FXD, 47pF NPO	PANASONIC/DIGIKEY	3
PCC101CQCT-ND (0402)	CAP, FXD, 100pF NPO	PANASONIC/DIGIKEY	15
PCC103BQCT-ND (0402)	CAP, FXD, 0.01μF X7R	PANASONIC/DIGIKEY	10
MC-104M50-7U08-NI (0805)	CAP, FXD, 0.1μF	NIC COMPS/PRIDMORE	9
ECS-T1CY475R	CAP TANT, 4.7μF	PANASONIC/DIGIKEY	2
TZC03 R100A110	CAR VAR, 3-10pF	MURATA/NEWARK	1
GKG40067-07	CAP, VAR, 8-40pF	SPRAGUE-GOODMAN/DIGIKEY	1
ERJ-2GEJ0.0 (0402)	5% RES, FXD, 0Ω	PANASONIC/DIGIKEY	2
ERJ-2GEJ56 (0402)	5% RES, FXD, 56Ω	PANASONIC/DIGIKEY	4
ERJ-2GEJ220 (0402)	5% RES, FXD, 220Ω	PANASONIC/DIGIKEY	1
ERJ-2GEJ510 (0402)	5% RES, FXD, 510Ω	PANASONIC/DIGIKEY	1
ERJ-2GEJ560 (0402)	5% RES, FXD, 560Ω	PANASONIC/DIGIKEY	3
ERJ-2GEJ680 (0402)	5% RES, FXD, 680Ω	PANASONIC/DIGIKEY	2
ERJ-2GEJ1K (0402)	5% RES, FXD, 1K	PANASONIC/DIGIKEY	1
ERJ-2GEJ2K (0402)	5% RES, FXD, 2K	PANASONIC/DIGIKEY	2
ERJ-2GEJ4.3K (0402)	5% RES, FXD, 4.3K	PANASONIC/DIGIKEY	2
ERJ-2GEJ4.7K (0402)	5% RES, FXD, 4.7K	PANASONIC/DIGIKEY	4
RK73H1J-316 (0603)	1% RES, FXD, 316Ω	KOA/GARRET	1
EVM-1SSX50B501	POT- 500Ω	PANASONIC/DIGIKEY	1
LL1608-F10NK (0603)	IND, FXD, 10nH	TOKO/DIGIKEY	1
LL2012-F47NK (0805)	IND, FXD, 47nH	TOKO/DIGIKEY	1
EXC-CL3225U	SURFACE MT FERRITE BEAD	PANASONIC/DIGIKEY	1
DL4001	DIODE, RECT	DIODES INC/DIGIKEY	1
142-0701-211	WIDE-BODY CON-RCPT SMA	EF JOHNSON/NEWARK	4
142-0701-321	WIDE-BODY CON-RCPT, SMA (RIGHT ANGLE)	EF JOHNSON/NEWARK	4
MHB10G-ND	10 POS ST SHROUDED HEADER	3M/NEWARK	1
TSW-120-08GS	DEL POST TERMINAL PINS	SAMTEC/DEANCO	3
TSW-1 20-08GS	TERMINAL PINS	SAMTEC/DEANCO	1
SNT100BKT	SHORTING BAR FOR POSTS	SAMTEC/DEANCO	3
HFA3724	IC	INTERSIL	1
HFA3724 VER.4	PC BOARD	AVANTI	1
ERJ-2GEJ1K (0402)	5% RES, FXD, 1K	PANASONIC/DIGIKEY	4 (Note)
ERJ-2GEJ43K (0402)	5% RES, FXD, 43K	PANASONIC/DIGIKEY	2 (Note)
ST5W503CT-ND	POT 50K	MEPCOPAL/PHILIPS/DIGIKEY	2 (Note)

NOTE: Indicates optional component may be used.

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