CDB4382

# Evaluation Board for CS4382

## Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives AES/EBU, S/PDIF, & EIAJ-340 compatible digital audio
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

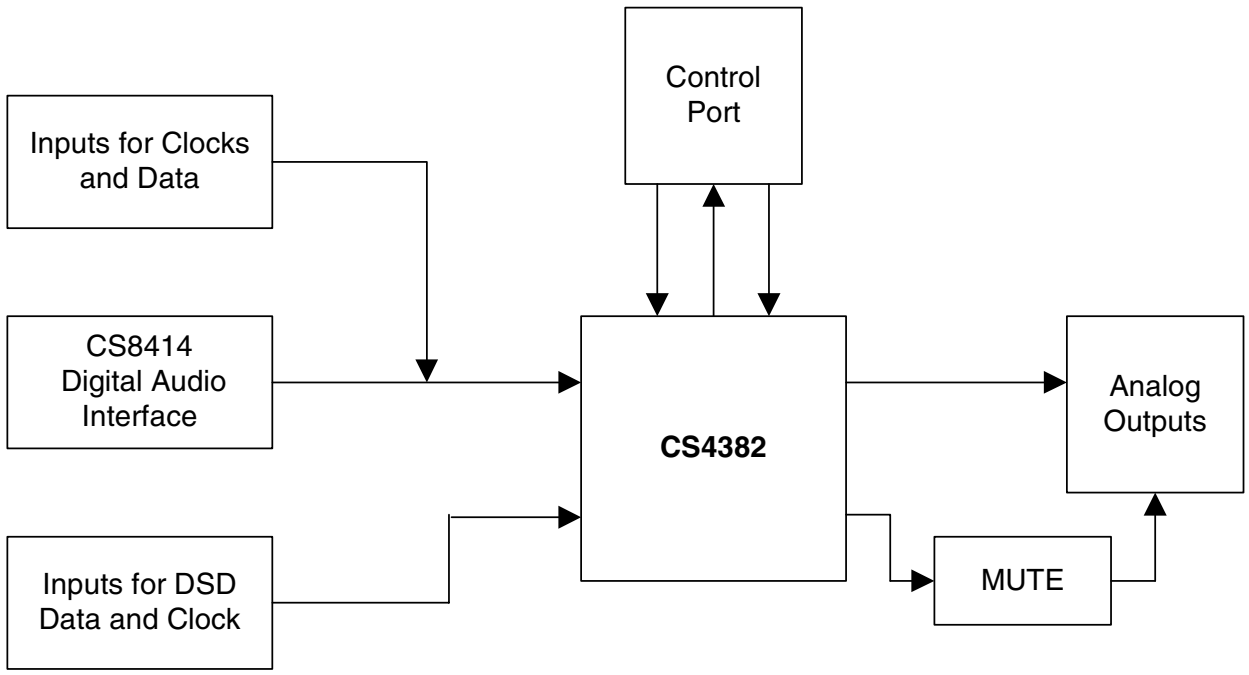
## Description

The CDB4382 evaluation board is an excellent means for quickly evaluating the CS4382 24-bit, eight channel D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4382 (for control port mode only) and a power supply. Analog line level outputs are provided via RCA phono jacks.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

**ORDERING INFORMATION**

CDB4382 Evaluation Board




*Preliminary Product Information* | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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## CDB4382 SYSTEM OVERVIEW

The CDB4382 evaluation board is an excellent means of quickly evaluating the CS4382. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply either PCM or DSD clocks and data through 18-pin headers for system development.

The CDB4382 schematic has been partitioned into 10 schematics shown in Figures 2 through 11. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

### 1. CS4382 DIGITAL TO ANALOG CONVERTER

A description of the CS4382 is included in the CS4382 datasheet.

### 2. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 3. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), and a 256 Fs master clock. The CS8414 data format has been configured for I2S. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 3. However, both inputs cannot be driven simultaneously.

### 3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 18-pin headers, J15 and J16. Header J15 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 4.

Header J16 allows the evaluation board to accept externally generated DSD data and clock. The schematic for the clock/data input is shown in Figure 5. A synchronous MCLK must still be provided via header J15. Please see the CS4382 datasheet for more information.

### 4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts (GND, +5V, VLS, VLC, +12V and -12V), see Figure 11. The +5V input supplies power to the +5 volt digital circuitry (+5V, VD_+5, VA_+5), while the VLS and VLC inputs supply power to the Voltage Level Converters and the CS4382 VLS and VLC pins respectively. +12V and -12V supply power to the op-amps and can be +/-5 to +/-12 volts.

**WARNING:** Refer to the CS4382 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

### 5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4382 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the power distribution used on this board. The decoupling capacitors are located as close to the CS4382 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

### 6. CONTROL PORT SOFTWARE

The CDB4382 is shipped with Windows based software for interfacing with the CS4382 control port via the DB25 connector, J1. The software can be used to communicate with the CS4382 in either SPI® or Two Wire mode; however, in SPI mode the CS4382 registers are write-only.

Note: The Two Wire control port mode is compatible with the $I^2C^®$ protocol.

## 7. DSD OPERATION

The CDB4382 supports Direct Stream Digital (DSD) operation through the header for external clocks and data, J16. The CS4382 must be placed into the DSD mode and headers J6 and J14 must be set accordingly. See Table 2 for more information.

## 8. ANALOG OUTPUT FILTER

The application note "Design Notes for a 2-Pole Filter with Differential Input" discusses the second-order Butterworth filter and differential to single-ended converter which was implemented on the CS4382 evaluation board, CDB4382. The filter, as seen in Figures 7 through 10, is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

| CONNECTOR | INPUT/OUTPUT | SIGNAL PRESENT |
|---|---|---|
| +5V | Input | + 5 Volt power |
| VLS | Input | + 1.8 to +5V power for the CS4382 serial interface |
| VLC | Input | + 1.8 to +5V power for the CS4382 control interface |
| -12V | Input | -12 to -5V negative supply for the op-amps |
| +12V | Input | +5 to +12V positive supply for the op-amps |
| GND | Input | Ground connection from power supply |
| Coax Input | Input | Digital audio interface input via coax |
| Optical Input | Input | Digital audio interface input via optical |
| J15 | Input | Input for master, serial, left/right clocks and serial data |
| J16 | Input | Input for DSD data and clock |
| Parallel Port | Input/Output | Parallel connection to PC for SPI / Two Wire control port signals |
| J17 | Input/Output | I/O for SPI / Two Wire control port signals |
| OUT1A | Output | Channel 1A line level analog output |
| OUT1B | Output | Channel 1B line level analog output |
| OUT2A | Output | Channel 2A line level analog output |
| OUT2B | Output | Channel 2B line level analog output |
| OUT3A | Output | Channel 3A line level analog output |
| OUT3B | Output | Channel 3B line level analog output |
| OUT4A | Output | Channel 4A line level analog output |
| OUT4B | Output | Channel 4B line level analog output |

**Table 1. System Connections**

| JUMPER / SWITCH | PURPOSE | POSITION | FUNCTION SELECTED |
|---|---|---|---|
| J4 | Stand-Alone/Control Port Select | SA<br>*CP | Stand-Alone Mode (No PC required)<br>Control Port Mode (PC required) |
| J6 | Clock Source Select | *CS8414<br>External | CS8414 provides PCM inputs to CS4382<br>PCM or DSD inputs are provided externally |
| J9 | M0/AD0/CS | *HI<br>LO | See CS4382 datasheet for details |
| J10 | M1/SDA/CDIN | *HI<br>LO | See CS4382 datasheet for details |
| J11 | M2/SCL/CCLK | *HI<br>LO | See CS4382 datasheet for details |
| J12 | M3/DSD_CLK | HI<br>*LO | See CS4382 datasheet for details |
| J14 | Input Mode Select | *PCM<br>DSD | Selects PCM input mode<br>Selects DSD input mode (via J16) |
| J21-J28 | Mute Enables | | Enables the external mute circuit for each channel when jumpered |

**Table 2. CDB4382 Jumper Settings**

*Default Factory Settings

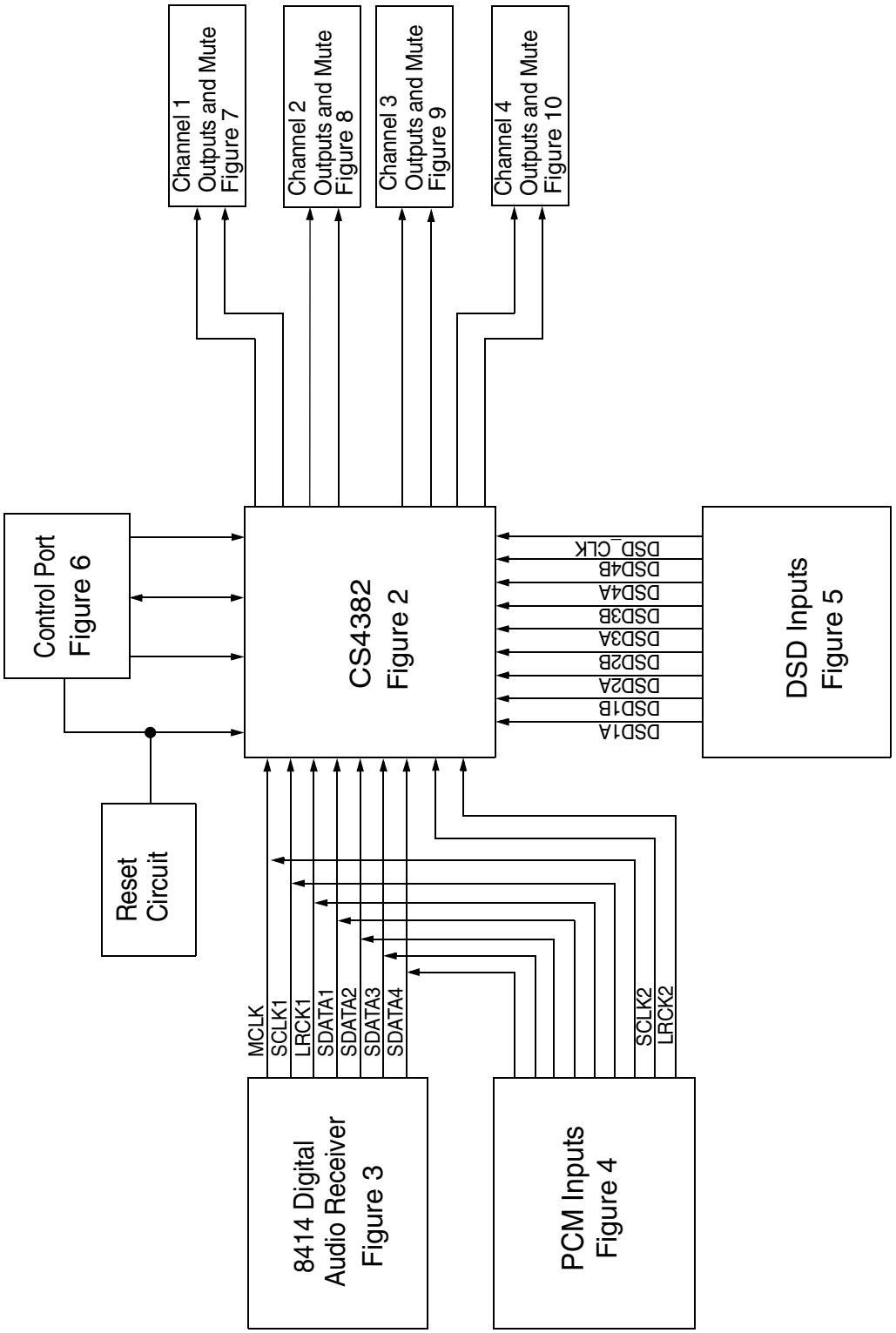



**Figure 1. System Block Diagram and Signal Flow**

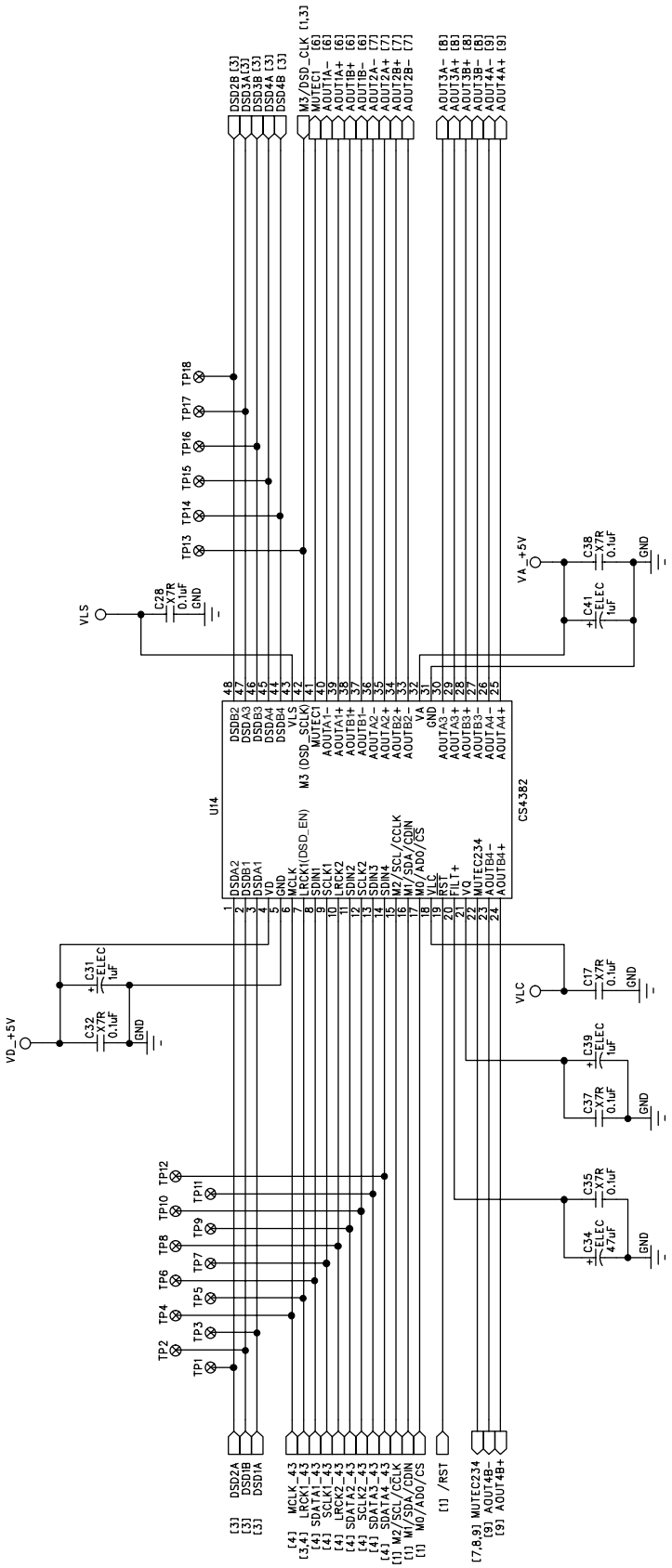



**Figure 2. CS4382**

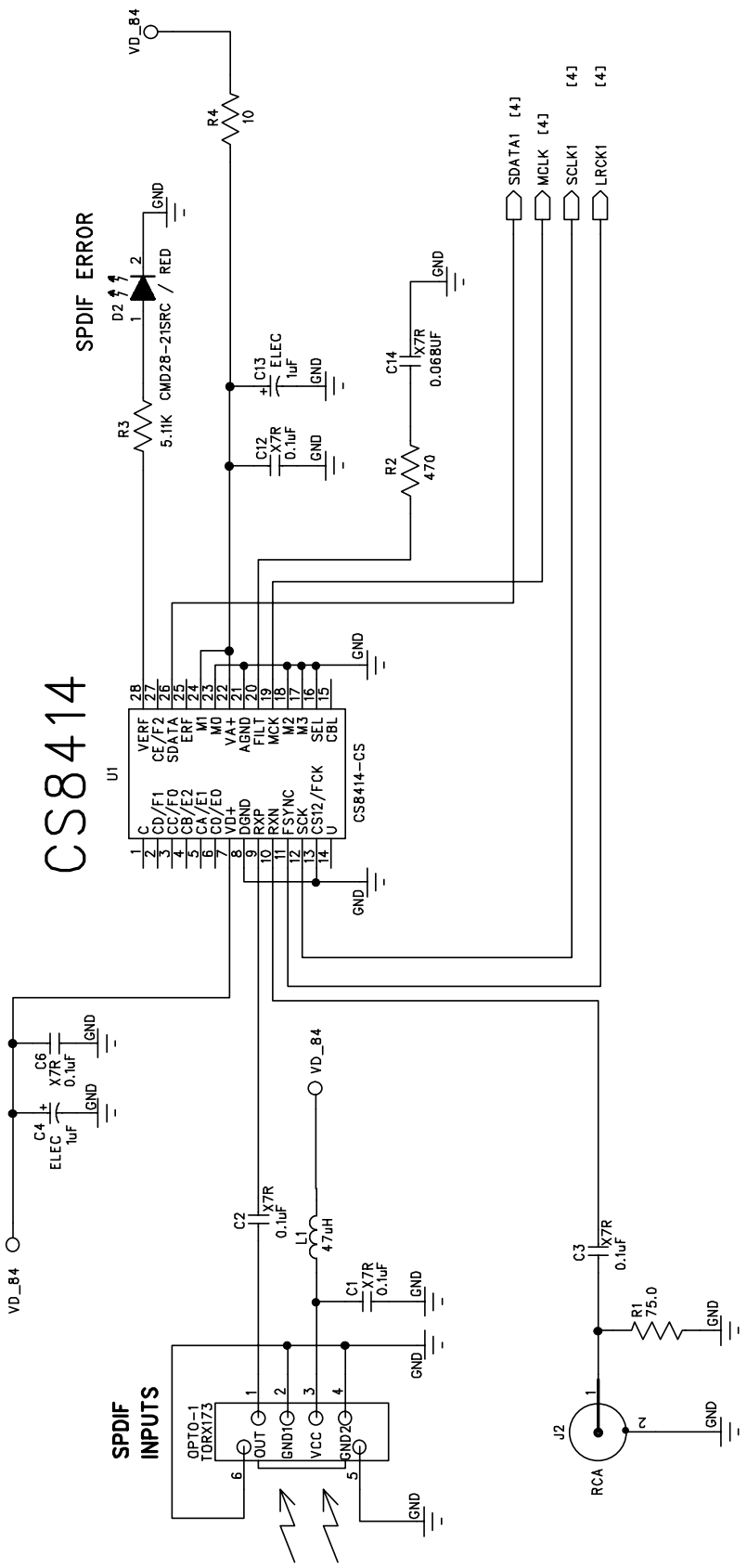



**Figure 3. CS8414 Digital Audio Receiver**

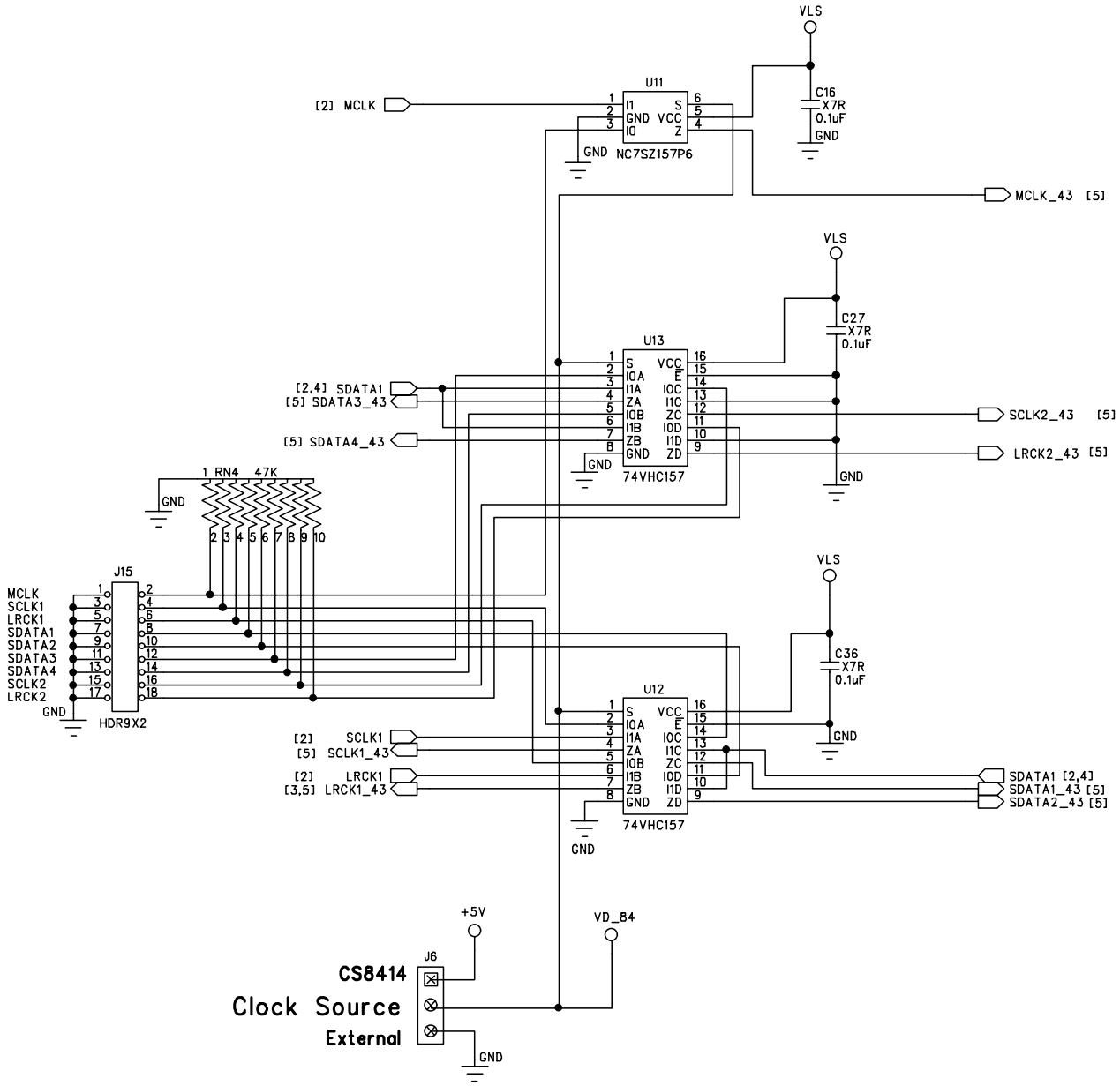



**Figure 4. PCM Input Header**

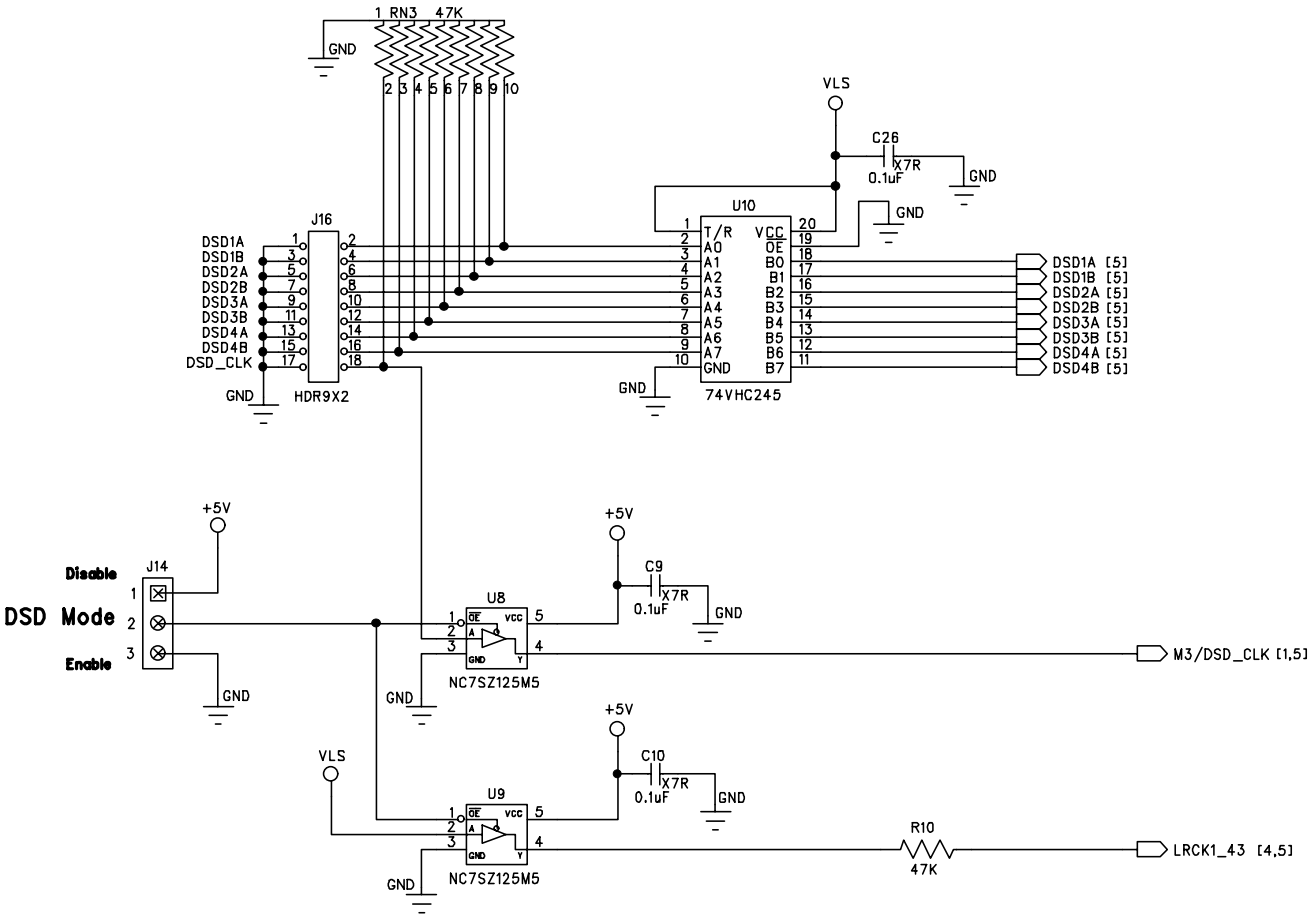



**Figure 5. DSD Input Header**

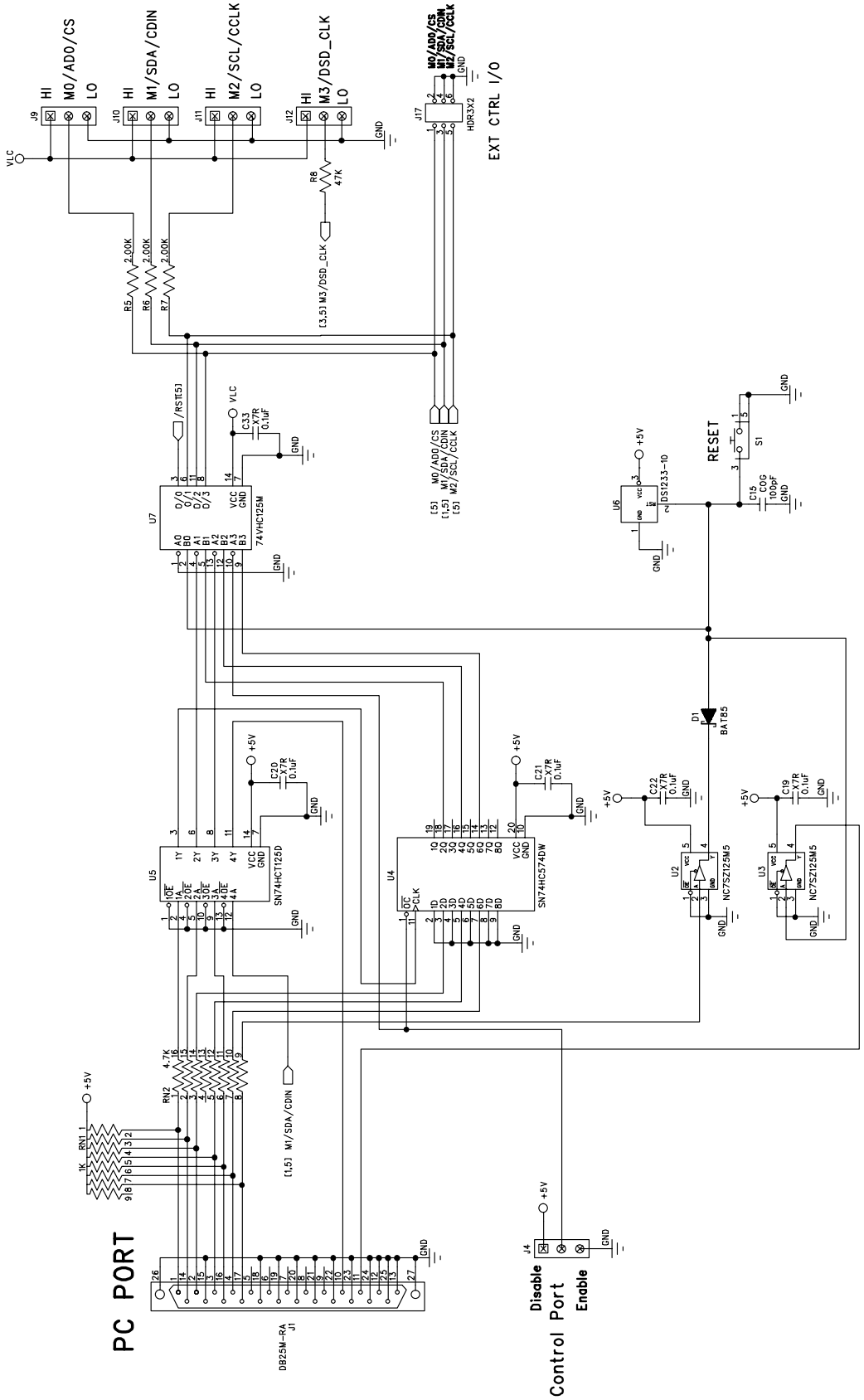



**Figure 6. Control Port**

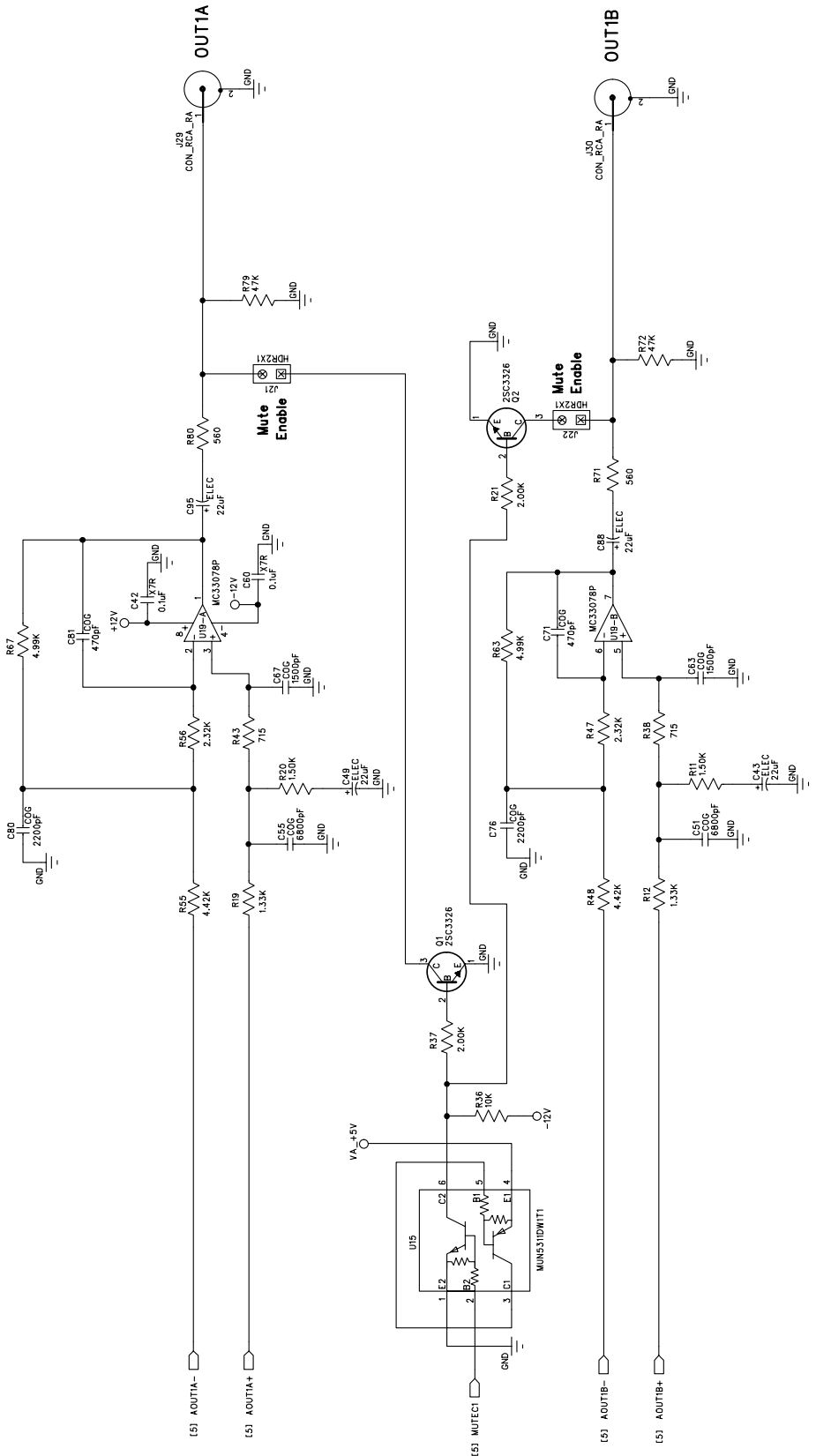



**Figure 7. Channel 1 Outputs and Mute**

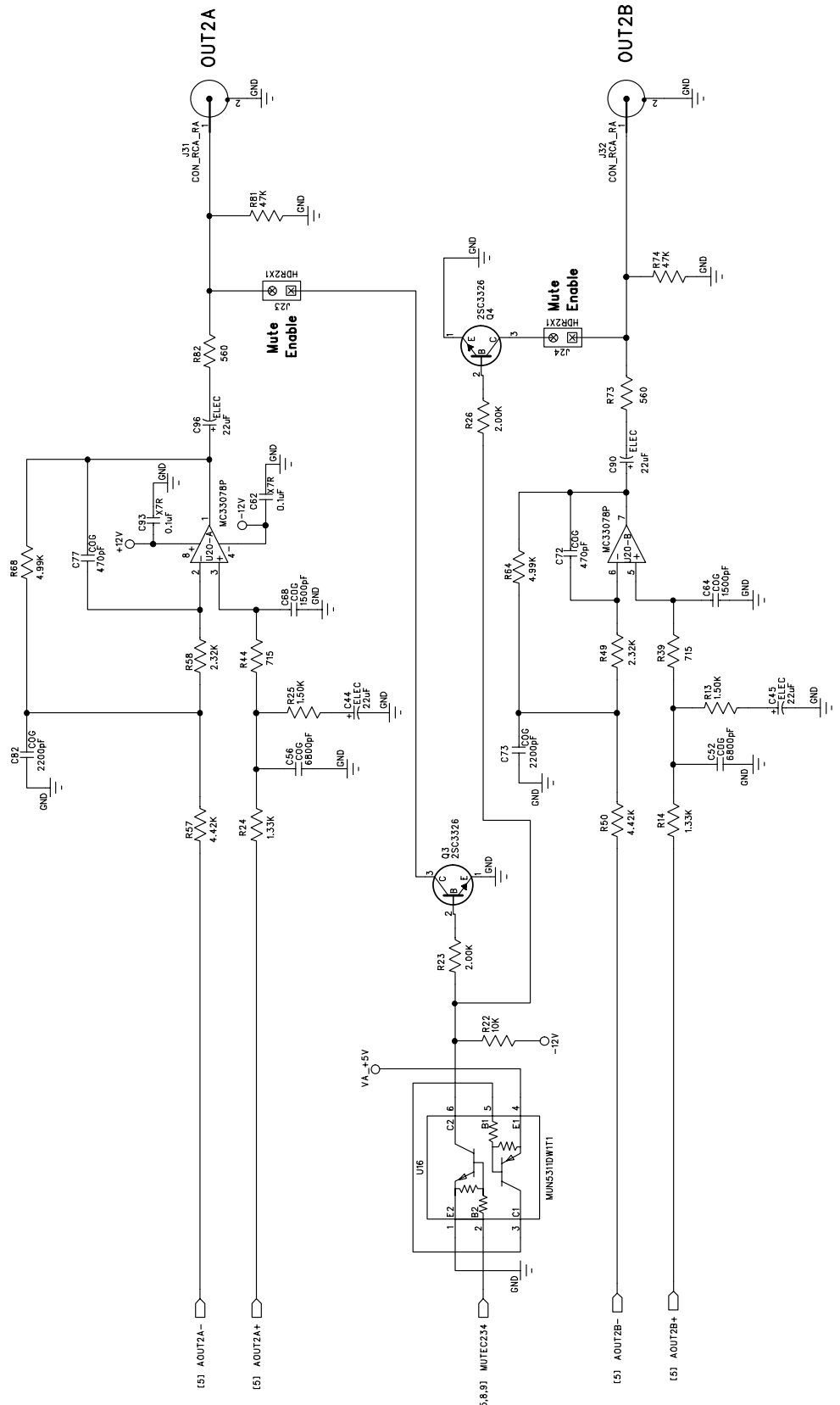



**Figure 8. Channel 2 Outputs and Mute**

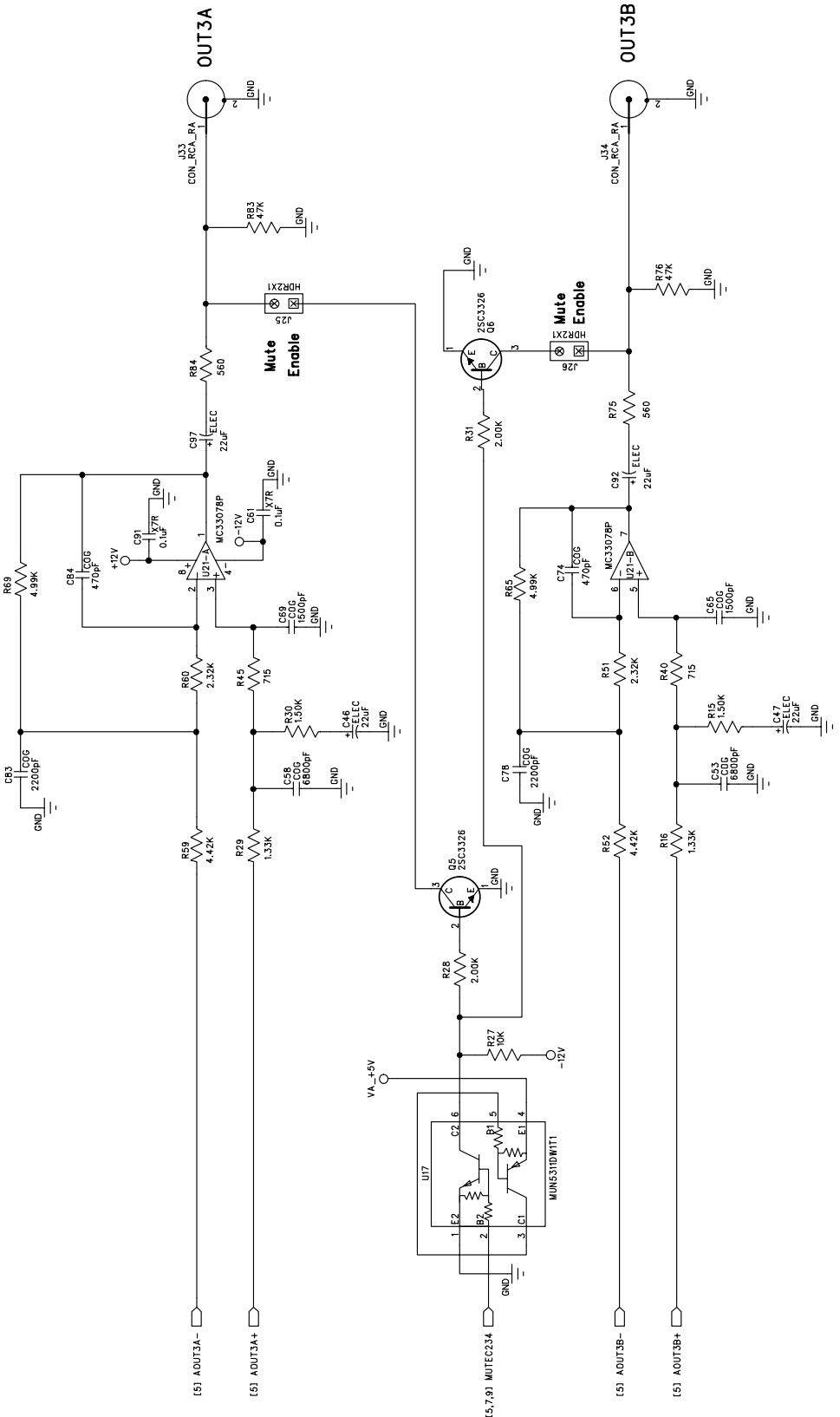



**Figure 9. Channel 3 Outputs and Mute**

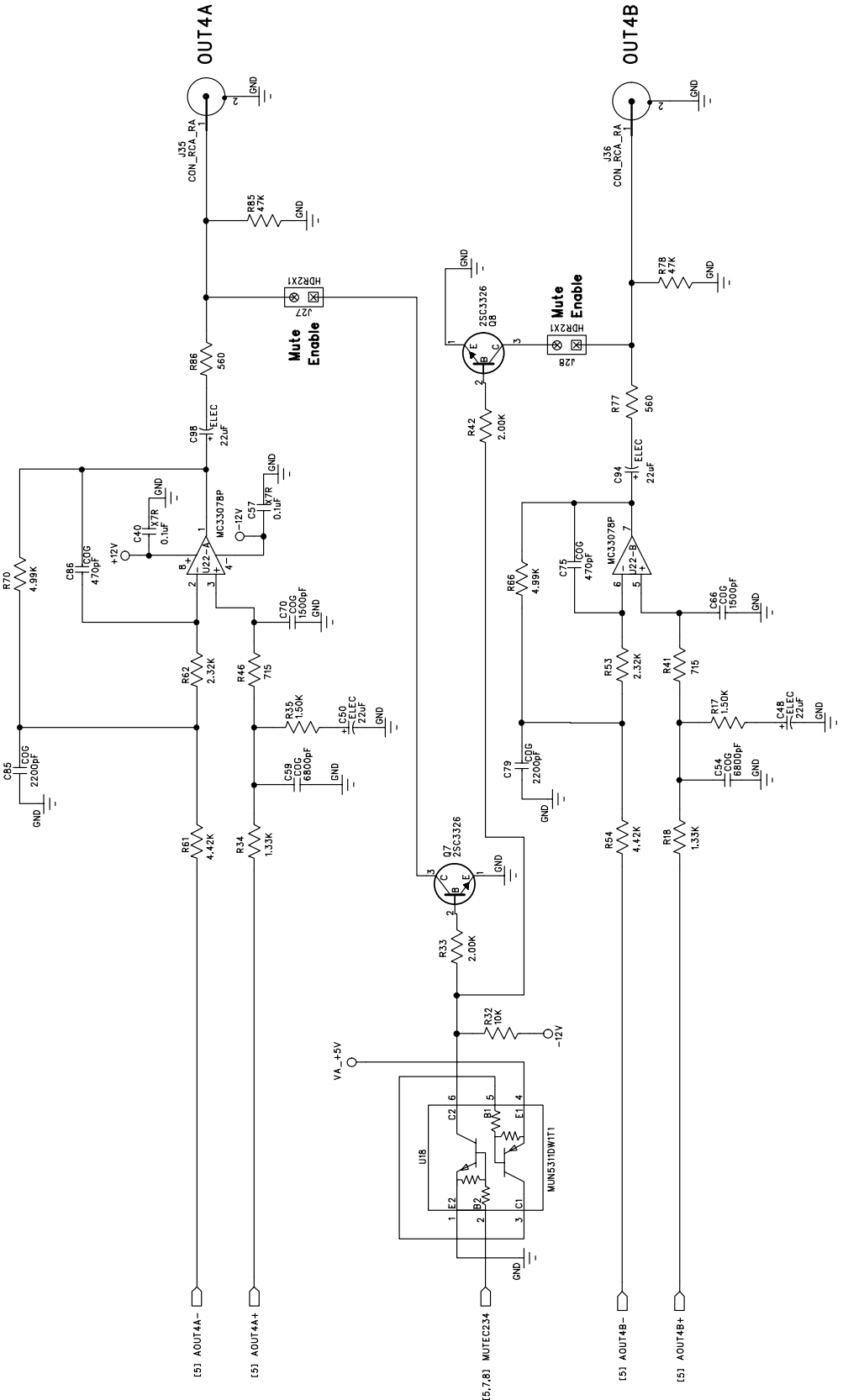



**Figure 10. Channel 4 Outputs and Mute**

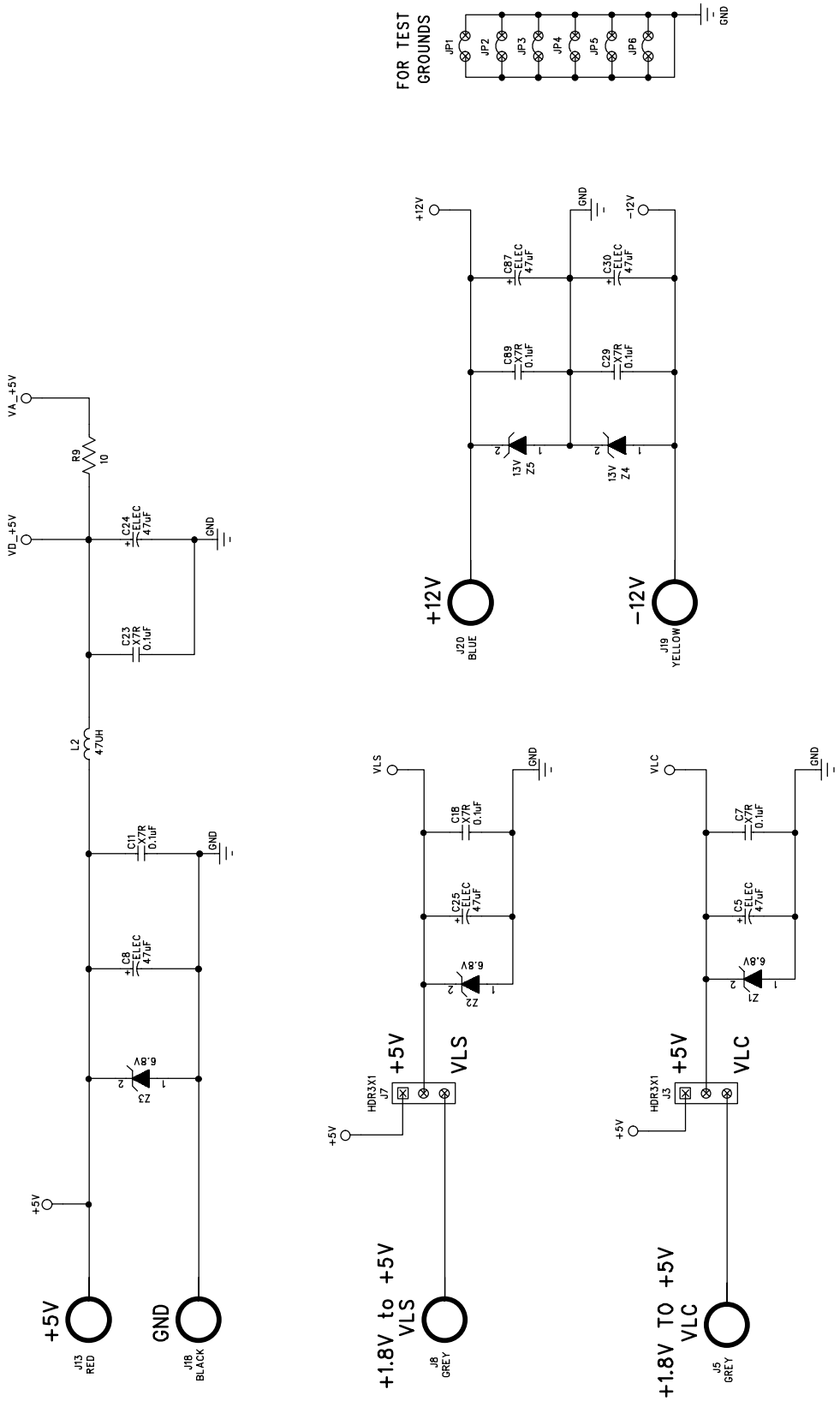
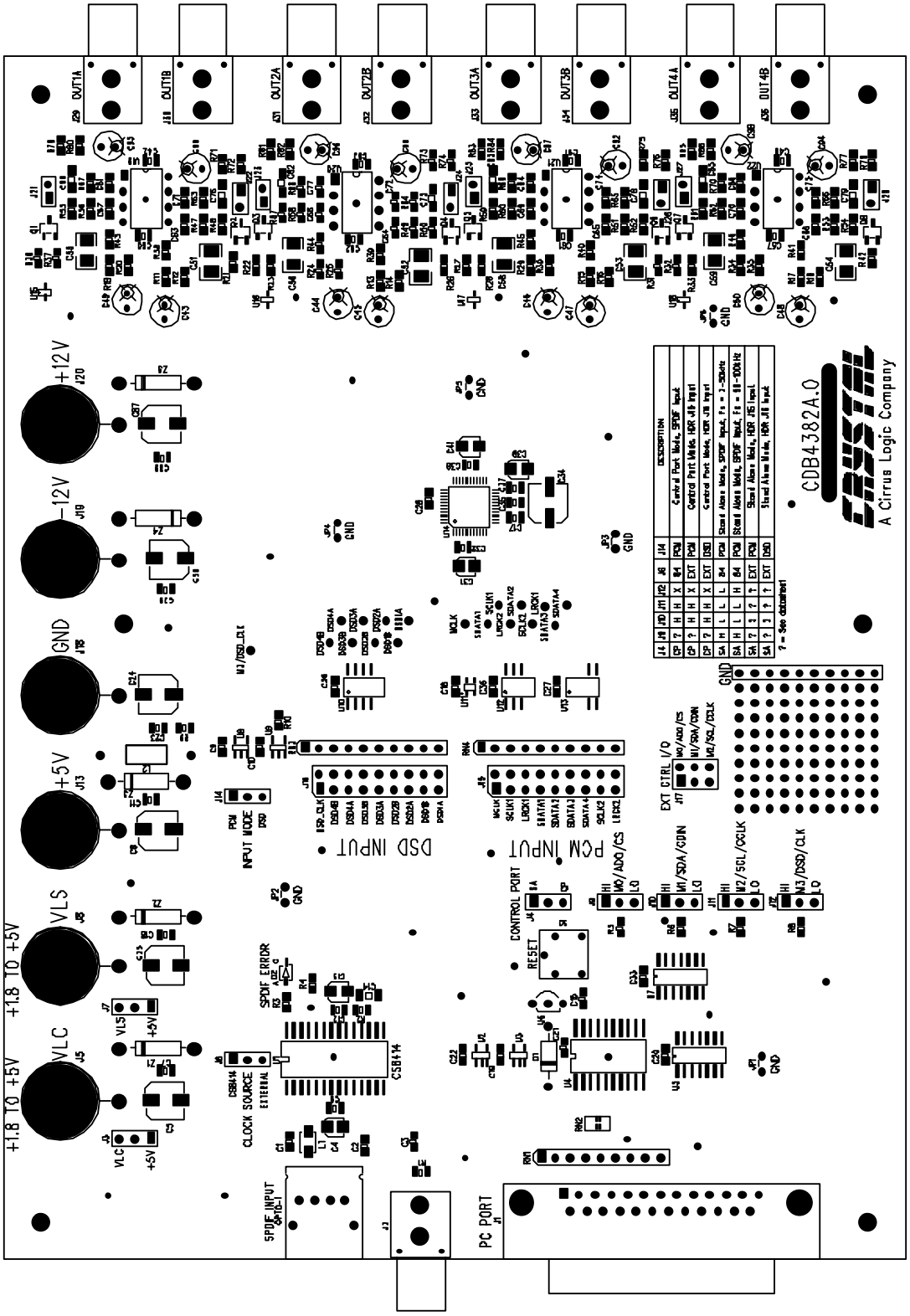
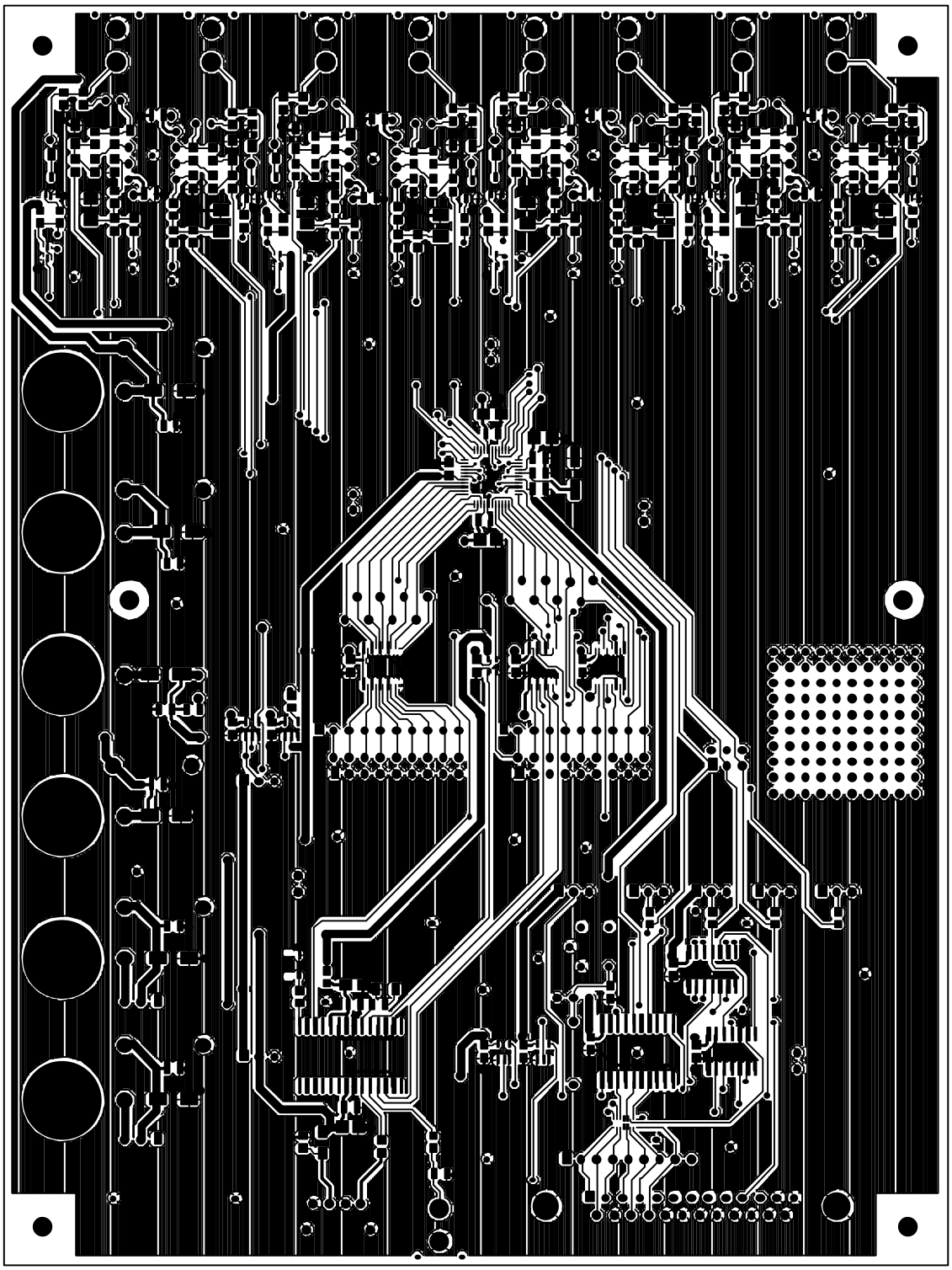



**Figure 11. Power Supply**



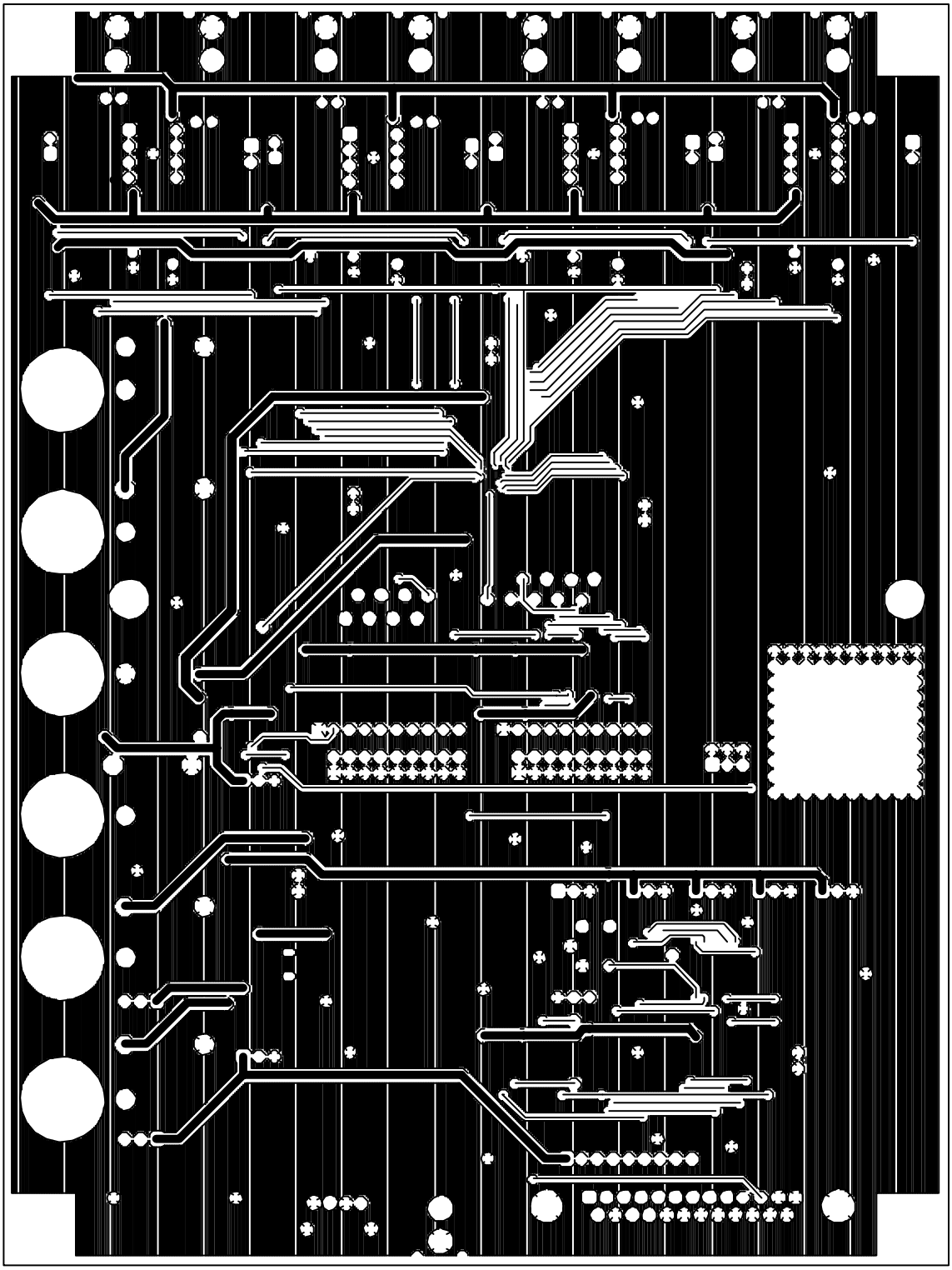

TOP SIDE, CDB4382SILKSCREEN TOP, CDB4382A

**Figure 12. Silkscreen Top**



TOP SIDE, CDB4382A

**Figure 13. Top Side**



BOTTOM SIDE, CDB4382A

**Figure 14. Bottom Side**

# • Notes •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