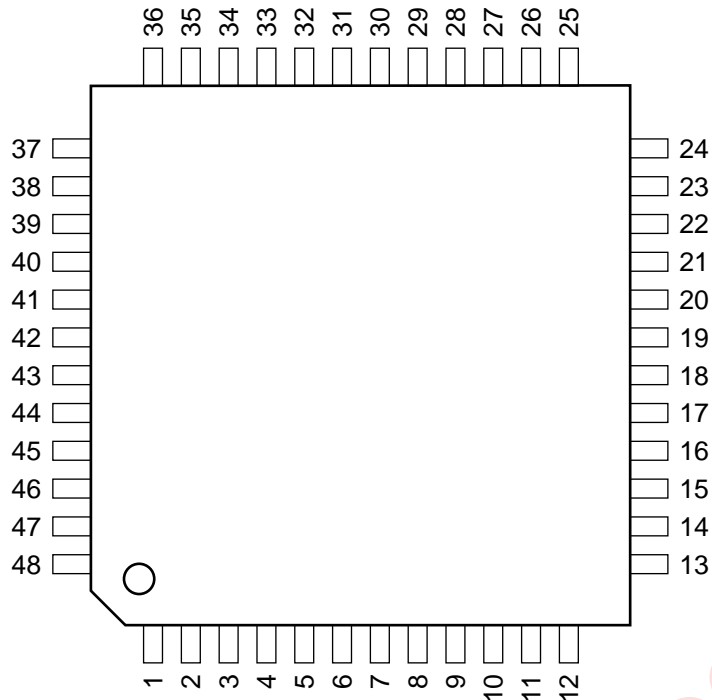


TIMING GENERATOR

—TOP VIEW—



| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---------|-----|--------|---------|-----|------------------|---------|-----|-------------------|---------|-----|--------|
| 1 | O | CAMENO | 13 | I/O | OSCO | 25 | O | $\overline{V2}$ | 37 | O | PBLK |
| 2 | O | BUSY | 14 | I | SMD2 | 26 | O | $\overline{V1}$ | 38 | O | ID |
| 3 | O | CL | 15 | I | STRB | 27 | O | \overline{SG} | 39 | O | WEN |
| 4 | O | CLD | 16 | I | DCLK | 28 | I | TSTMD | 40 | O | VD60 |
| 5 | O | CKO | 17 | I | DATA | 29 | I | WM | 41 | I | GRST |
| 6 | — | GND | 18 | — | GND | 30 | — | Vcc | 42 | — | GND |
| 7 | — | Vcc | 19 | — | Vcc | 31 | — | GND | 43 | — | Vcc |
| 8 | I | TRGM | 20 | O | RG | 32 | O | \overline{SHP} | 44 | I | STDBY |
| 9 | I | TRIG | 21 | O | \overline{SUB} | 33 | O | \overline{SHD} | 45 | I | I ACT |
| 10 | I | PS | 22 | O | H1 | 34 | O | \overline{RS} | 46 | I | MCENI |
| 11 | I | SMD1 | 23 | O | H2 | 35 | O | \overline{CPDM} | 47 | I | VD |
| 12 | I | OSCI | 24 | O | $\overline{V3}$ | 36 | O | \overline{CPOB} | 48 | I | HD |

INPUTS

| | |
|------------|------------------------------------|
| DATA | : SERIAL INTERFACE DATA |
| DCLK | : SERIAL INTERFACE CLOCK |
| GRST | : RESET |
| HD | : HORIZONTAL DRIVE PULS |
| I ACT | : MC ISO ACT |
| MCENI | : CPU ENABLE |
| OSCI | : OSCILLATOR |
| PS | : SHUTTER SPEED PARALLEL OR SERIAL |
| SMD1, SMD2 | : SHUTTER MODE |
| STDBY | : STANDBY |
| STRB | : SERIAL INTERFACE STROBE |
| TRGM | : TRIGGER MODE |
| TRIG | : EXT TRIGGER PULSE |
| TSTMD | : TEST MODE |
| VD | : VERTICAL DRIVE PULSE |
| WM | : WRITE ENABLE MODE |

OUTPUTS

| | |
|---|--------------------------------------|
| BUSY | : BUSY |
| CAMENO | : CAMERA ENABLE |
| CKO | : CLOCK (24.5 MHz) |
| CL | : CLOCK (12.3 MHz) |
| CLD | : CLOCK FOR A/D CONVERTER |
| $\overline{\text{CPDM}}$ | : CCD DUMMY SIGNAL CLAMP PULSE |
| $\overline{\text{CPOB}}$ | : CCD OPTICAL BLACK CLAMP PULSE |
| H1, H2 | : HORIZONTAL REGISTER CLOCK |
| ID | : VERTICAL LINE DISCRIMINATION |
| PBLK | : PRE-BLANKING PULSE |
| $\overline{\text{RG}}$ | : RESET GATE PULSE |
| $\overline{\text{RS}}$ | : PHASE ADJUST SAMPLE HOLD PULSE |
| $\overline{\text{SG}}$ | : SENSOR READ CLOCK |
| $\overline{\text{SHD}}$ | : DATA LEVEL SAMPLE HOLD PULSE |
| $\overline{\text{SHP}}$ | : PRE-CHARGE LEVEL SAMPLE HOLD PULSE |
| $\overline{\text{SUB}}$ | : SHUTTER PULSE |
| $\overline{\text{V1}} - \overline{\text{V3}}$ | : VERTICAL REGISTER CLOCK |
| VD60 | : VERTICAL DRIVE PULSE 60 Hz |
| WEN | : WRITE ENABLE PULSE |

INPUT/OUTPUT

| | |
|------|--------------|
| OSCO | : OSCILLATOR |
|------|--------------|

