



CYPRESS

CY29351

2.5V or 3.3V, 200-MHz, 9-Output Zero Delay Buffer

Features

- Output frequency range: 25 MHz to 200 MHz
- Input frequency range: 25 MHz to 200 MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- ±2.5% max Output duty cycle variation
- 9 Clock outputs: Drive up to 18 clock lines
- Two reference clock inputs: LVPECL or LVCMOS
- 150-ps max output-output skew
- Phase-locked loop (PLL) bypass mode
- Spread Aware™
- Output enable/disable
- Pin-compatible with MPC9351
- Industrial temperature range: -40°C to +85°C
- 32-Pin 1.0-mm TQFP package

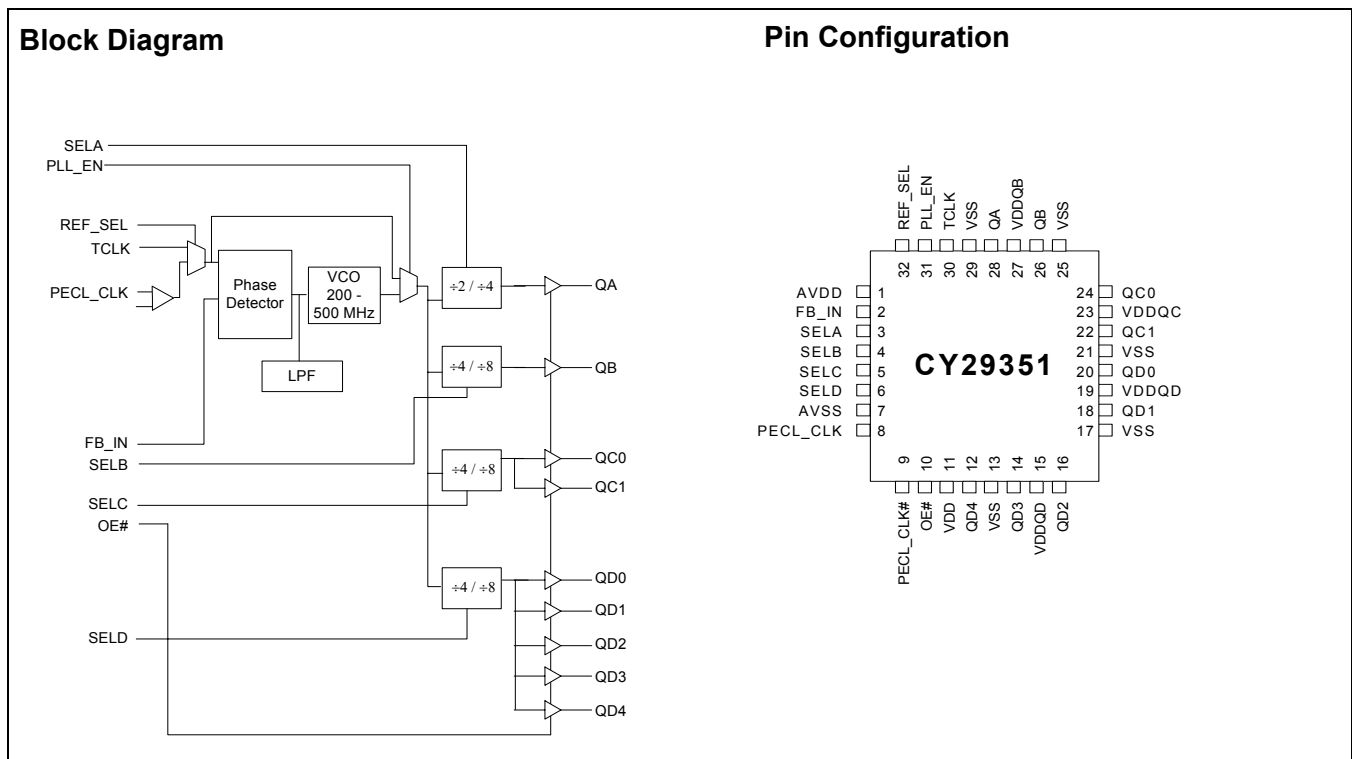
Functional Description

The CY29351 is a low voltage high performance 200 MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

The CY29351 features LVPECL and LVCMOS reference clock inputs and provides 9 outputs partitioned in 4 banks of 1, 1, 2, and 5 outputs. Bank A divides the VCO output by 2 or 4 while the other banks divide by 4 or 8 per SEL(A:D) settings, see *Functional Table*. These dividers allow output to input ratios of 4:1, 2:1, 1:1, 1:2, and 1:4. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18.

The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 25 MHz to 200 MHz. For normal operation, the external feedback input, FB\_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see the *Table 1*.

When PLL\_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.



**Pin Definitions<sup>[1]</sup>**

Pin	Name	I/O	Type	Description
8	PECL_CLK	I, PU	LVPECL	<b>LVPECL reference clock input</b>
9	PECL_CLK#	I, PU/PD	LVPECL	<b>LVPECL reference clock input.</b> Weak pull-up to VDD/2.
30	TCLK	I, PD	LVCMOS	<b>LVCMOS/LVTTL reference clock input</b>
28	QA	O	LVCMOS	<b>Clock output bank A</b>
26	QB	O	LVCMOS	<b>Clock output bank B</b>
22, 24	QC(1,0)	O	LVCMOS	<b>Clock output bank C</b>
12, 14, 16, 18, 20	QD(4:0)	O	LVCMOS	<b>Clock output bank D</b>
2	FB_IN	I, PD	LVCMOS	<b>Feedback clock input.</b> Connect to an output for normal operation. This input should be at the same voltage rail as input reference clock. See <i>Table 1</i> .
10	OE#	I, PD	LVCMOS	<b>Output enable/disable input.</b> See <i>Table 2</i> .
31	PLL_EN	I, PU	LVCMOS	<b>PLL enable/disable input.</b> See <i>Table 2</i> .
32	REF_SEL	I, PD	LVCMOS	<b>Reference select input.</b> See <i>Table 2</i> .
3, 4, 5, 6	SEL(A:D)	I, PD	LVCMOS	<b>Frequency select input, Bank (A:D).</b> See <i>Table 2</i> .
27	VDDQB	Supply	VDD	<b>2.5V or 3.3V Power supply for bank B output clock<sup>[2,3]</sup></b>
23	VDDQC	Supply	VDD	<b>2.5V or 3.3V Power supply for bank C output clocks<sup>[2,3]</sup></b>
15, 19	VDDQD	Supply	VDD	<b>2.5V or 3.3V Power supply for bank D output clocks<sup>[2,3]</sup></b>
1	AVDD	Supply	VDD	<b>2.5V or 3.3V Power supply for PLL<sup>[2,3]</sup></b>
11	VDD	Supply	VDD	<b>2.5V or 3.3V Power supply for core, inputs, and bank A output clock<sup>[2,3]</sup></b>
7	AVSS	Supply	Ground	<b>Analog ground</b>
13, 17, 21, 25, 29	VSS	Supply	Ground	<b>Common ground</b>

**Table 1. Frequency Table**

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷2	Input Clock * 2	100 MHz to 200 MHz	100 MHz to 190MHz
÷4	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 95MHz
÷8	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 47.5MHz

**Table 2. Function Table**

Control	Default	0	1
REF_SEL	0	PCLK	TCLK
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
OE#	0	Outputs enabled	Outputs disabled (three-state), VCO running at its minimum frequency
SELA	0	÷ 2 (Bank A)	÷ 4 (Bank A)
SELB	0	÷ 4 (Bank B)	÷ 8 (Bank B)
SELC	0	÷ 4 (Bank C)	÷ 8 (Bank C)
SELD	0	÷ 4 (Bank D)	÷ 8 (Bank D)

**Notes:**

1. PU = Internal pull-up, PD = Internal pull-down.
2. A 0.1-μF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQB, VDDQC, and VDDQD power supply pins.

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		-0.3	5.5	V
V <sub>DD</sub>	DC Operating Voltage	Functional	2.375	3.465	V
V <sub>IN</sub>	DC Input Voltage	Relative to V <sub>SS</sub>	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>OUT</sub>	DC Output Voltage	Relative to V <sub>SS</sub>	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>TT</sub>	Output termination Voltage		-	V <sub>DD</sub> ÷ 2	V
LU	Latch-up Immunity	Functional	200	-	mA
R <sub>PS</sub>	Power Supply Ripple	Ripple Frequency < 100 kHz	-	150	mVp-p
T <sub>S</sub>	Temperature, Storage	Non Functional	-65	+150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	-40	+85	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	+150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	Functional		42	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	Functional		105	°C/W
ESD <sub>H</sub>	ESD Protection (Human Body Model)		2000	-	Volts
FIT	Failure in Time	Manufacturing test		10	ppm

**DC Electrical Specifications** (V<sub>DD</sub> = 2.5V ± 5%, T<sub>A</sub> = -40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input Voltage, Low	LVC MOS	-	-	0.7	V
V <sub>IH</sub>	Input Voltage, High	LVC MOS	1.7	-	V <sub>DD</sub> +0.3	V
V <sub>PP</sub>	Peak-Peak Input Voltage	LVPECL	250	-	1000	mV
V <sub>CMR</sub>	Common Mode Range <sup>[4]</sup>	LVPECL	1.0	-	V <sub>DD</sub> - 0.6	V
V <sub>OL</sub>	Output Voltage, Low <sup>[5]</sup>	I <sub>OL</sub> = 15mA	-	-	0.6	V
V <sub>OH</sub>	Output Voltage, High <sup>[5]</sup>	I <sub>OH</sub> = -15mA	1.8	-	-	V
I <sub>IL</sub>	Input Current, Low <sup>[6]</sup>	V <sub>IL</sub> = V <sub>SS</sub>	-	-	-100	μA
I <sub>IH</sub>	Input Current, High <sup>[6]</sup>	V <sub>IL</sub> = V <sub>DD</sub>	-	-	100	μA
I <sub>DDA</sub>	PLL Supply Current	AVDD only	-	5	10	mA
I <sub>DDQ</sub>	Quiescent Supply Current	All V <sub>DD</sub> pins except AVDD	-	-	7	mA
I <sub>DD</sub>	Dynamic Supply Current	Outputs loaded @ 100 MHz	-	180	-	mA
		Outputs loaded @ 200 MHz	-	210	-	
C <sub>IN</sub>	Input Pin Capacitance		-	4	-	pF
Z <sub>OUT</sub>	Output Impedance		14	18	22	Ω

**DC Electrical Specifications** (V<sub>DD</sub> = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input Voltage, Low	LVC MOS	-	-	0.8	V
V <sub>IH</sub>	Input Voltage, High	LVC MOS	2.0	-	V <sub>DD</sub> + 0.3	V
V <sub>PP</sub>	Peak-Peak Input Voltage	LVPECL	250	-	1000	mV
V <sub>CMR</sub>	Common Mode Range <sup>[4]</sup>	LVPECL	1.0	-	V <sub>DD</sub> - 0.6	V
V <sub>OL</sub>	Output Voltage, Low <sup>[5]</sup>	I <sub>OL</sub> = 24 mA	-	-	0.55	V
		I <sub>OL</sub> = 12 mA	-	-	0.30	
V <sub>OH</sub>	Output Voltage, High <sup>[5]</sup>	I <sub>OH</sub> = -24 mA	2.4	-	-	V

**Notes:**

- V<sub>CMR</sub> (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the V<sub>CMR</sub> range and the input swing is within the V<sub>PP</sub> (DC) specification.
- Driving one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
- Inputs have pull-up or pull-down resistors that affect the input current.

**DC Electrical Specifications** ( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ) (continued)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$I_{IL}$	Input Current, Low <sup>[6]</sup>	$V_{IL} = V_{SS}$	–	–	–100	$\mu A$
$I_{IH}$	Input Current, High <sup>[6]</sup>	$V_{IL} = V_{DD}$	–	–	100	$\mu A$
$I_{DDA}$	PLL Supply Current	AVDD only	–	5	10	mA
$I_{DDQ}$	Quiescent Supply Current	All VDD pins except AVDD	–	–	7	mA
$I_{DD}$	Dynamic Supply Current	Outputs loaded @ 100 MHz	–	270	–	mA
		Outputs loaded @ 200 MHz	–	300	–	
$C_{IN}$	Input Pin Capacitance		–	4	–	pF
$Z_{OUT}$	Output Impedance		12	15	18	$\Omega$

**AC Electrical Specifications** ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>[7]</sup>

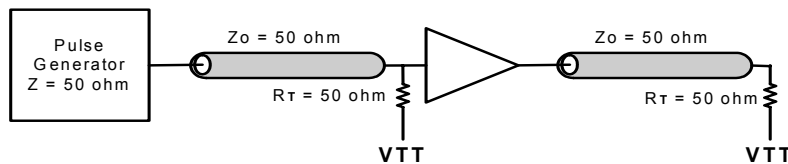
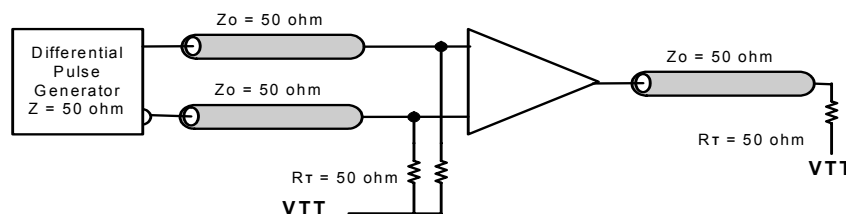
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$f_{VCO}$	VCO Frequency		200	–	380	MHz
$f_{in}$	Input Frequency	$\div 2$ Feedback	100	–	190	MHz
		$\div 4$ Feedback	50	–	95	
		$\div 8$ Feedback	25	–	47.5	
		Bypass mode (PLL_EN = 0)	0	–	200	
$f_{refDC}$	Input Duty Cycle		25	–	75	%
$V_{PP}$	Peak-Peak Input Voltage	LVPECL	500	–	1000	mV
$V_{CMR}$	Common Mode Range <sup>[8]</sup>	LVPECL	1.2	–	$V_{DD} - 0.6$	V
$t_r, t_f$	TCLK Input Rise/Fall Time	0.7V to 1.7V	–	–	1.0	ns
$f_{MAX}$	Maximum Output Frequency	$\div 2$ Output	100	–	190	MHz
		$\div 4$ Output	50	–	95	
		$\div 8$ Output	25	–	47.5	
DC	Output Duty Cycle	$f_{MAX} < 100$ MHz	47.5	–	52.5	%
		$f_{MAX} > 100$ MHz	45	–	55	
$t_r, t_f$	Output Rise/Fall times	0.6V to 1.8V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN	–100	–	100	ps
		PCLK to FB_IN	–100	–	100	
$t_{sk(O)}$	Output-to-Output Skew		–	–	150	ps
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns
BW	PLL Closed Loop Bandwidth (–3dB)	$\div 2$ Feedback	–	2.2	–	MHz
		$\div 4$ Feedback	–	0.85	–	
		$\div 8$ Feedback	–	0.6	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period Jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	175	
$t_{JIT(\phi)}$	I/O Phase Jitter		–	175	–	ps
$t_{LOCK}$	Maximum PLL Lock Time		–	–	1	ms

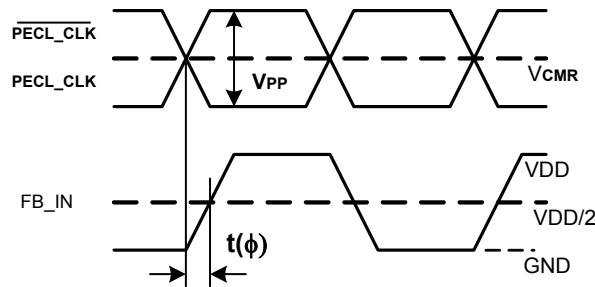
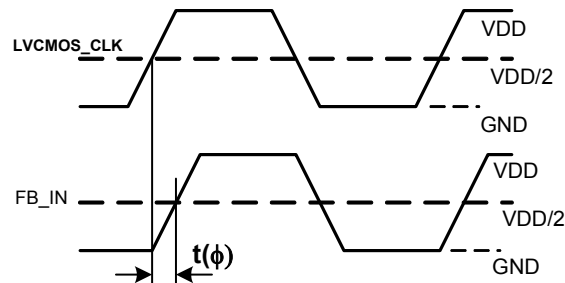
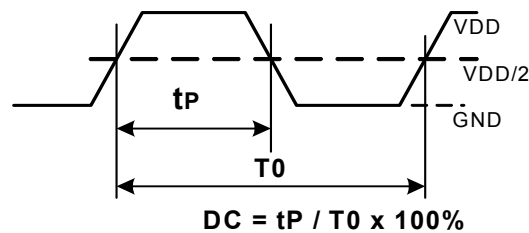
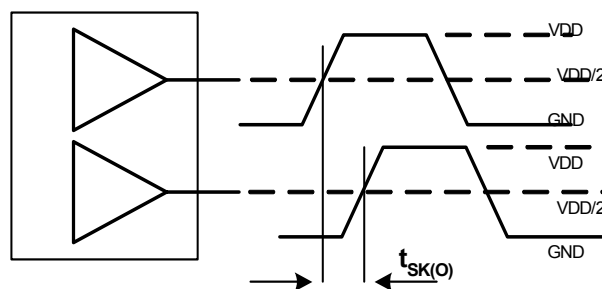
**Notes:**

- AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{TT}$ . Parameters are guaranteed by characterization and are not 100% tested.
- $V_{CMR}$  (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the  $V_{CMR}$  range and the input swing lies within the  $V_{PP}$  (AC) specification. Violation of  $V_{CMR}$  or  $V_{PP}$  impacts static phase offset  $t_{(\phi)}$ .

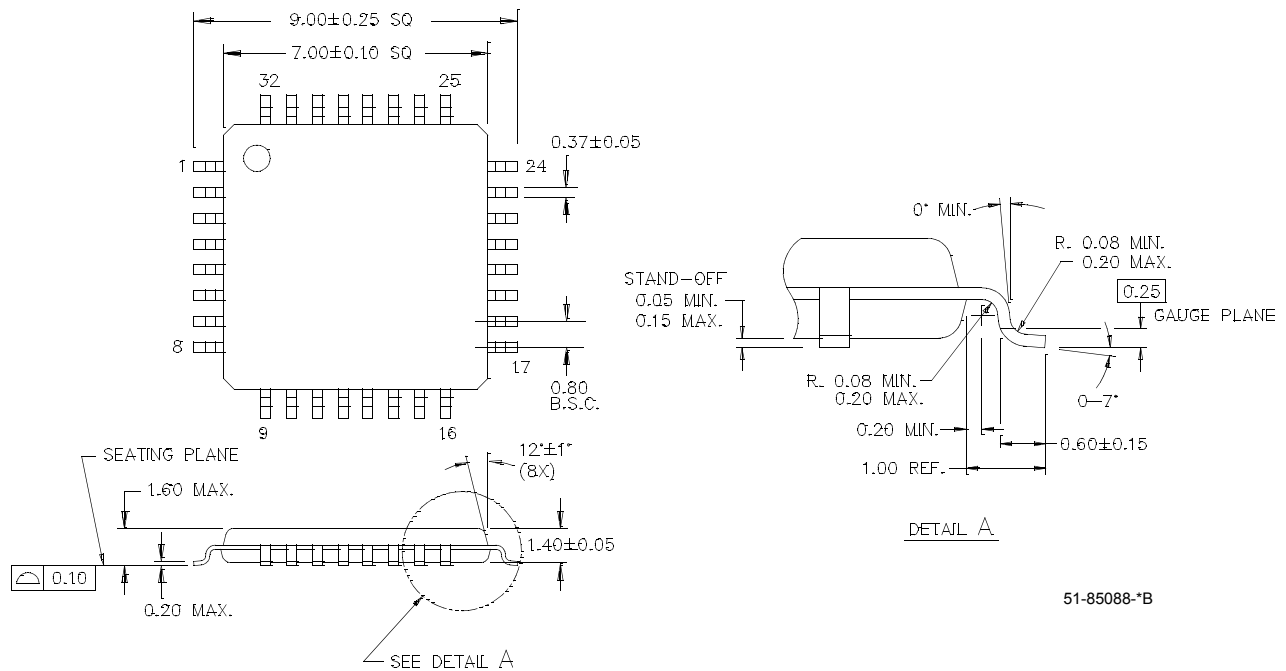
**AC Electrical Specifications** ( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ) [7]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$f_{VCO}$	VCO Frequency		200	–	500	MHz
$f_{in}$	Input Frequency	$\div 2$ Feedback	100	–	200	MHz
		$\div 4$ Feedback	50	–	125	
		$\div 8$ Feedback	25	–	62.5	
		Bypass mode (PLL_EN = 0)	0	–	200	
$f_{refDC}$	Input Duty Cycle		25	–	75	%
$V_{PP}$	Peak-Peak Input Voltage	LVPECL	500	–	1000	mV
$V_{CMR}$	Common Mode Range <sup>[8]</sup>	LVPECL	1.2	–	$V_{DD} - 0.9$	V
$t_r, t_f$	TCLK Input Rise/Fall Time	0.8V to 2.0V	–	–	1.0	ns
$f_{MAX}$	Maximum Output Frequency	$\div 2$ Output	100	–	200	MHz
		$\div 4$ Output	50	–	125	
		$\div 8$ Output	25	–	62.5	
DC	Output Duty Cycle	$f_{MAX} < 100$ MHz	47.5	–	52.5	%
		$f_{MAX} > 100$ MHz	45	–	55	
$t_r, t_f$	Output Rise/Fall times	0.8V to 2.4V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD	–100	–	100	ps
		PCLK to FB_IN, same VDD	–100	–	100	
$t_{sk(O)}$	Output-to-Output Skew	Banks at same voltage	–	–	150	ps
$t_{sk(B)}$	Bank-to-Bank Skew	Banks at different voltages	–	–	350	ps
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns
BW	PLL Closed Loop Bandwidth (–3dB)	$\div 2$ Feedback	–	2.2	–	MHz
		$\div 4$ Feedback	–	0.85	–	
		$\div 8$ Feedback	–	0.6	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period Jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	150	
$t_{JIT(\phi)}$	I/O Phase Jitter	I/O same $V_{DD}$	–	175	–	ps
$t_{LOCK}$	Maximum PLL Lock Time		–	–	1	ms


**Figure 1. LVC MOS\_CLK AC Test Reference for  $V_{DD} = 3.3V / 2.5V$** 

**Figure 2. PECL\_CLK AC Test Reference for  $V_{DD} = 3.3V / 2.5V$**


**Figure 3. LVPECL Propagation Delay  $t(\phi)$ , static phase offset**

**Figure 4. LVCMOS Propagation Delay  $t(\phi)$ , static phase offset**

**Figure 5. Output Duty Cycle (DC)**

**Figure 6. Output-to-Output Skew,  $t_{sk(O)}$** 
**Ordering Information**

Part Number	Package Type	Product Flow
CY29351AI	32-pin TQFP	Industrial, $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
CY29351AIT	32-pin TQFP – Tape and Reel	Industrial, $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$

**Package Drawing and Dimension**
**32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14**


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**Document History Page**

<b>Document Title: CY29351 2.5V or 3.3V, 200-MHz, 9-Output Zero Delay Buffer</b> <b>Document Number: 38-07475</b>				
<b>REV.</b>	<b>ECN No.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	128152	07/07/03	RGL	New Data Sheet
*A	245448	See ECN	RGL	Re-worded Select Function Descriptions in table 2.



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