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PRODUCT INFORMATION

MC68349
MC68349V

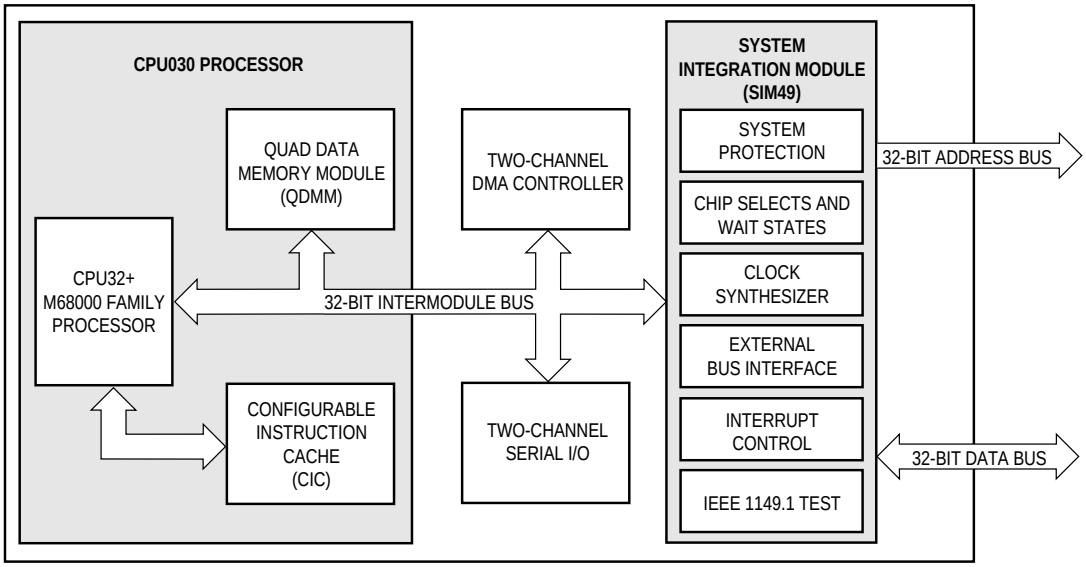
Product Brief

Dragon I™—
High Performance Integrated Processor

The MC68349 Dragon I is the highest performance member of the Motorola M68300 family of integrated processors. The MC68349 is designed to serve as the central processor of personal intelligent communicators (PICs) and similar products requiring an optimal balance of performance, integration, cost, and power consumption. The MC68349 is the first in a series of M68300 family integrated processors designed specifically to support rigorous requirements of consumer-oriented intelligent personal electronics.

The MC68349 is based on the powerful CPU030 processor which combines a full 32-bit central processor with a configurable instruction cache and dedicated data memory structures. The MC68349 also incorporates a high-speed 32-bit dual direct memory access (DMA) controller, a two-channel serial communications interface, and clock synthesis, power management functions, system protection features, and a glueless memory interface.

The MC68349 is fully compatible with previous members of the M68000 family and offers a long-term future migration path to successors based on MC68040 and MC68060 processors. The modular nature of the MC68349 also provides for cost-effective migration paths to higher levels of integration in future products.



MC68349 Block Diagram

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The primary features of the MC68349 include:

- High-Performance CPU030 Processor
  - —CPU32+ 32-Bit Execution Unit
    - M68000 Upward User Code Compatible
    - 32-Bit Bus Interface
    - Two-Clock Instruction Execution Rate
  - —Configurable Instruction Cache (CIC)
    - Four Independent Blocks, Each Configurable as Cache or SRAM
    - 1-Kbyte Instruction Cache or 2-Kbyte SRAM Total Storage
    - Four-Way Set Associative (All Blocks Configured as Cache)
    - Each Block Independently Lockable
    - Supports Simultaneous CPU and DMA Bus Activity
  - —Quad Data Memory Module (QDMM)
    - Four Independent 1-Kbyte SRAM Blocks
    - Useful for Scratchpad, Variable Storage, and Stacks
    - Each Block Independently Mapped and Protected
- High-Speed 32-Bit Dual DMA Controllers for Low-Latency Data Transfers
  - —Full 32-Bit Data Transfers for Highest Performance
  - —50-Mbyte/Sec Sustained Transfer Rate
  - —Dual or Single Address Transfers
  - —8-, 16-, or 32-Bit Transfers
- Dual Serial Communication Ports
  - —Synchronous or Asynchronous Operation
  - —3-Mbit/Sec Sustained Transfer Rate
  - —Modem Control
  - —Baud Rate Generation
  - —MC68681/MC2681 Compatible
- System Integration Module for Flexible and Cost-Effective System Interface
  - —32-Bit Address Bus
  - —32-Bit Data Bus with Dynamic Bus Sizing
  - —System Protection, Reset, and Configuration Control
  - —Chip-Select, Wait State Generation, Bus Watchdog
  - —Periodic Interrupt/System Timer
  - —Interrupt Controller
  - —Dual 8-Bit Parallel Ports
  - —IEEE 1149.1 Boundary Scan (JTAG)
- Power Management
  - —5 V or 3.3 V Operation
  - —Fully Static HCMOS Technology
  - —Programmable Clock Synthesizer for Full Frequency Control
  - —Power-Down/Low Power Stop Capabilities
  - —Idle Modules Can Be Individually Powered Down
- 32-Bit Data Paths for On-Chip and Off-Chip Access
- 0–16- or 25-MHz Operation
- 160-Pin Plastic QFP

CPU030 CENTRAL PROCESSING UNIT

Processing power for the MC68349 is provided by the CPU030 central processing unit. The CPU030 delivers MC68030 performance in a form factor that is highly optimized for the needs of portable intelligent personal electronics applications. The CPU030 is a modular processor whose configuration can be modified to suit the requirements of many different classes of applications.

The CPU030 employed in the MC68349 is composed of three principle modular elements: the CPU32+ 32-bit processor , a configurable instruction cache module, and a quad data memory module. Memory management is an option not supported in the MC68349.

CPU32+ PROCESSOR

The CPU32+ processor is the full 32-bit extension of the CPU32 processor found on many M68300 family of integrated processors and provides the execution units for the CPU030. The CPU32+ provides 32-bit execution units and 32-bit data paths (internal and external) and has a basic instruction execution rate of two clock periods for a 32-bit operation. The CPU32+ is completely upward software compatible with the MC68000 and CPU32.

In addition to performing basic instruction execution, the CPU32+ also provides central power management capabilities to the MC68349 as well as a sophisticated background debug port for non-invasive instrumentation in the software development and debug environments.

CONFIGURABLE INSTRUCTION CACHE (CIC)

The CIC is a highly configurable memory resource designed to optimize the supply of instructions to the CPU030 while moderating power consumption by reducing external accesses. Considerable flexibility in the handling of instructions is provided by the CIC to allow the operating systems programmer to ensure deterministic response to real-time events while also maximizing average or statistical performance.

The CIC is composed of four identical blocks each of which can be independently configured as a 256-byte instruction cache or as a 512-byte static random access memory (SRAM). When configured as an SRAM, a block is independently relocatable in the system's address space. When configured as a cache, a block operates as a direct-mapped cache of sixty-four 32-bit entries. When multiple blocks are configured as caches, set-associativity is supported up to a maximum of four sets. Each cache block can be independently locked to freeze its internal contents.

Using CIC flexibility, it is feasible to place high-priority interrupt or operating system routines in protected SRAM, which is always instantly available, while allowing remaining blocks to operate as caches to increase the performance of general system and user tasks. The CIC configuration can be established at system initialization or on a task-by-task basis, yielding maximum flexibility.

QUAD DATA MEMORY MODULE (QDMM)

The QDMM provides dedicated data storage resources for the CPU030 in the form of four, independent, 1-Kbyte SRAM blocks. Each of these blocks can be independently relocated anywhere in the system address space, and each is independently protected (supervisor/user, read/write).

The QDMM can be used as scratchpad memory, stack caches for independent tasks, buffers for I/O operations, or parameter storage. The QDMM does not provide direct data caching due to the real-time nature of its anticipated applications, but provides significant performance and power-management benefits to MC68349-based systems.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce parts count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules and typical glue logic. These functions on the MC68349 include a DMA controller, a serial module, and the system integration module.

The processor communicates with these modules over the on-chip intermodule bus (IMB). This backbone of the chip is similar to traditional external buses with address, data, clock, interrupt, arbitration, and handshake signals. Because bus masters (like the CPU32+ and DMA), peripherals, and the SIM49 are all on the chip, the IMB ensures that communication between these modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers, greatly improving system performance. Internal accesses across the IMB can be monitored from outside the chip, if desired.

DMA MODULE

The MC68349 contains a high-speed 32-bit DMA controller to quickly move large blocks of data between internal peripherals, external peripherals, or memory without processor intervention. The DMA module consists of two, independent, programmable channels. Each channel has separate request, acknowledge, and done signals. Each channel can operate in a single-address (flyby) or a dual-address mode. Each channel supports 32 bits of address and 8, 16, or 32 bits of data.

SERIAL MODULE

Most digital systems use serial I/O to communicate with host computers, operator terminals, or remote devices. The MC68349 contains a two-channel, full-duplex universal synchronous/asynchronous receive/transfer (USART). An on-chip baud rate generator provides standard baud rates up to 76.8k baud independently to each channel's receiver and transmitter. The module is functionally equivalent to the MC68681/MC2681 dual universal asynchronous receive/transfer (DUART).

SYSTEM INTEGRATION MODULE

The MC68349 system integration module (SIM49) handles a wide array of functions, eliminating the need for much of the glue logic which typically supports the microprocessor and its interface with peripherals and external memory. The SIM49 includes:

- External Bus Interface—Transfers information between the CPU32+ or DMA controller and external memory or peripherals by providing up to 32 address lines and 32 data lines.
- System Configuration and Protection—Achieves maximum system protection by providing various monitors and timers to prevent system lockup, recover from catastrophic failure, exit infinite loops, provide refresh, etc.
- Clock Synthesizer—Generates the clock signals used by all internal operations as well as a clock output used by external devices.
- Chip Select and Wait State Generation—Offers four programmable chip selects which provide signals to enable external memory and peripheral circuits and create all external handshaking and timing signals.
- Interrupt Control—Provides up to seven discrete interrupt inputs for external devices.
- IEEE 1149.1 Test Access Port (JTAG)—Aids in system diagnostics by providing dedicated, user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability.

PERSONAL INTELLIGENT COMMUNICATIONS

Representing a new class of consumer electronics, the PIC is oriented towards providing maximum personal productivity to its user in a form-factor emphasizing low cost, minimal physical size, extended operation on batteries, seamless communications in a complex wireless/wireline environment, and extreme ease-of-use.

The solution to the needs of the PIC applications requires a carefully selected balance of performance and integration to satisfy the system's functional requirements while also meeting rigorous cost, weight, and power consumption. The MC68349 was developed to the specifications of General Magic and its Alliance Founders and, coupled with the proprietary Astro™ circuit, provides the complete digital core of a PIC.

The MC68349 represents a carefully selected balance of capabilities oriented towards enabling the PIC vision:

- Advanced Motorola CMOS Process for Proven Reliability and Low Cost
- Static Design and Extensive Power Management for Long Battery Life
- Highly Integrated for Low Power, Low System Cost and High Reliability
- CPU030 Provides 8 to 10 Sustained MIPS for Support of Advanced User Interfaces
- Integration of Key System Functions for Performance/Power Optimizations
- M68000 Architecture Provides Strong Software Base and Upward Migration Paths

ADDITIONAL APPLICATION AREAS

While specifically optimized for the needs of personal intelligent communications, the MC68349 was partitioned to provide the general-purpose elements of the PIC application while highly specialized features were placed in a proprietary companion circuit. Thus, the MC68349 can provide substantial benefit to other application areas as well.

In general, applications requiring moderate performance, low power consumption, high-bandwidth DMA, and cost-effectiveness can be well-serviced by the MC68349. In addition, since the MC68349 is a member of the M68000 family, its users have access to a broad range of superior support tools and services to facilitate rapid system development and deployment.

Application areas suited to the MC68349 include:

- Personal Digital Assistants (PDAs)
- I/O Processors for High-Performance Systems
- Real-Time Control Processors
- Sophisticated 32-Bit DMA Controllers

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The following table identifies the packages and operating frequencies available for the MC68349.

MC68349 Package/Frequency Availability

Package	Frequency/Voltage		
	16 MHz/3.3 V	16 MHz/5 V	25 MHz/5 V
Plastic Quad Flat Pack (FT)			

The documents listed in the following table contain detailed information on the MC68349. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Title	Order Number
M68300 Integrated Processor Family	BR1114/D
MC68349 User's Manual	MC68349UM/AD
M68000 Family Programmer's Reference Manual	M68000PM/AD
DRAM Controller for the MC68340	AN1063/D
Software Implementation of SPI on the MC68340	AN453
The 68K Source	BR729/D
3.3 Volt Logic and Interface Circuits	BR1407/D

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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