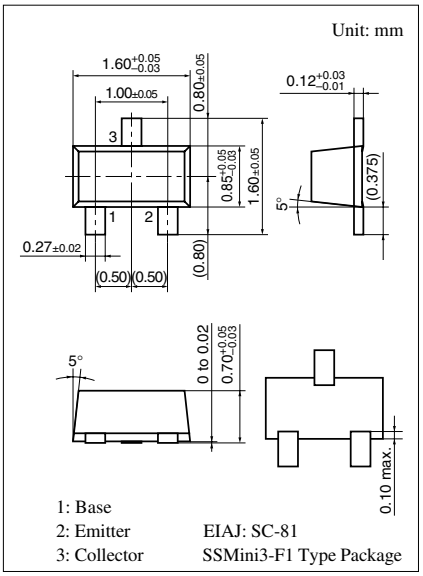
UNR911TJ (UN911TJ)

Silicon PNP epitaxial planer type

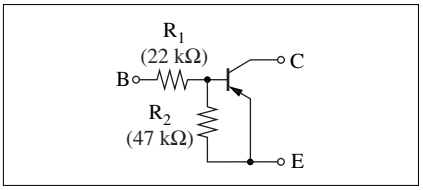
For digital circuit

For switching



Marking Symbol: EY

Internal Connection



■ Features

- Costs can be reduced through downsizing of the equipment and reduction of the number of parts.
- SS-mini type package, allowing automatic insertion through tape packing.
- Flat lead type, high mounting efficiency

■ Absolute Maximum Ratings $T_a = 25°C$

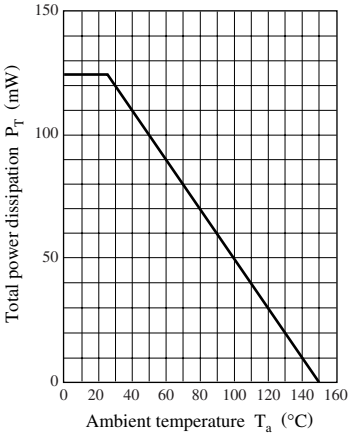
Parameter	Symbol	Rating	Unit
Collector to base voltage	V_{CBO}	−50	V
Collector to emitter voltage	V_{CEO}	−50	V
Collector current	I_C	−100	mA
Total power dissipation	P_T	125	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

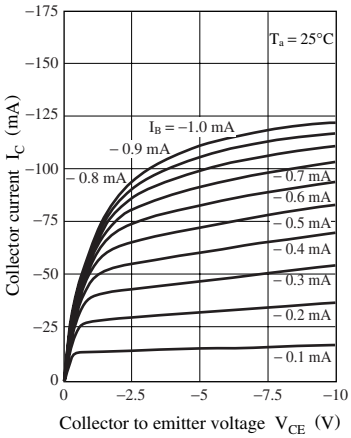
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector cutoff current	I_{CBO}	$V_{CB} = -50$ V, $I_E = 0$			− 0.1	μA
	I_{CEO}	$V_{CE} = -50$ V, $I_B = 0$			− 0.5	μA
Emitter cutoff current	I_{EBO}	$V_{EB} = -6$ V, $I_C = 0$			− 0.2	mA
Collector to base voltage	V_{CBO}	$I_C = -10$ μA, $I_E = 0$	−50			V
Collector to emitter voltage	V_{CEO}	$I_C = -2$ mA, $I_B = 0$	−50			V
Forward current transfer ratio	h_{FE}	$V_{CE} = -10$ V, $I_C = -5$ mA	80		400	
Collector to emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10$ mA, $I_B = -0.3$ mA			− 0.25	V
High-level output voltage	V_{OH}	$V_{CC} = -5$ V, $V_B = -0.5$ V, $R_L = 1$ kΩ	−4.9			V
Low-level output voltage	V_{OL}	$V_{CC} = -5$ V, $V_B = -2.5$ V, $R_L = 1$ kΩ			− 0.2	V
Input resistance	R_1		−30%	22	+30%	kΩ
Resistance ratio	R_1/R_2			0.47		
Transition frequency	f_T	$V_{CB} = -10$ V, $I_E = 1$ mA, f = 200 MHz		80		MHz

Note) The part number in the parenthesis shows conventional part number.

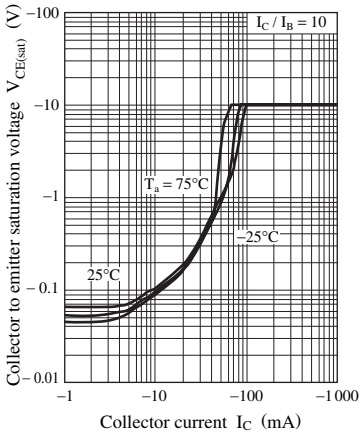
P_T — T_a



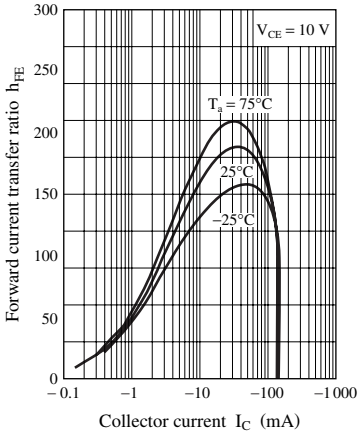
I_C — V_{CE}



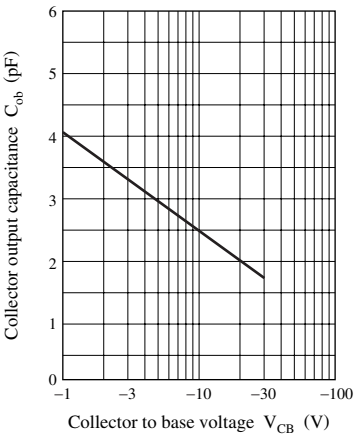
$V_{CE(sat)}$ — I_C



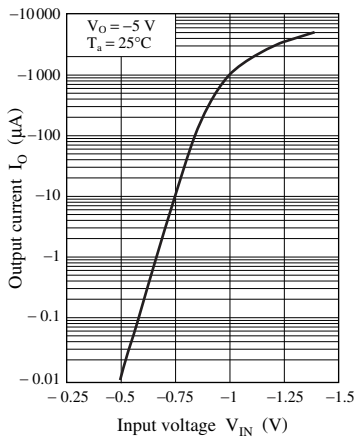
h_{FE} — I_C



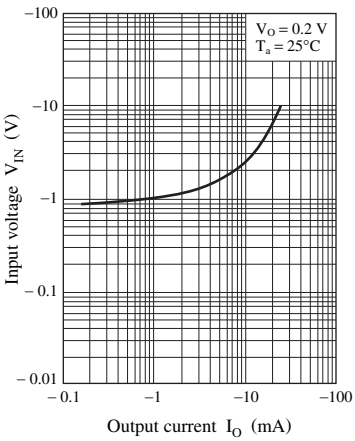
C_{ob} — V_{CB}



I_O — V_{IN}



V_{IN} — I_O



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