LTC1067/LTC1067-50

Rail-to-Rail, Very Low Noise Universal Dual Filter Building Block

February 1998

FEATURES

- **Dual 2nd Order Filter in a 16-Lead SO Package**
- **Rail-to-Rail Input and Output Operation**
- **Operates from a Single 3V to ±5V Supply**
- > 80dB Dynamic Range on Single 3.3V Supply
- Clock-to-Center Frequency Ratio of 100:1 for the LTC1067 and 50:1 for the LTC1067-50
- Internal Sampling-to-Center Frequency Ratio of 200:1 for the LTC1067 and 100:1 for the LTC1067-50
- Center Frequency Error < ±0.2% Typ
- Low Noise: < 40μV_{RMS}, Q ≤ 5
- Customizable with Internal Resistors

APPLICATIONS

- Data Acquisition Filters
- Telecom Filters
- Noise Reduction Systems

DESCRIPTION

The LTC®1067/LTC1067-50 consist of two identical rail-to-rail, high accuracy and very wide dynamic range 2nd order switched-capacitor building blocks. Each building block, together with three to five resistors, provides 2nd order filter functions such as bandpass, highpass, lowpass, notch and allpass. High precision 4th order filters are easily designed.

The center frequency of each 2nd order section is tuned by the external clock frequency. The internal clock-to-center frequency ratio (100:1 for the LTC1067 and 50:1 for the LTC1067-50) can be modified by the external resistors. These devices have a double sampled architecture which places aliasing and imaging components at twice the clock frequency. The LTC1067-50 is a low power device consuming about one half the current of the LTC1067. The LTC1067-50's typical supply current is about 1mA from a 3.3V supply.

The LTC1067 and LTC1067-50 are available in 16-pin GN and SO packages.

Mask programmable versions of the LTC1067 and LTC1067-50, with thin film resistors on-chip and custom clock-to-cutoff frequency ratios, can be designed to realize application specific monolithic filters, in an SO-8 package. Please contact LTC Marketing for more details.

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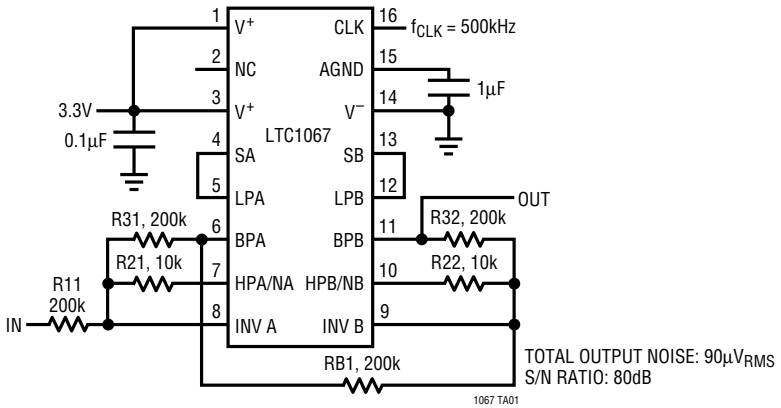
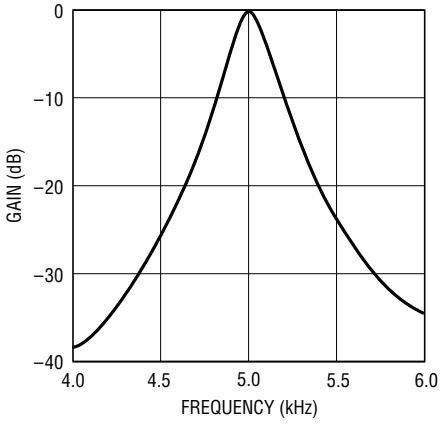
TYPICAL APPLICATION

Single 3.3V Supply Rail-to-Rail, 4th Order, 5kHz Bandpass Filter



Frequency Response



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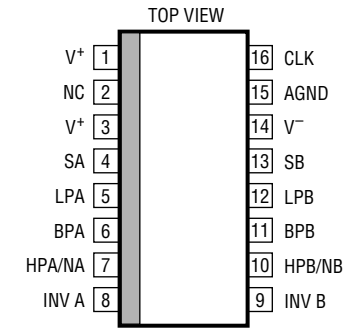
ABSOLUTE MAXIMUM RATINGS

Total Voltage Supply (V^+ to V^-) 12V
Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 500mV
Operating Temperature Range
LTC1067C ..... 0°C to 70°C
LTC1067I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 135°C/W (GN)
T_{JMAX} = 110°C, θ_{JA} = 115°C/W (S)

ORDER PART NUMBER

LTC1067CGN
LTC1067-50CGN
LTC1067IGN
LTC1067-50IGN
LTC1067CS
LTC1067-50CS
LTC1067IS
LTC1067-50IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

LTC1067 (internal op amps) V_S = 4.75V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			3		11	V
Positive Output Voltage Swing	V_S = 3V, R_L = 10k	●	2.65	2.80		V
	V_S = 4.75V, R_L = 10k	●	4.25	4.50		V
	V_S = ±5V, R_L = 10k	●	4.15	4.50		V
Negative Output Voltage Swing	V_S = 3V, R_L = 10k	●		0.020	0.200	V
	V_S = 4.75V, R_L = 10k	●		0.025	0.225	V
	V_S = ±5V, R_L = 10k	●		–4.96	–4.80	V
Output Short-Circuit Current (Source/Sink)	V_S = 3V			16/1.0		mA
	V_S = 4.75V			33/2.2		mA
	V_S = ±5V			70/7.2		mA
DC Open-Loop Gain	R_L = 10k			90		dB
GBW Product	R_L = 10k			2.8		MHz
Slew Rate	R_L = 10k			2.25		V/µs

LTC1067 (complete filter) V_S = 4.75V, f_{CLK} = 250kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O (Note 1)				0.001 to 20		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_O	V_S = 3V, f_{CLK} = 250kHz, Mode 1, f_O = 2.5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
	V_S = 4.75V, f_{CLK} = 250kHz, Mode 1, f_O = 2.5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
	V_S = ±5V, f_{CLK} = 500kHz, Mode 1, f_O = 5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S = 3V, f_{CLK} = 250kHz, Q = 5	●		±0.1	±0.35	%
	V_S = 4.75V, f_{CLK} = 250kHz, Q = 5	●		±0.1	±0.35	%
	V_S = ±5V, f_{CLK} = 500kHz, Q = 5	●		±0.1	±0.35	%

ELECTRICAL CHARACTERISTICS

LTC1067 (complete filter) V_S = 4.75V, f_{CLK} = 250kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Q Accuracy	V_S = 3V, f_{CLK} = 250kHz, Q = 5	●		0.5	2	%
	V_S = 4.75V, f_{CLK} = 250kHz, Q = 5	●		0.5	2	%
	V_S = ±5V, f_{CLK} = 500kHz, Q = 5	●		0.5	2	%
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (See Table 2)	V_{OS1} (DC Offset of Input Inverter)	●		3	12.5	mV
	V_{OS2} (DC Offset of First Integrator)	●		4	15.0	mV
	V_{OS3} (DC Offset of Second Integrator)	●		4	15.0	mV
Clock Feedthrough				150		μV_{RMS}
Maximum Clock Frequency	Q < 2.5, V_S = ±5V			2.0		MHz
Power Supply Current	V_S = 3V, f_{CLK} = 250kHz	●		2.50	4.5	mA
	V_S = 4.75V, f_{CLK} = 250kHz	●		3.00	5.5	mA
	V_S = ±5V, f_{CLK} = 500kHz	●		4.35	7.5	mA

LTC1067-50 (internal op amps) V_S = 4.75V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			2.7		11	V
Positive Output Voltage Swing	V_S = 3V, R_L = 10k	●	2.65	2.80		V
	V_S = 4.75V, R_L = 10k	●	4.25	4.50		V
	V_S = ±5V, R_L = 10k	●	4.15	4.50		V
Negative Output Voltage Swing	V_S = 3V, R_L = 10k	●		0.020	0.200	V
	V_S = 4.75V, R_L = 10k	●		0.025	0.225	V
	V_S = ±5V, R_L = 10k	●		–4.96	–4.80	V
Output Short-Circuit Current (Source/Sink)	V_S = 3V			16/0.6		mA
	V_S = 4.75V			33/1.2		mA
	V_S = ±5V			70/5.7		mA
DC Open-Loop Gain	R_L = 10k			90		dB
GBW Product	R_L = 10k			1.9		MHz
Slew Rate	R_L = 10k			0.8		V/µs

LTC1067-50 (complete filter) V_S = 4.75V, f_{CLK} = 125kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O (Note 1)				0.001 to 40		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_O	V_S = 3V, f_{CLK} = 125kHz, Mode 1, f_O = 2.5kHz, Q = 5			50:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
	V_S = 4.75V, f_{CLK} = 125kHz, Mode 1, f_O = 2.5kHz, Q = 5			50:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
	V_S = ±5V, f_{CLK} = 250kHz, Mode 1, f_O = 5kHz, Q = 5			50:1 ±0.3		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S = 3V, f_{CLK} = 125kHz, Q = 5	●		±0.2	±0.55	%
	V_S = 4.75V, f_{CLK} = 125kHz, Q = 5	●		±0.2	±0.55	%
	V_S = ±5V, f_{CLK} = 250kHz, Q = 5	●		±0.2	±0.55	%
Q Accuracy	V_S = 3V, f_{CLK} = 125kHz, Q = 5	●		±0.5	±2	%
	V_S = 4.75V, f_{CLK} = 125kHz, Q = 5	●		±0.5	±2	%
	V_S = ±5V, f_{CLK} = 250kHz, Q = 5	●		±0.5	±2	%

ELECTRICAL CHARACTERISTICS

LTC1067-50 (complete filter) V_S = 4.75V, f_{CLK} = 125kHz, T_A = 25°C, unless otherwise noted.

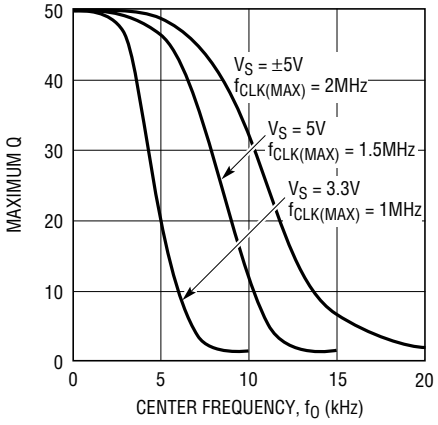
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (See Table 2)	V_{OS1} (DC Offset of Input Inverter)	●		3	12.5	mV
	V_{OS2} (DC Offset of First Integrator)	●		4	15.0	mV
	V_{OS3} (DC Offset of Second Integrator)	●		4	15.0	mV
Clock Feedthrough				150		μV_{RMS}
Maximum Clock Frequency	Q < 2.5, V_S = ±5V			2.0		MHz
Power Supply Current	V_S = 3V, f_{CLK} = 125kHz	●		1.00	2.5	mA
	V_S = 4.75V, f_{CLK} = 125kHz	●		1.45	3.0	mA
	V_S = ±5V, f_{CLK} = 250kHz	●		2.35	4.0	mA

The ● denotes the specifications which apply over the full operating temperature range.

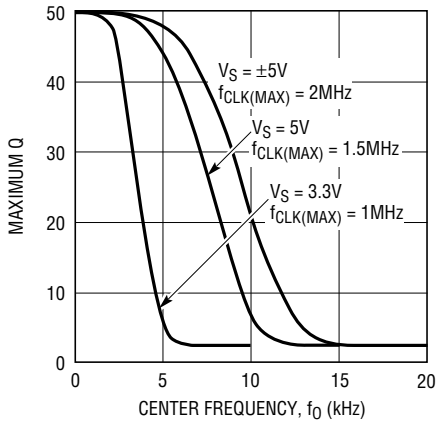
Note 1: See Typical Performance Characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

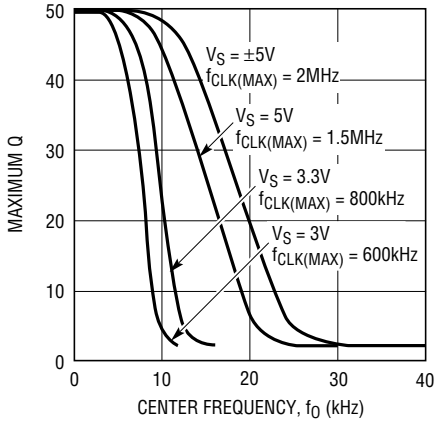
LTC1067 Maximum Q vs Center Frequency (Modes 1, 1B, 2 where R4 ≥ 10R2)



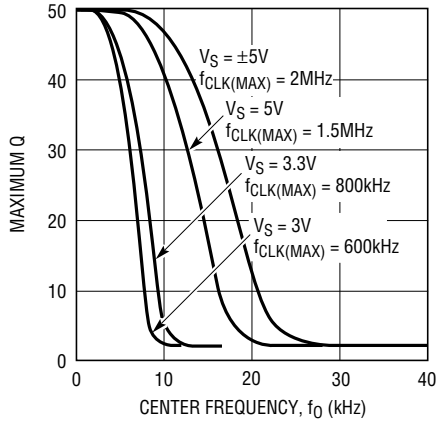
LTC1067 Maximum Q vs Center Frequency (Modes 2 where R4 < 10R2, 3)



LTC1067-50 Maximum Q vs Center Frequency (Modes 1, 1B, 2 where R4 ≥ 10R2)



LTC1067-50 Maximum Q vs Center Frequency (Modes 2 where R4 < 10R2, 3)



PIN FUNCTIONS

V^+, V^- (Pins 1, 3,14): The V^+ (Pins 1, 3) and the V^- (Pin 14) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply's power-up slew rate should be less than 1V/µs. When V^+ is applied before V^-, and V^- is allowed to go above ground, a diode should clamp V^- to prevent latch-up. Figures 1 and 2 show typical connections for dual and single supply operation.

SA, SB (Pins 4, 13): Summing Inputs. The summing pins' connection, along with the other resistor connections, determine the circuit topology (mode) of each 2nd order section. These pins should never be left floating.

LPA, BPA, HPA/NA, HPB/NB, BPB, LPB (Pins 5, 6, 7, 10, 11, 12): Output Pins. Each 2nd order section of the LTC1067 has three outputs which typically source 33mA and sink 2mA. Driving coaxial cable, capacitive loads or resistive loads less than 10k will degrade the total harmonic distortion performance of any filter design. When evaluating the distortion or noise performance of a filter, the output should be buffered with a wideband amplifier.

INV A, INV B (Pins 8, 9): Inverting Input. These pins are the high impedance inverting inputs of internal op amps. They are susceptible to stray capacitance coupling to low impedance nodes such as signal outputs and power supply lines. Resistors that are connected from a signal output to the inverting input pin should be located as close to the inverting input as possible.

AGND (Pin 15): Analog Ground. The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation Pin 6 is connected to the analog ground plane. For single supply operation Pin 6 should be bypassed to the analog ground plane with at least a 1µF capacitor. An on-chip resistive voltage divider sets the bias at one-half of the supply.

CLK (Pin 16): Clock Input. Any CMOS logic clock source with a square-wave output and a 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to the clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for dual supply or single supply operation.

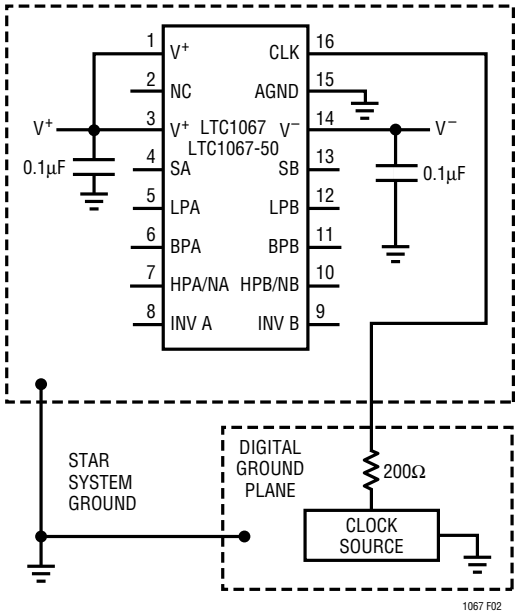
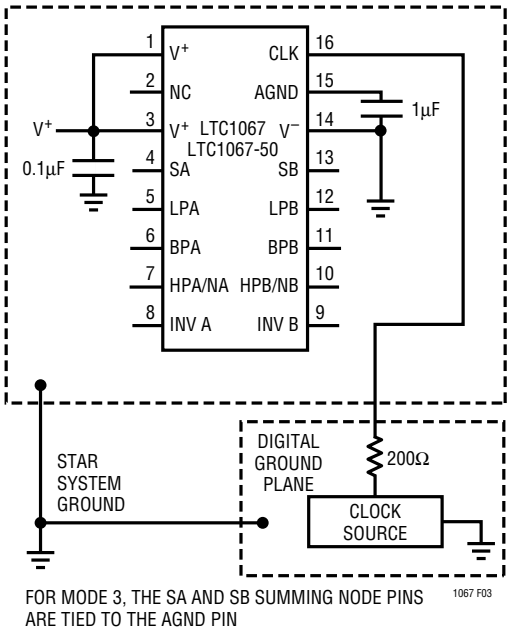


Figure 1. Dual Supply Ground Plane Connections



FOR MODE 3, THE SA AND SB SUMMING NODE PINS ARE TIED TO THE AGND PIN

Figure 2. Single Supply Ground Plane Connections

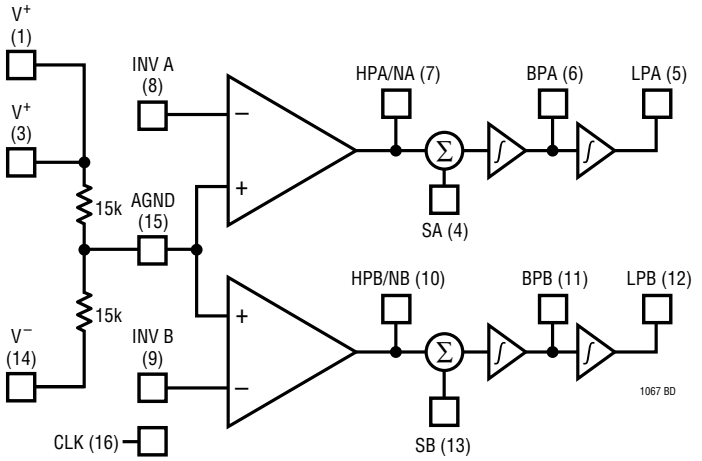
PIN FUNCTIONS

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
±5V	≥ 2.2V	≤ 0.50V
Single 5V	≥ 2.2V	≤ 0.50V
Single 3V, 3.3V	≥ 2V	≤ 0.40V

Sine waves are not recommended for the clock input. The clock signal should be routed from the right side of the IC package to avoid coupling to any power supply lines or input or output signal paths. A 200Ω resistor between the clock source and Pin 16 will slow down the rise and fall times of the clock to reduce charge coupling of the clock. This will result in less clock feedthrough noise on the output signal.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

A switched capacitor integrator generally exhibits a higher input offset than a discrete RC integrator. The larger offset is mainly due to the charge injection from the CMOS switches into the integrated capacitor. The integrator's op amp offset, typically a couple of millivolts, also adds to the overall offset value. Figure 3 shows the input offsets from a single 2nd order section. Table 2 lists the formula for the output offset voltage for various modes and output pins.

Table 2. Output DC Offsets for a Second Order Section

MODE	$V_{OSHP/N}$	V_{OSBP}	V_{OSLP}
1	V_{OS1} [1 + (R2/R3) + (R2/R1)] – (V_{OS3})(R2/R3)	V_{OS3}	$V_{OSHP/N} – V_{OS2}$
1b	V_{OS1} [1 + (R2/R3) + (R2/R1)] – (V_{OS3})(R2/R3)	V_{OS3}	($V_{OSHP/N} – V_{OS2}$)[1 + (R5/R6)]
2	V_{OS1} [1 + (R2/R3) + (R2/R1) + (R2/R4) – (V_{OS3}) (R2/R3)](R4/R2 + R4) + (V_{OS2})(R2/R2 + R4)	V_{OS3}	$V_{OSHP/N} – V_{OS2}$
3	V_{OS2}	V_{OS3}	V_{OS1} [1 + (R4/R1) + (R4/R2) + (R4/R3)] – (V_{OS2}) (R4/R2) – (V_{OS3})(R4/R3)

APPLICATIONS INFORMATION

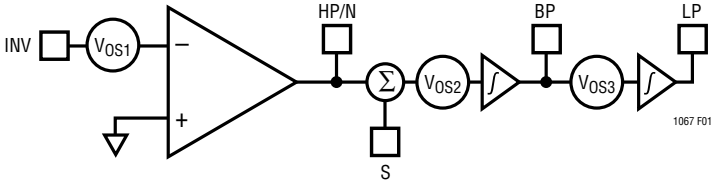
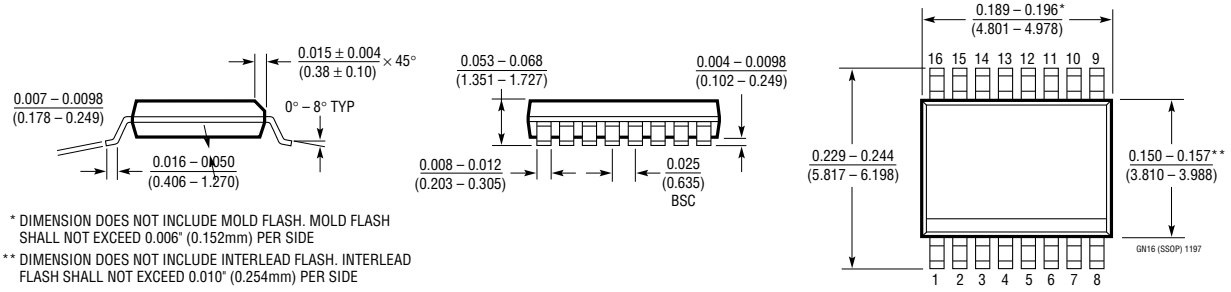


Figure 3. Block Diagram of a 2nd Order Section Showing the Input Offsets

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

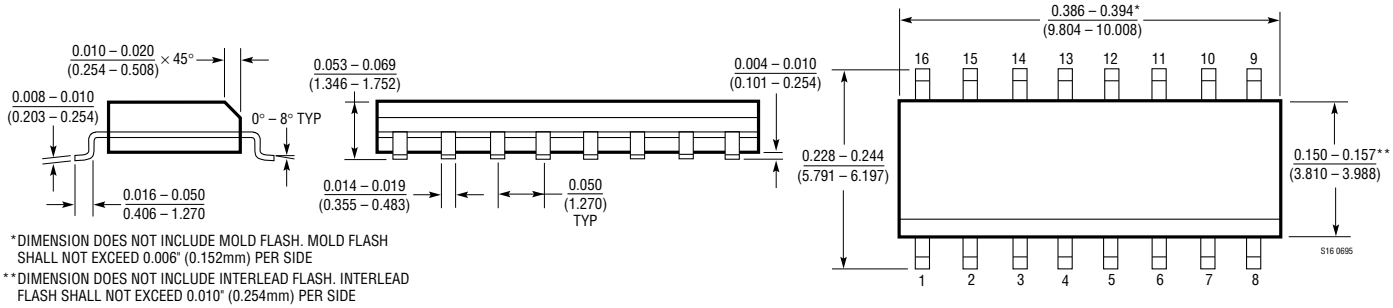
GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

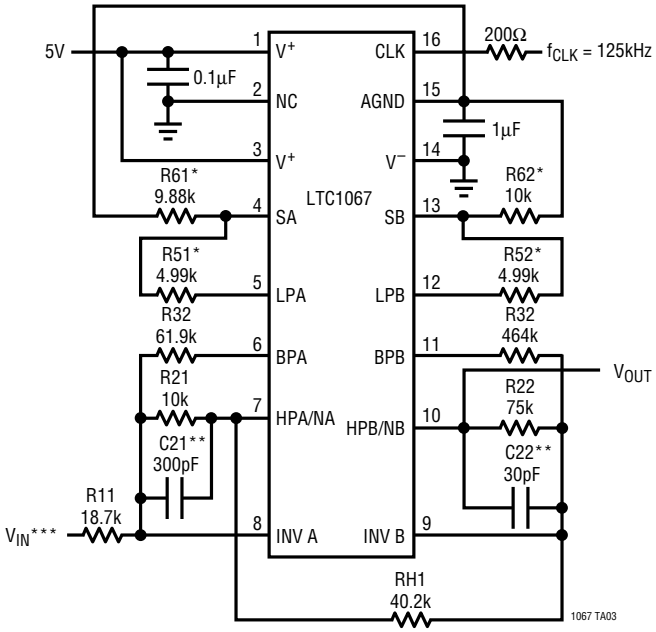


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

1.02kHz Notch Filter for Telecom Systems

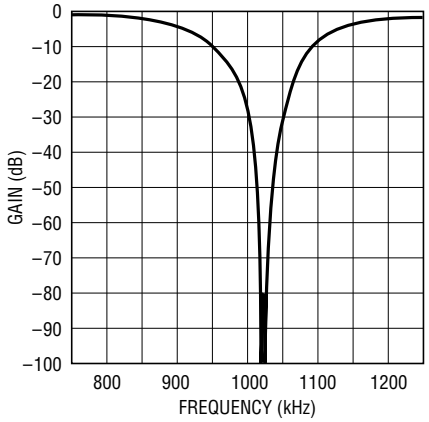


* R51, R61, R52, R62 ARE 0.1% TOLERANCE RESISTORS

** C21 AND C22 IMPROVE THE NOTCH DEPTH WHERE $(30)(f_{NOTCH}) < \frac{1}{2\pi(R2x)(C2X)} < (75)(f_{NOTCH})$ WITHOUT C21 AND C22 THE NOTCH DEPTH IS LIMITED TO –35dB

*** $V_{IN} \leq 1.25V_{P-P}$

Frequency Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064	Low Noise, Low Power Quad Building Block Filter	100:1 Clock-to-f_0 Ratio
LTC1068	Quad Universal Building Block Filter	100:1 Clock-to-f_0 Ratio
LTC1164	Low Power Quad Universal Building Block Filter	50:1 and 100:1 Clock-to-f_0 Ratio
LTC1264	High Speed Quad Universal Building Block Filter	20:1 Clock-to-f_0 Ratio

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