KESTX02

290MHz - 320MHz ASK Transmitter

Preliminary Information

DS4265 ISSUE 3.5 October 2001

The KESTX02 is a single chip ASK (Amplitude Shift Key) transmitter IC. It is designed to operate in a variety of low power radio applications including keyless entry, general domestic and industrial remote control, RF tagging and local paging systems.

The transmitter offers a high level of integration and performance, which enables the harmonic rejection and fundamental power requirements of the FCC part 15, and other governing bodies, to be met.

The basic architecture utilises a crystal reference oscillator, an integrated frequency multiplying PLL and a power output stage. Particular emphasis has been placed on low current drain, including a power–down feature which greatly increases battery life.

Features

- Low supply Current
- Power down feature
- Adjustable output power level
- Low external part count
- Fully integrated VCO, PLL and Power Amplifier

Absolute Maximum Ratings

Junction temperature	–55 to +150°C
Storage temperature	–55 to +150°C
Supply voltage	V_{EE} –0.5 to +8.0 V
Voltage on any pin	V_{EE} –0.5 to V_{CC} +0.5V

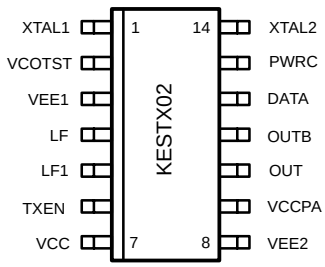
Notes:

1. The voltage on pin OUT and OUTB (open collector outputs) can support a higher voltage than this (+14V).

Ordering Information

KESTX02/IG/MPAD (Tape and Reel)

KESTX02/IG/MPAS (Tubes)



MP14

Figure 1 - Pin connections - top view

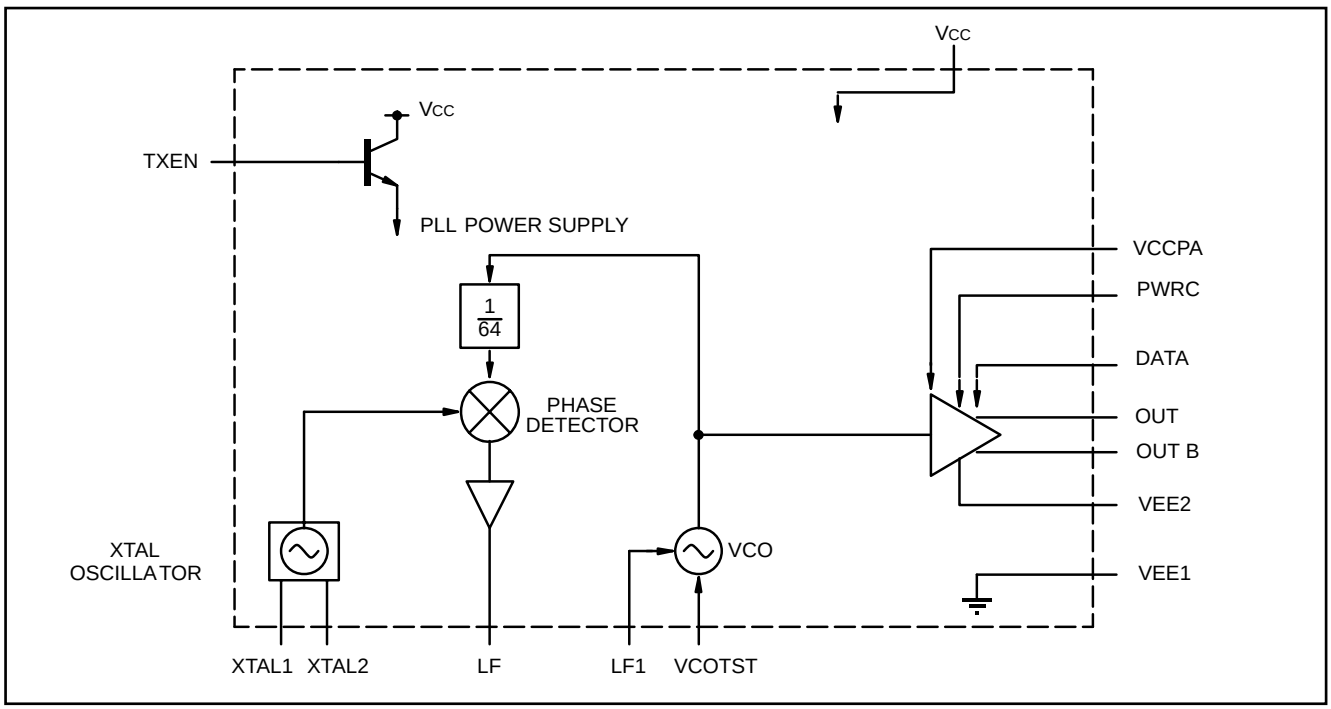


Figure 2 - Block diagram

Electrical Characteristics Operating conditions

T amb = –40°C to + 70°C, V_{CC} = 3.5V to 6.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5		6.5	V	
Ambient temperature	T a	–40		+85	°C	

Electro static discharge 2kV all pins – human body model

Electrical Characteristics D.C.

T amb = –40°C to + 70°C, V_{CC} = 3.5V to 6.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Condition
		Min	Typ	Max		
Supply current stand by mode	$I_{CC}1$			0.7	µA	V_{TXEN} =0V; V_{DATA} =0V;T_a=25°C
Supply current PLL enable/transmit space	$I_{CC}2$		2.50	4	mA	I_{mod} =150µA; V_{CC} =V_{TXEN} =3.5V V_{DATA} =LOW; 315MHz
Supply current PLL enable/transmit mark	$I_{CC}3$		10.5	12.0	mA	I_{mod} =150µA; V_{CC} =V_{TXEN} =3.5V V_{DATA} =HIGH; 315MHz
Supply current PLL enable/transmit space	$I_{CC}4$		3.25	4	mA	I_{mod} =150µA; V_{CC} =V_{TXEN}=6.5V V_{Data} =LOW; 315MHz
Supply current PLL enable/transmit mark see note 1	$I_{CC}5$		11.3	14.5	mA	I_{mod} =150µA; V_{CC} =V_{TXEN} =6.5A; V_{DATA} =HIGH; 315MHz
TXEN – transmit enable	Ven	3.5		V_{CC} +0.2	V	
TXEN – transmit disable/stand by	V dis	V_{EE} –0.2		0.5	V	
Input bias current TXEN	I_{txen}			150	µA	TXEN = V_{CC} transmit enable
Bias voltage pin PWRC			1.20		V	I_{mod} =150µA
Data pin input logic high	V_{ih}	0.7V_{CC}		V_{CC} +0.5	V	
Data pin input logic low	V_{il}	V_{EE} –0.5		0.3V_{CC}	V	
Data pin input current – logic low	I_{inl}	-100			µA	
Data pin input current – logic high	I_{inh}			+100	µA	

Notes:– The maximum supply current is directly related to Imod and hence the output power level (Fig. 4).

Electrical Characteristics A.C.

T amb = –40°C to + 70°C, V_{CC} = 3.5V to 6.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Parameter	Symbol	Value			Units	Condition
		Min	Typ	Max		
Output current at fundamental, V_{CC}=3.5V	IF75	2.1	2.95	3.8	pk–pk mA	I_{mod} =75µA, F_o =315MHz
Output current at fundamental, V_{CC}=3.5V	IF150	2.2	5.3	6.9	pk–pk mA	I_{mod} =150µA, F_o =315MHz
Output current fundamental, V_{CC}=6.5V	IF150 (6V5)	2.6	5.8	7.8	pk–pk mA	I_{mod} =150µA, F_o =315MHz
Output level at 2 x fundamental see note 1				–22	dBc	I_{mod} =150µA, F_o =315MHz
Output level at 3x fundamental and all other spurii see note 1				–11	dBc	I_{mod} =150µA, F_o=315MHz
Phase detector gain	PDG		8		µA/rad	
Extinction ratio see note 2	ER	40	80		dB	
VCO gain	G_{VCO}		100		MHz/V	
TXEN settling time see note 3	Txe			5.0	ms	
Output sidebands due to reference frequency see note 4	SB		–40		dBc	I_{mod} =150µA, F_o =315MHz
30dB rise time, RF envelope of Data pulse	T30R		380		ns	
30dB fall time, RF envelope of Data pulse	T30F		430		ns	
VCO operating frequency		290		320	MHz	

Notes:

1. The spurii are specified relative to the fundamental measured in a 300KHz resolution bandwidth.
2. Extinction ratio is defined as the ratio of the output power "SPACE" to output power "MARK" measured at the output operating frequency.
3. Regulatory issues demand that transmission does not take place until the PLL has acquired lock and the VCO is operating at its final output frequency. This requirement demands that pin TXEN is set high at least Txe ms prior to the transmission of any data. This value is dependent on the PLL loop bandwidth and hence on the value of the external loop filter component values. The specification value above is for the loop filter components shown in the applications diagram (Fig. 6)
4. Sidebands on the output due to the PLL reference are a function of the PLL loop bandwidth and the application. Reducing the closed loop bandwidth of the PLL loop will aid in reducing the level of the PLL reference spurii.

PIN Listing

Signal	Description
XTAL1	Crystal oscillator
XTAL2	Crystal oscillator
DATA	Input data
TXEN	Transmit enable/stand by
OUT	Power amplifier output/antenna interface
OUTB	Power amplifier output/antenna interface (complementary output)
LF	Phase detector output
LF1	VCO control input
PWRC	Output power control
VCCPA	Power amplifier positive supply
VEE2	Power amplifier ground
VEE1	PLL ground
VCC	Positive supply
VCOTST	VCO test control input

Function

When the IC is enabled (TXEN high) a phase locked loop locks the output of the VCO to a multiple of a crystal defined reference input. The output of the VCO operates at the final output frequency and is the input to a power amplifier stage. The power amplifier directly drives the antenna.

Phase locked loop

Dividers

A divide by 64 prescaler is present in the PLL feedback loop. The final output frequency is then Fo = 64xFref.

Phase detector

The phase detector used is a phase frequency detector (PFD) with a current (charge pump) output. This phase detector has a triangular characteristic for an input phase error in the range $-2\pi < \theta e < 2\pi$. The charge pump provides an output current in the range +50μA and hence gives a phase detector gain of $(50/2\pi)$ μA/rad (≈8μA/rad).

The advantage of the PFD over a pure phase detector is that it is also a frequency discriminator and will always lock the loop irrespective of the initial frequency offset. The PLL loop characteristics such as lock–up time, capture range, loop bandwidth and VCO reference sideband suppression are controlled by the external loop filter.

For certain applications spurious sidebands at the reference frequency must be adequately suppressed and a 3rd order loop is recommended.

VCO

To minimize external component costs the VCO is fully integrated. The frequency of the VCO is controlled by the voltage on pin LF.

Reference crystal oscillator

A single transistor Collpits crystal oscillator provides a reference clock for the PLL. The oscillator is configured for parallel resonant operation in the fundamental mode (typical operating frequency of 3–7MHz). The crystal is connected between pins XTAL2 and $V_{EE}1$ with external components as shown in Fig.6.

Alternatively, a reference clock can be provided by an external source connected to pin XTAL2 Fig. 7.

Output stage (PA)

The input signal at pin DATA produces amplitude shift key (ASK) modulation of the VCO output. This is achieved by on–off keying of the bias current in the output power amplifier stage. The output of the PA is a balanced output (pin OUT and OUTB) and is current source driven (open collector outputs). The outputs of which should be D.C. referenced to a positive supply voltage (anticipated to be V_{CC} in most applications). The current source outputs can drive a PCB antenna directly (Fig. 6) or if a higher output power is required on limited supply headroom via a simple impedance transforming network.

A balanced output stage is used as it automatically suppresses the even order harmonics of the fundamental. Of particular importance for the European application is suppression of the 2nd harmonic (due to regulatory issues concerning spurious outputs). In order to obtain the benefits of this output stage it is essential to use a balanced antenna.

Power up

In the intended application it is expected that the transmitter will spend a large proportion of time in ‘‘stand by” not transmitting data. To maximise battery life it is important that very little quiescent current is taken in this mode.

The ‘‘stand by mode” is selected by setting pin TXEN low and similarly the transmitter is enabled by setting TXEN high. To minimize stand–by current TXEN is used to bias an on–chip npn transistor connected in a common collector configuration (Fig. 3). This transistor is used to provide the supply to large portions of the IC. Collapsing the supply when TXEN is set low results in a very low stand by current. The voltage on TXEN should not exceed V_{CC} by more than 0.2V.

From an application standpoint the TXEN pin must be able to source the bias current for the input transistor and should also be decoupled if possible to prevent high frequency noise directly coupling into the IC power supply. The value of the decoupling capacitor and the drive capability of the TXEN source will affect power up delay. Since TXEN enables the PLL it is therefore essential that it is set high prior to any data transmission and that it remains high during the transmission. Therefore three different power drain modes are possible

(i) Stand by (TXEN low, DATA low)
(ii) PLL Mode/Transmit SPACE (TXEN high, DATA low)
(iii) Transmit MARK (TXEN high, DATA high)

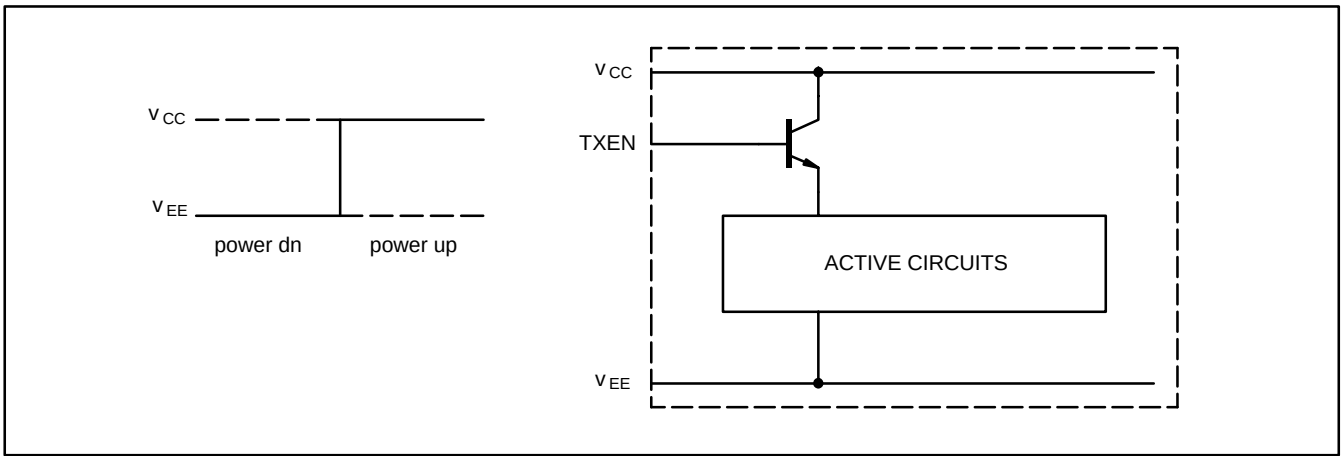


Figure 3 - TXEN power up operation

Applications Information

Power control

The bias current for the power amplifier directly controls the output current (and hence the output power). The bias current is set by the external resistor connected between PWRC and ground. The bias voltage on pin PWRC is nominally 1.20V and hence the modulation current Imod is given by 1.20/R.

To a first order neither the linearity (harmonic spurii relative to fundamental) or the amplifier efficiency are affected by Imod. The graph below shows typical simulation results for the amplifier current output with Imod variation.

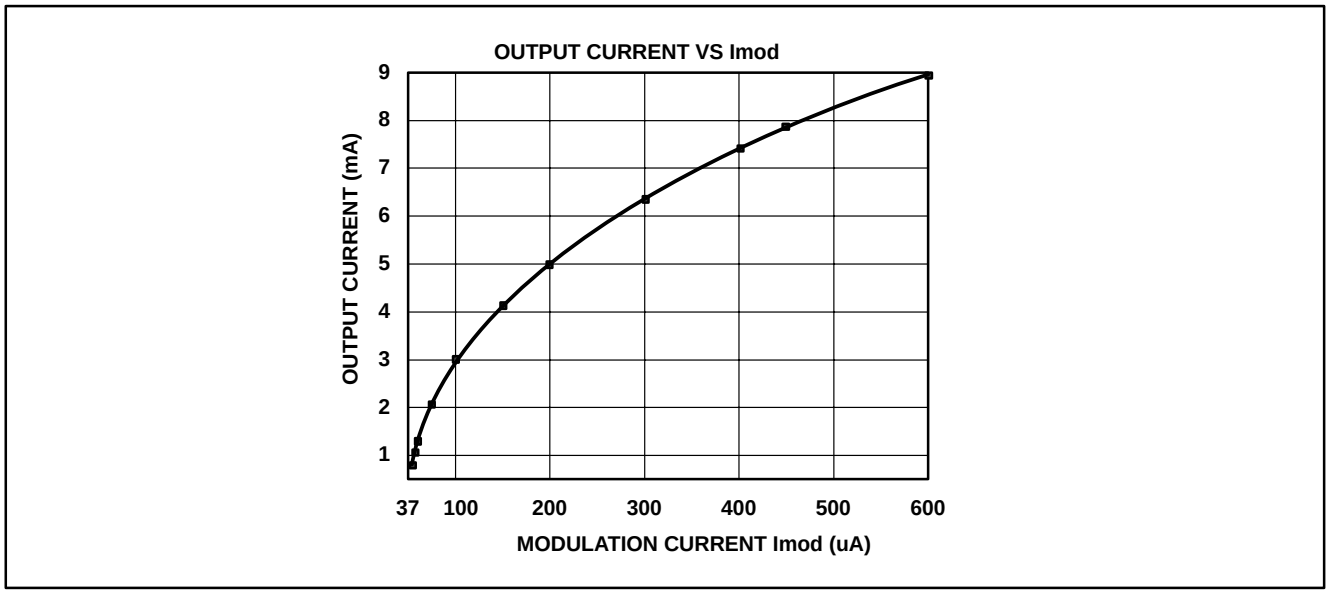


Figure 4 - PWRC power output control

Frequency accuracy

The stability of the output frequency is equal to that of the crystal referenced oscillator and shift in the VCO frequency during data modulation. To operate with a final output accuracy of ± 50KHz at 315MHz (as required for use with the receiver KESRX01) would require a crystal with a tolerance specification of ± 150ppm. This tolerance should encompass all causes e.g. initial accuracy, temperature stability and ageing.

Operation at a final output frequency of 315MHz requires a crystal specified for operation at 4.92MHz.

Antenna interface

The IC is capable of directly interfacing to a PCB loop antenna as shown in the applications diagram (Fig. 6).

The Figure below (Fig. 5) is an equivalent circuit for a PCB loop antenna. The inductance of the loop is Lant and this is in series with two resistors. These represent Rr the radiation resistance and Rs the series resistance of the antenna.

The Q of the antenna is defined as (ωo*Lant/(Rs+Rr) where ωo is the resonant frequency (rad/s) of the antenna. At resonance the antenna can be transformed to the equivalent circuit on the right hand side. Here the equivalent parallel resistance Rp is given by

$$Rp = (Rs + Rr)(Q^2 + 1)$$

For example, Ls=55nH, fo=315MHz, Rs + R r =2.2Ω, Q=50, gives an equivalent parallel resistance of 5.4kΩ.

Typically the antenna will be d.c. referenced to V_{CC} as shown in the applications diagram. The maximum voltage swing across the antenna is therefore limited by the RF saturation voltage of the output PA stage. This is of the order of 0.5V and hence the peak to peak voltage across the antenna will be 2*(VCC–0.5V) e.g. 9V for Vcc=5V. This means that the maximum current that can be driven into the load is 1.7mA (peak–peak at the fundamental) and the external power control resistor should be set accordingly.

If it is necessary to drive more power into the antenna a possible way to accomplish this is to perform an impedance transformation to the antenna.

The antenna also acts as a filter on unwanted harmonic spurii. The use of a balanced output suppresses the 2nd harmonic (and other even order harmonics). The 3rd harmonic of the fundamental is not automatically suppressed. However even a Q as low as 10 will reduce the 3rd harmonic by a further 32dB relative to the fundamental.

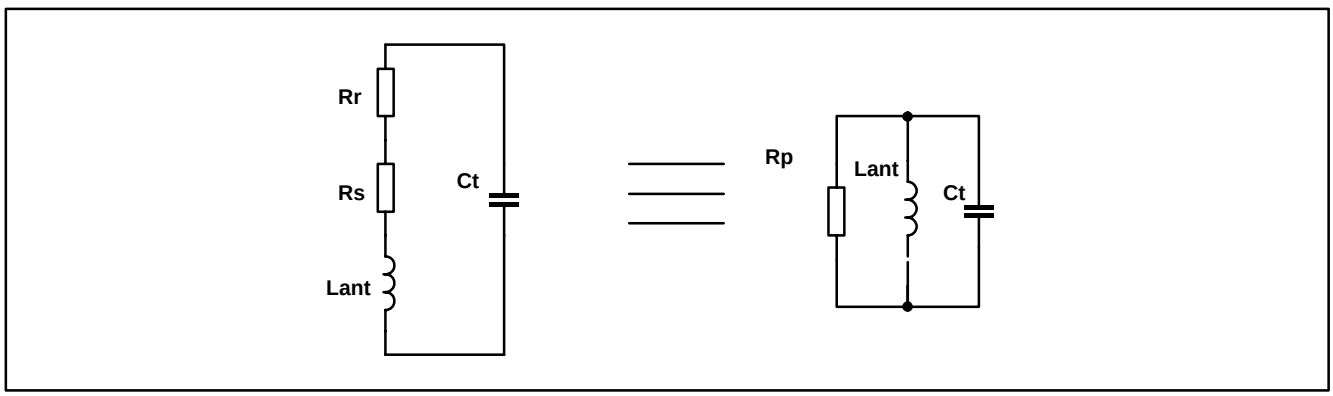


Figure 5 - loop antenna

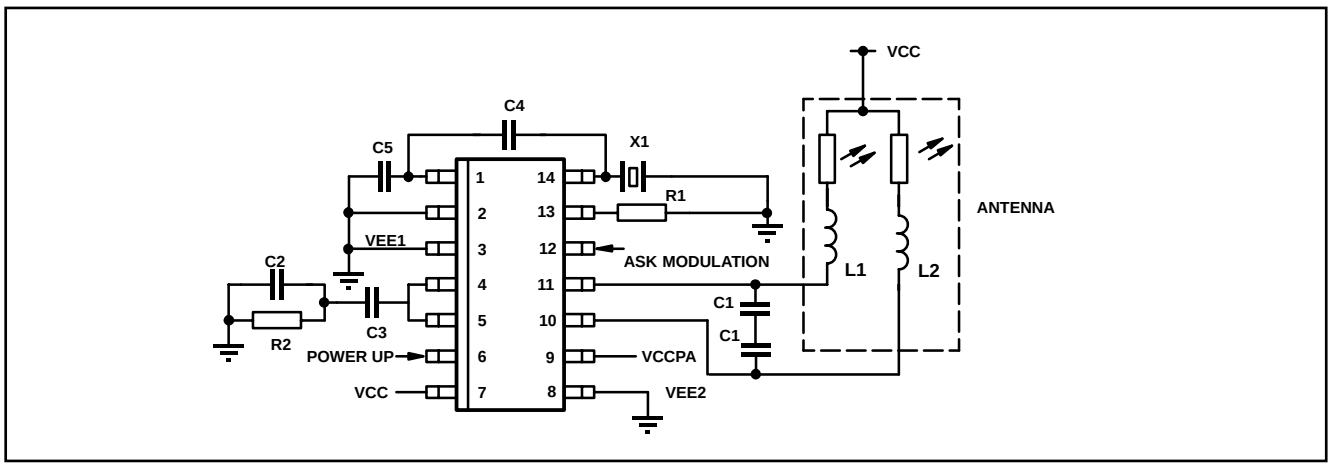


Figure 6 - Application diagram

Note: The above application diagram is provided to assist the customer in using the IC and no guarantee can be made to its correctness.

Component List at 315MHz

COMPONENTS	FUNCTION	VALUE	UNITS
R1	OUTPUT POWER CONTROL	2.0	kΩ
R2	PLL LOOP FILTER	4.7	kΩ
C1 and C1	ANTENNA TUNING	APPLICATION DEPENDENT	pF
L1 / L2	ANTENNA TUNING	APPLICATION DEPENDENT	nH
C2	PLL LOOP FILTER	220	pF
C3	PLL LOOP FILTER	10	nF
X1	PARALLEL RESONANT CRYSTAL	4.92	MHz
C4	CRYSTAL OSCILLATOR	18	pF
C5	CRYSTAL OSCILLATOR	18	pF

Note: The value of C1 is split between two capacitors to aid in balancing the antenna loop reducing the level of the second harmonic.

TESTABILITY REQUIREMENTS

This section is a summary of the observability and controllability requirements identified to simplify the production test requirements of the device.

1. Ability to directly drive crystal oscillator from the tester (no Crystal). The XTAL2 pin allows direct drive of the oscillator with an external clock source as shown in Fig. 7. Typically a 200mVpk clock signal is AC coupled to produce differential output on OP and OPb to the PFB (C=10nF, R s (Source) <5Ω)

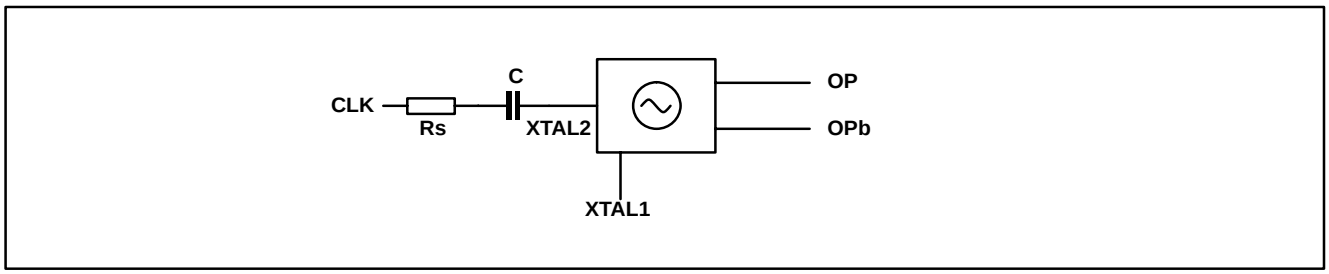
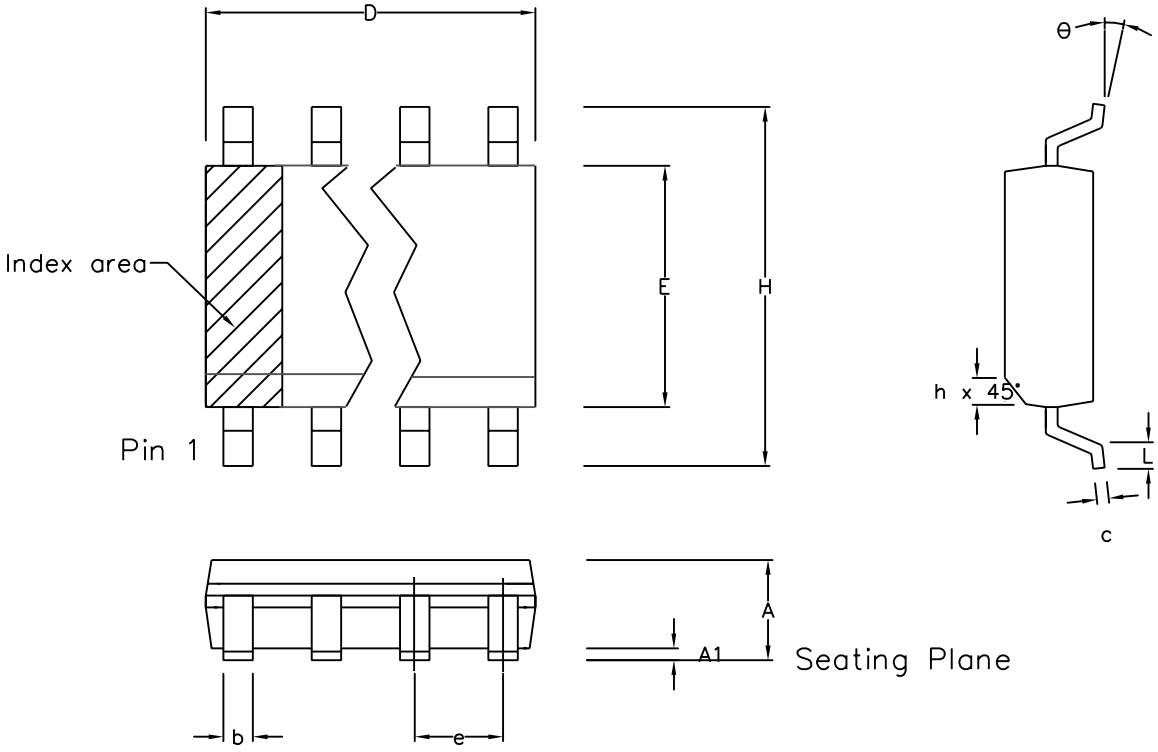


Figure 7 - Direct drive of crystal oscillator

2. Control of the VCO frequency is obtained via the LF1 signal pin. The output of the dividers is tested by measuring the DC current output of the charge pump (with XTAL2 held at V CC).

3. DC operation of the power amplifier is observed by measuring the current through the open collector outputs OUT and OUTB. The VCO input to the power amplifier is disabled with VCOTST tied to V_{CC} and the bias current being measured with DATA tied to V_{CC}. Toggling DATA input will modulate the bias current in the power amplifier.



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes
MP / S

Package Code DC

Package Outline for
14 lead SOIC
(0.150" Body Width)

GPD00011



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