DATEL®
A SUBSIDIARY OF C&D TECHNOLOGIES

ADS-953
18-Bit, 1MHz, Low-Distortion Sampling A/D Converters

FEATURES

- **18-bit resolution**
- **1MHz minimum sampling rate**
- **No missing codes over extended temperature range**
- **Very low power, 1.45 Watts**
- **Small, 32-pin, side-brazed, ceramic TDIP**
- **Edge-triggered**
- **Excellent performance, –95dB peak harmonics**
- **Ideal for both time and frequency-domain applications**
- **Low cost**

GENERAL DESCRIPTION

The ADS-953 is an 18-bit, 1MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. This feature, combined with excellent signal-to-noise ratio (SNR) and –95dB peak harmonic distortion (THD), makes the ADS-953 the ideal choice for both time-domain (medical imaging, scanners, process control) and frequency-domain (radar, telecommunications, spectrum analysis) applications.

Packaged in a 32-pin, side-brazed, metal-sealed, ceramic TDIP, the functionally complete ADS-953 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL, and the ADS-953 only requires the rising edge of the start convert pulse to operate.

Requiring ±15V and ±5V supplies, the ADS-953 typically dissipates 1.45 Watts. The device is offered with a bipolar (±5V) analog input range. Models are available for use in either commercial (0 to +70°C) or extended (–40 to +110°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 2	32	BIT 3
2	BIT 1 (MSB)	31	BIT 4
3	ANALOG GROUND	30	BIT 5
4	ANALOG INPUT	29	BIT 6
5	+5V REFERENCE OUT	28	BIT 7
6	GAIN ADJUST	27	BIT 8
7	COMPENSATION	26	BIT 9
8	–15V SUPPLY	25	BIT 10
9	+15V SUPPLY	24	BIT 11
10	+5V ANALOG SUPPLY	23	BIT 12
11	–5V ANALOG SUPPLY	22	BIT 13
12	ANALOG GROUND	21	BIT 14
13	DIGITAL GROUND	20	BIT 15
14	+5V DIGITAL SUPPLY	19	BIT 16
15	$\overline{EOC}$	18	BIT 17
16	START CONVERT	17	BIT 18 (LSB)

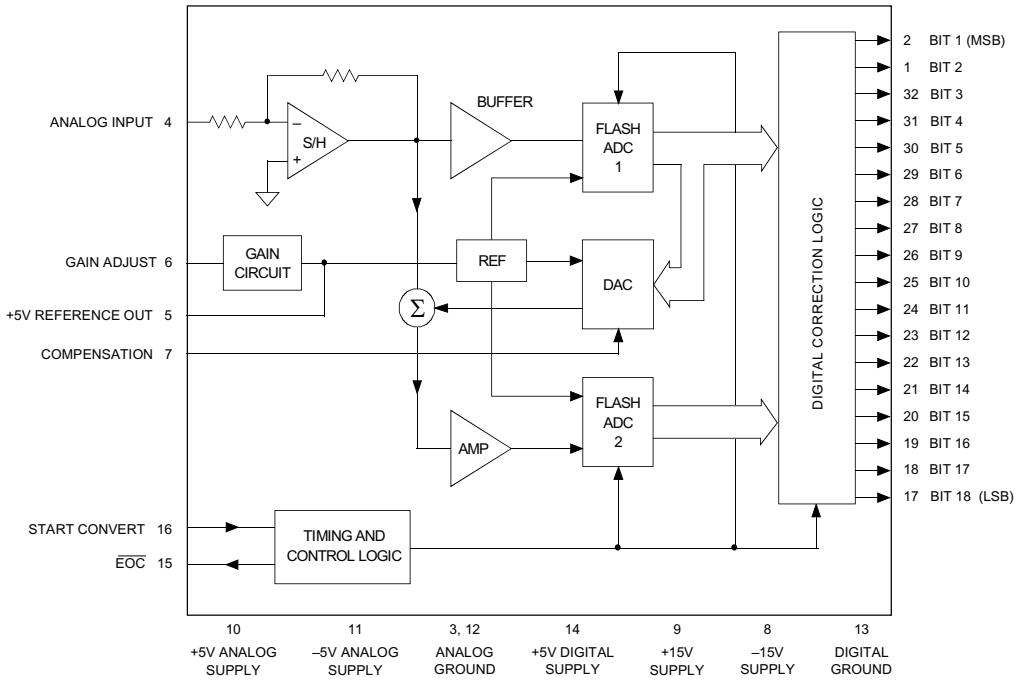


Figure 1. ADS-953 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 9)	0 to +16	Volts
–15V Supply (Pin 8)	0 to –16	Volts
+5V Supply (Pins 10, 14)	0 to +6	Volts
–5V Supply (Pin 11)	0 to –6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 4)	±15	Volts
Lead Temperature (10 seconds)	+300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-953MC	**0**	**—**	**+70**	**°C**
ADS-953ME	**–40**	**—**	**+110**	**°C**
Thermal Impedance				
θjc	—	5	—	°C/Watt
θca	—	22	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin,side-brazed, metal-sealed, ceramic TDIP			
Weight	0.46 ounces (13 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, ±V_{DD} = ±5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–40 to +110°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±5	—	—	±5	—	—	±5	—	Volts
Input Resistance	—	500	—	—	500	—	—	500	—	Ω
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUT										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	20	500	—	20	500	—	20	500	—	ns
STATIC PERFORMANCE										
Resolution	—	18	—	—	18	—	—	18	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±10	—	—	±10	—	—	±15	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1	–0.95	±0.5	+1	–0.95	±0.50	+1.25	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.25	—	±0.25	±0.4	—	±0.4	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.25	—	±0.25	±0.5	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.3	—	±0.3	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.25	—	±0.25	±0.4	—	±0.4	±0.9	%
No Missing Codes (f_{in} = 10kHz)	18	—	—	18	—	—	18	—	—	Bits
DYNAMIC PERFORMANCE (500kHz Sampling Rate)										
Peak Harmonics (–0.5dB)										
dc to 1kHz	—	–95	–93	—	–95	–93	—	–82	—	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–85	–80	—	–85	–80	—	–81	—	dB
Signal-to-Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 100kHz	91	93	—	91	93	—	—	92	—	dB
Signal-to-Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 100kHz	76	84	—	76	84	—	—	80	—	dB
DC Noise	—	76	—	—	76	—	—	76	—	µVrms
Two-Tone Intermodulation										
Distortion (f_{in} = 100kHz,										
240kHz, f_s = 500kHz, –0.5dB)	—	–85	—	—	–85	—	—	–81	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Large Signal (–0.5dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	TBD	—	—	TBD	—	—	TBD	—	V/µs
Aperture Delay Time	—	+20	—	—	+20	—	—	+20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time										
(to ±0.003%FSR, 10V step)	—	260	—	—	260	—	—	260	—	ns
Overvoltage Recovery Time ⑤	—	500	—	—	500	—	—	500	—	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–40 to +110°C MIN.	–40 to +110°C TYP.	–40 to +110°C MAX.	UNITS
Internal Reference										
Voltage	+4.95	+5.0	+5.05	+4.95	+5.0	+5.05	+4.95	+5.0	+5.05	Volts
Drift	—	±30	—	—	±30	—	—	±30	—	ppm/°C
External Current	—	1	—	—	1	—	—	1	—	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Complementary Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	Volts
Power Supply Currents										
+15V Supply	—	+29	—	—	+29	—	—	+29	—	mA
–15V Supply	—	–15	—	—	–15	—	—	–15	—	mA
+5V Supply	—	+104	—	—	+104	—	—	+104	—	mA
–5V Supply	—	–54	—	—	–54	—	—	–54	—	mA
Power Dissipation	—	1.45	1.65	—	1.45	1.65	—	1.45	1.65	Watts
Power Supply Rejection	—	—	±0.05	—	—	±0.05	—	—	±0.05	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for other input voltage ranges.

③ A 1MHz clock with a 500nsec positive pulse width (50% duty cycle) is used for all production testing. Any duty cycle may be used as long as a minimum positive pulse width of 20nsec is maintained. For applications requiring lower sampling rates, clock frequencies lower than 1MHz may be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-953 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are not connected to each other internally. For optimal performance, tie all ground pins (3, 12 and 13) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +5V REFERENCE OUTPUT (pin 5) to ground with 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. Tie a 47µF capacitor between COMPENSATION (pin 7) and ground.

2. The ADS-953 achieves its specified accuracies without the need for external calibration. If required, the device's small initial errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain. Float pin 6 if not using gain adjust circuits.

3. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") will initiate a new and probably inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –40 to +110°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

CALIBRATION PROCEDURE

Connect the converter per Table 1 for the appropriate input voltage range. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuits in Figure 2 are guaranteed to compensate for the ADS-953's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-953, offset adjusting is normally accomplished when the analog input is 0 minus ½LSB (–19µV). See Table 2 for the proper bipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1½LSB's (–4.999943V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so that the converter is continuously converting.
2. For bipolar zero/offset adjust, apply –19µV to the ANALOG INPUT (pin 4).
3. Adjust the offset potentiometer until the output code flickers equally between 01 1111 1111 1111 1111 and 10 0000 0000 0000 0000.

Gain Adjust Procedure

1. Apply –4.999943V to the ANALOG INPUT (pin 4).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2.

Table 1. Input Connections

INPUT VOLTAGE RANGE	ZERO ADJUST (–½ LSB)	GAIN ADJUST (–FS +1½ LSB)
±5V	–19µV	–4.999943

Table 2. Output Coding

COMPLEMENTARY OFFSET BINARY			
BIPLOAR SCALE	INPUT VOLTAGE ±5V	OUTPUT CODING MSB	LSB
+FS –1 LSB	+4.999962	00 0000 0000 0000 0000	
+3/4 FS	+3.750000	00 0111 1111 1111 1111	
+1/2 FS	+2.500000	00 1111 1111 1111 1111	
0	+0.000000	01 1111 1111 1111 1111	
–1/2 FS	–2.500000	10 1111 1111 1111 1111	
–3/4 FS	–3.750000	11 0111 1111 1111 1111	
–FS +1 LSB	–4.999962	11 1111 1111 1111 1110	
–FS	–5.000000	11 1111 1111 1111 1111	

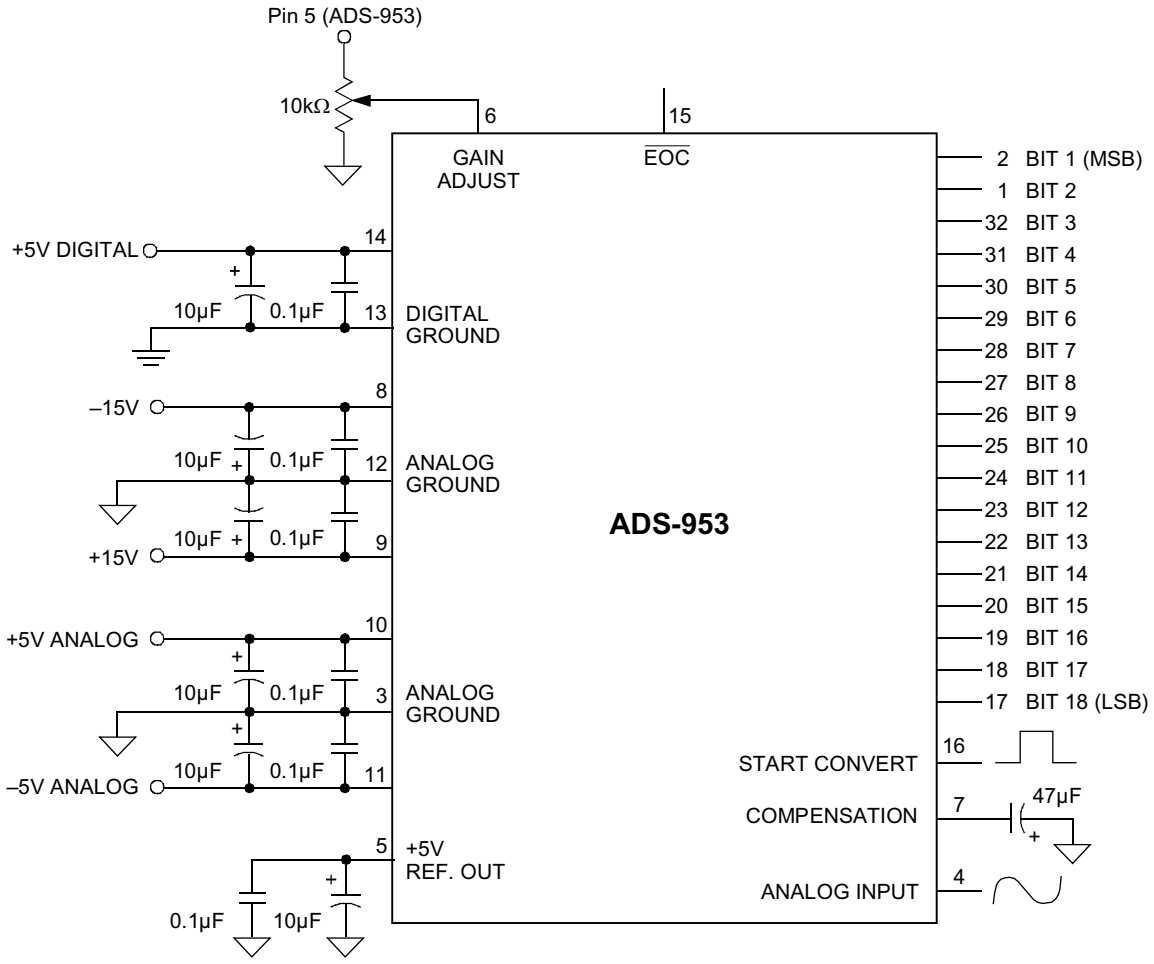
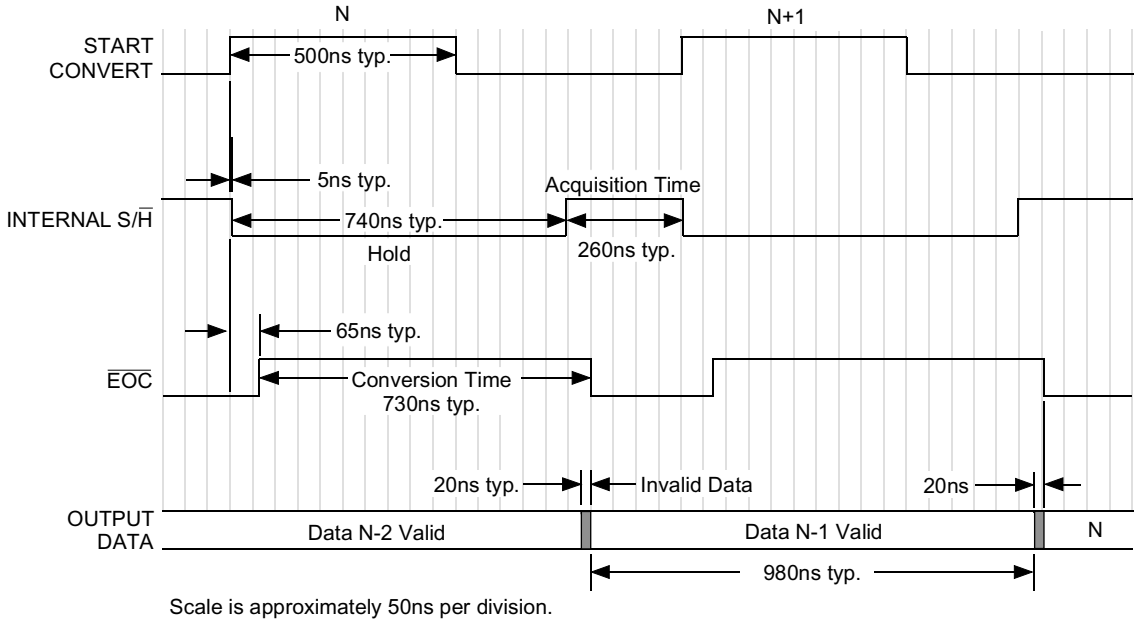


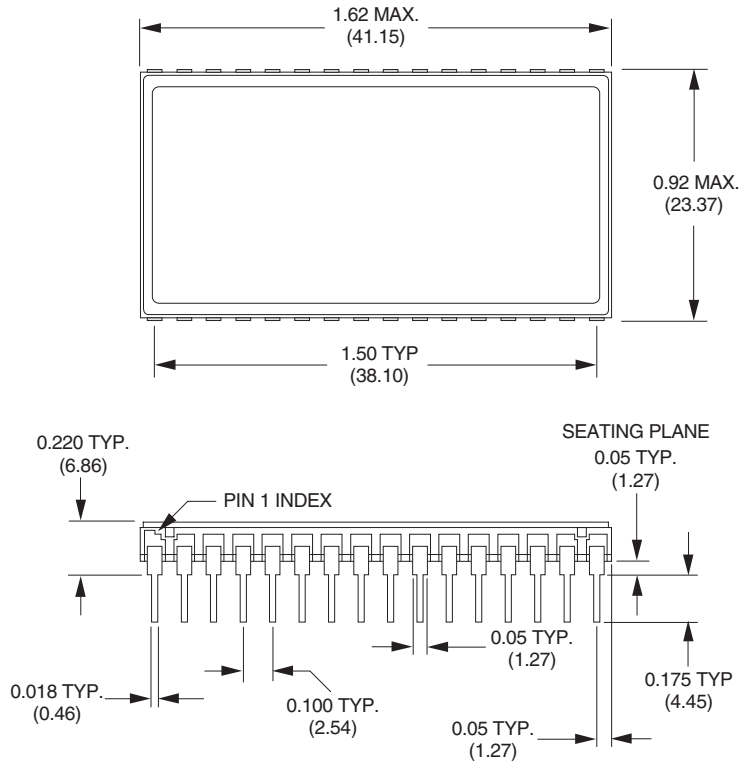
Figure 2. Typical ADS-953 Connection Diagram



Scale is approximately 50ns per division.

Figure 3. ADS-953 Timing Diagram

MECHANICAL DIMENSIONS INCHES (mm)



Dimension Tolerances
(unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar Alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	32-PIN PACKAGE
ADS-953MC	0 to +70°C	TDIP
ADS-953ME	–40 to +110°C	TDIP

ACCESSORIES

ADS-B951 * Evaluation Board (without ADS-951)

Receptacles for PC board mounting can be ordered through AMP, Inc., Part # 3-331272-8 (Component Lead Socket), 32 required. For availability of MIL-STD-883 product, contact DATEL.

*** NOTE** The ADS-951 evalution board is used for the AD-953, as the ADS-951 and ADS-953, share a common pinout

A SUBSIDIARY OF C&D TECHNOLOGIES

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1151
Tel: (508) 339-3000 (800) 233-2765 Fax: (508) 339-6356
Internet: www.datel.com E-mail: sales@datel.com

ISO 9001 REGISTERED

DS-0541 3/05

DATEL (UK) LTD. Tadley, England Tel: (01256)-880444
Internet: www.datel-europe.com E-mail: datel.ltd@datel.com

DATEL S.A.R.L. Montigny Le Bretonneux, France Tel: 01-34-60-01-01
Internet: www.datel-europe.com E-mail: datel.sarl@datel.com

DATEL GmbH München, Germany Tel: 89-544334-0
Internet: www.datel-europe.com E-mail: datel.gmbh@datel.com

DATEL KK Tokyo, Japan Tel: 3-3779-1031, Osaka Tel: 6-6354-2025
Internet: www.datel-co.jp E-mail: salestko@datel.co.jp, salesosa@datel.co.jp

DATEL China Shanghai, China Tel: 011-86-51317131
E-mail: davidx@datel.com