élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2423/EL2423C

Quad De-Compensated High Speed Operational Amplifier

Features

- Stable for gains > 10
- Wide bandwidth—500 MHz
- High slew rate—350 V/μs
- Wide supply range— ±5V to ±15V
- Output short circuit protected
- Low supply current—4 mA per amplifier

Applications

- High frequency active filters
- Video amplifiers
- Pulse amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline*
EL2423CJ	0°C to +75°C	CerDIP	MDP0010
EL2423CN	0°C to +75°C	P-DIP	MDP0006
EL2423J	−55°C to +125°C	CerDIP	MDP0010
EL2423J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2423L/883B	−55°C to +125°C	LCC	MDP0007
EL2423CM	0°C to +75°C	SOL	MDP0027

*See 1990 Databook for package outlines.

General Description

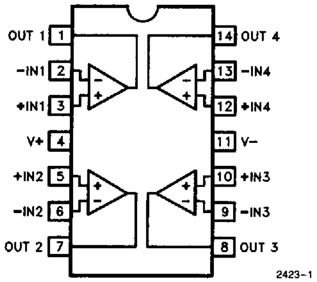
The EL2423 monolithic quad operational amplifier is an example of Elantec's commitment to high speed low power consumption products. This amplifier is stable for gains of 10 or greater, exhibits Slew Rates of 350V per microsecond, and a Gain Bandwidth of 500 MHz while drawing supply currents of 4 mA per amplifier. The output provides short circuit protection but is capable of delivering currents in excess of 50 mA. The device is manufactured using Elantec's advanced Complementary Bipolar process.

The EL2423 is available in 14-lead Plastic DIP, 14-lead CerDIP, 20-pad LCC, and 20-pad SOL.

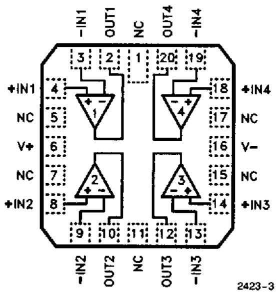
Elantec's products and facilities comply with MIL-STD-883, Revision C, MIL-I-45082A, and other applicable quality assurance specifications. For information on Elantec's Military processing, see QRA-2, "*Elantec's Military Processing, Monolithic Integrated Circuits*". For information on Elantec's Commercial processing, see QRA-1, "*Summary of Elantec's Reliability and Quality Assurance Policy*".

Connection Diagrams

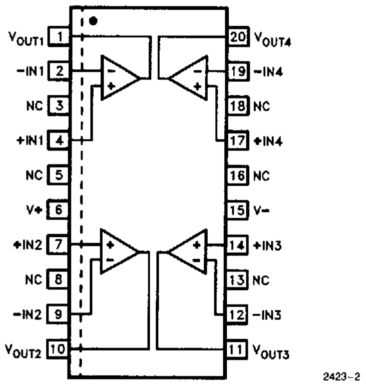
EL2423J/CN



EL2423L



EL2423CM



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Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V
Differential Input Voltage	6V
Peak Output Current	Short Circuit Protected
Output Short Circuit Duration (Note 1)	Continuous
Internal Power Dissipation	See Curves
Operating Temperature Range	
EL2423	−55°C to +125°C
EL2423C	0°C to +75°C
Storage Temperature Range	−65°C to 150°C
Maximum Junction Temperature	
CerDIP, LCC	175°C
Plastic DIP, SOL	150°C
Lead Temperature	
DIP Package	300°C
SOL Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	25°C		1.0	6	I		1.0	6	I	mV
		Full			10	I			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		10		V		10		V	µV/°C
I_B	Bias Current	25°C		1.0	4	I		1.0	4	I	µA
		Full			6	I			6	III	µA
I_{OS}	Offset Current	25°C		0.5	2	I		0.5	2	I	µA
		Full			3	I			3	III	µA
R_{IN}	Input Resistance	25°C		20		V		20		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±11		I	±10	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		7		V		7		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	25°C	20k	40k		I	20k	40k		I	V/V
		Full	10k			I	10k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	80		I	70	80		II	dB

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Quad De-Compensated High Speed Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	Full	±11	±12		I	±11	±12		II	V
I_{SC}	Short Circuit Current	25°C	±10	+50	±85	I	±10	±50	±85	I	mA
R_O	Output Resistance	25°C		40		V		40		V	Ω
I_S	Supply Current	Full		16	18	I		16	18	II	mA
PSRR	Power Supply Rejection Ration (Note 5)	Full	70	80		I	70	80		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified

Parameter	Description	Temp	EL2423				EL2423C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		200		V		200		V	MHz
FPBW	Full Power Bandwidth (Note 7)	25°C	3.48	5.5		I	4.7	5.5		I	MHz
t_r	Rise Time (Note 6)	25°C		7		V		7		V	ns
OS	Overshoot (Note 6)	25°C		20		V		20		V	%
SR	Slew Rate (Note 6)	25°C	250	350		I	250	350		I	V/µs
t_s	Settling Time (Note 9) 10V Step to 0.05%	25°C		330		V		330		V	ns
CHSp	Channel Separation f = 1 MHz	25°C		65		V		65		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: $V_O = \pm 10V$.
Note 3: $R_L = 2k\Omega$.
Note 4: Two tests are performed. $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: $V_O = 100$ mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/$2\pi\ V_{peak}$.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurements are made with techniques in the following reference: "*Take The Guesswork Out of Settling-Time Measurements,*" EDN September 19, 1985.

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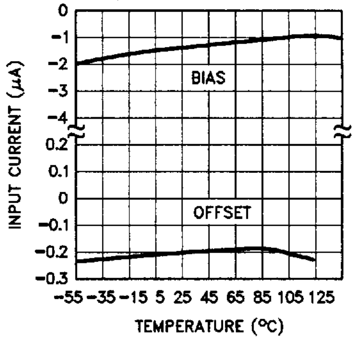
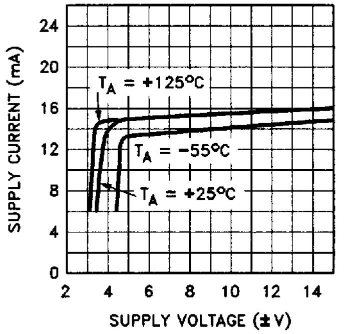
Quad De-Compensated High Speed Operational Amplifier

Typical Performance Curves

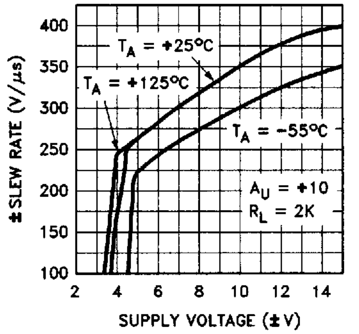
Input Current vs Temperature (2 Typical Units)



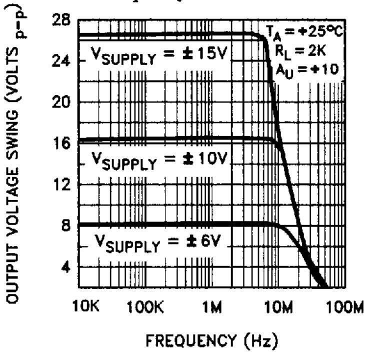
Supply Current vs Supply Voltage



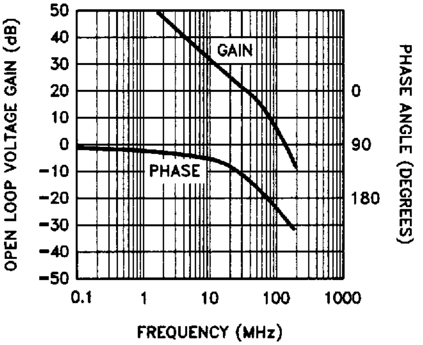
Slew Rate vs Supply Voltage



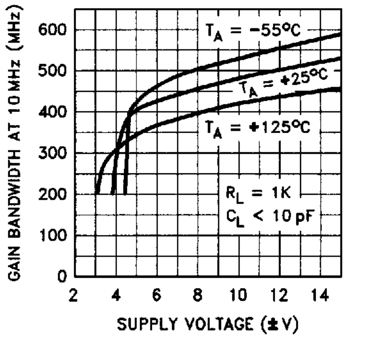
Output Voltage Swing vs Frequency



Open Loop Voltage Gain vs Frequency



Gain Bandwidth at 10 MHz vs Supply Voltage



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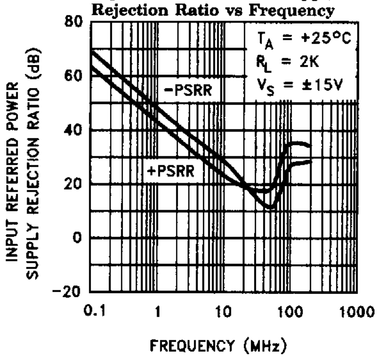
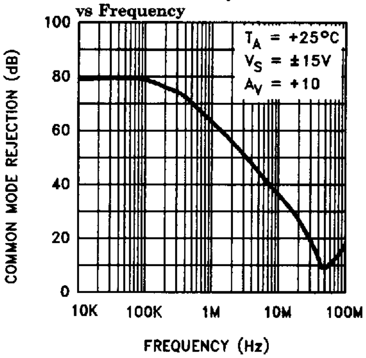
Typical Performance Curves — Contd.

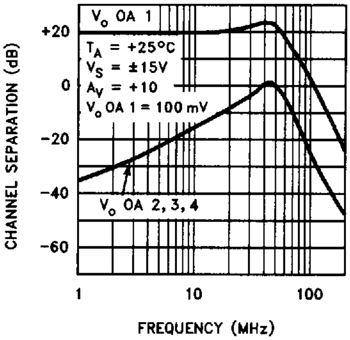
Input Referred Power Supply Rejection Ratio vs Frequency



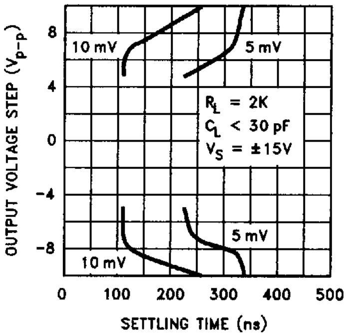
Common Mode Rejection vs Frequency



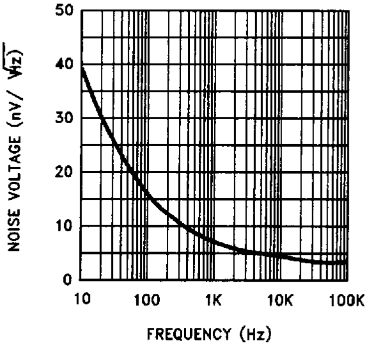
Channel Separation vs Frequency



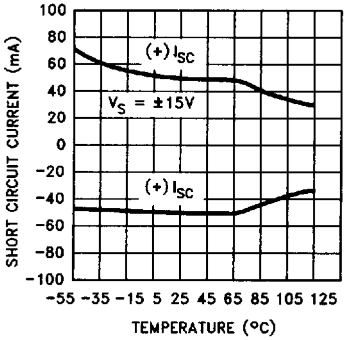
Settling Time A_V = +10



Noise Voltage vs Frequency



Short Circuit Current vs Temperature



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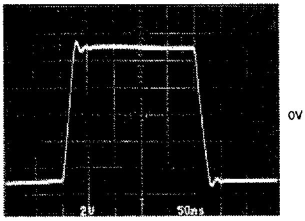
Typical Performance Curves — Contd.

Large Signal Response



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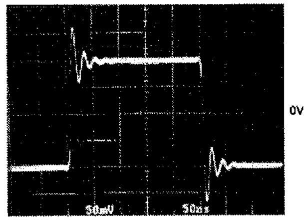
A_V = +10
V_{IN} = ±0.5V
V_O = ±5V
R_L = 2k

Small Signal Response



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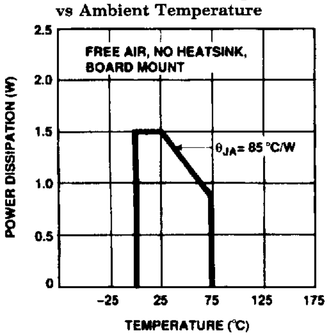
A_V = +10
V_{IN} = ±10 mV
V_O = ±100 mV
R_L = 2k

20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



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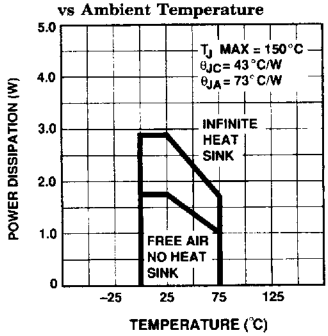
14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



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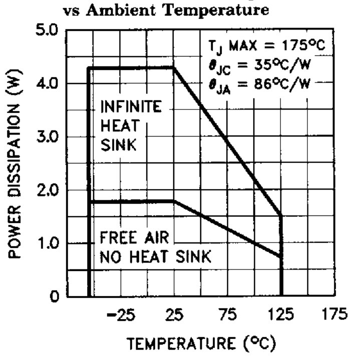
14-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



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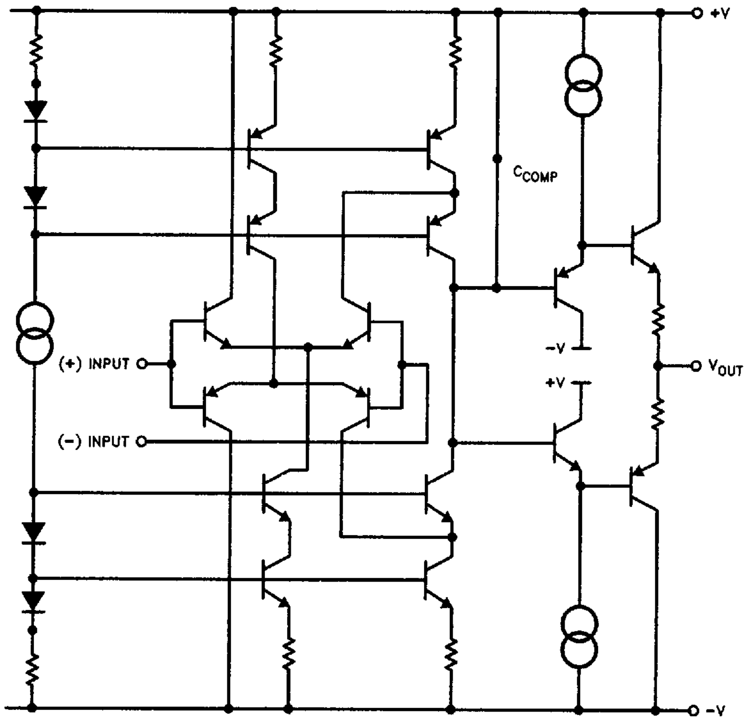
Simplified Schematic (One Amplifier)



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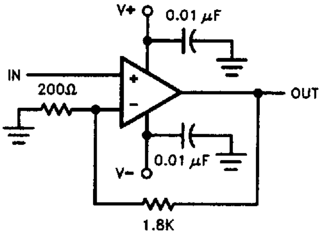
Test Circuit



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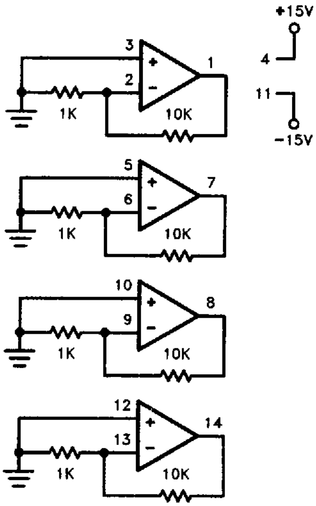
Pin numbers indicated are for the 14-lead DIP. Circuit is identical for all package types.

Burn In Circuit



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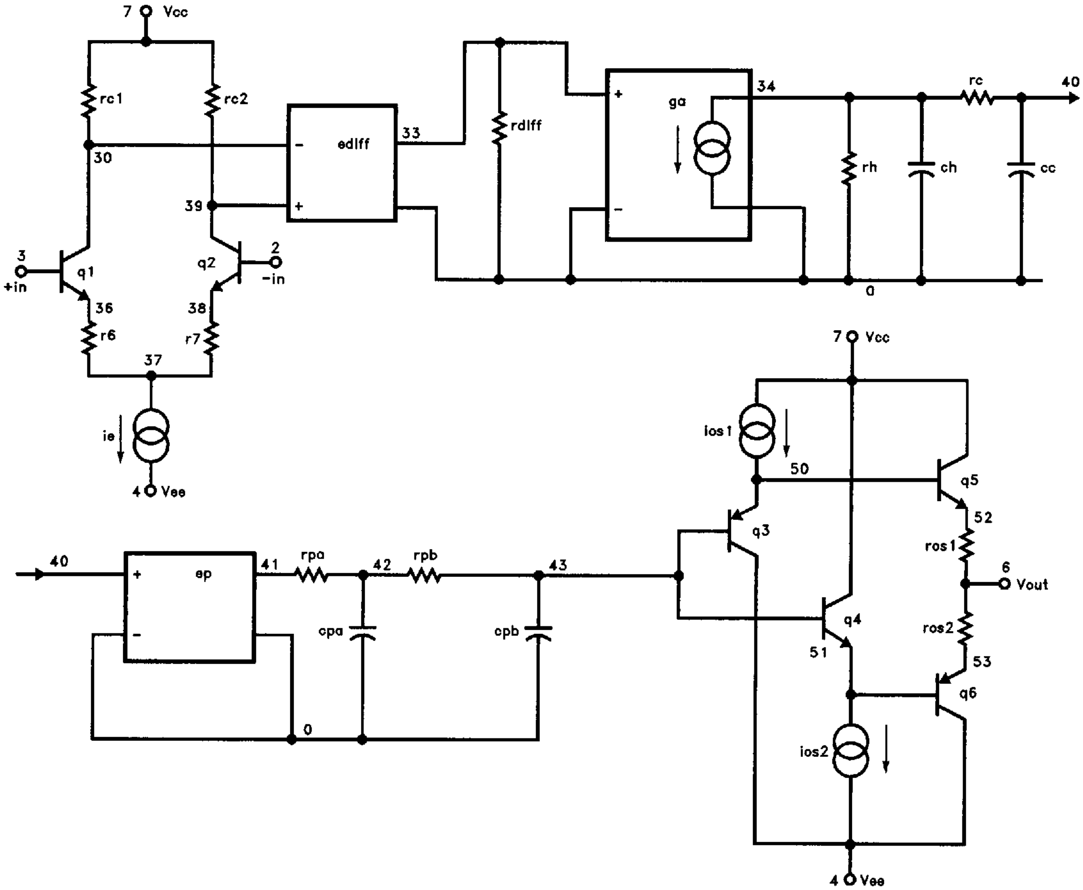
EL2423 Macromodel

```
* Connections:   +input
*                 |    -input
*                 |     |    +Vsupply
*                 |     |     |    -Vsupply
*                 |     |     |     |    output
*                 |     |     |     |     |
.subckt M2423     3     2     7     4     6
* Input stage
ie 37 4 2mA
r6 36 37 60
r7 38 37 60
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 2.6m
rh 34 0 3Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 25pF
rpb 42 43 50
cpb 43 0 15pF
* Output Stage
ios1 7 50 1.25mA
ios2 51 4 1.25mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn(is=800.0E-18 bf=250 tf=0.2nS)
.model qna npn(is=864E-18 bf=300 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2423 Macromodel — Contd.



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