

1. Overview

The M16C/28 group of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 64-pin and 80-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.2.1 lists performance outline of M16C/28 group 80-pin device.

Table 1.2.2 lists performance outline of M16C/28 group 64-pin device.

Table 1.2.1. Performance outline of M16C/28 group (80-pin device)

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port		71 lines
Multifunction timer		TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I ² C bus ¹ (option ³), or IE bus ² (option ³) 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I ² C bus ¹ (option ³))
A-D converter		10 bits x 24 channels
DMAC		2 channels (trigger: 31 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits <ul style="list-style-type: none"> • Main clock • Sub-clock • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer } (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator)
Voltage detection circuit		Present (option ³)
Power supply voltage		Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz) Vcc=3.0V to 5.5V (T-ver.) Vcc=4.2V to 5.5V (V-ver.)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option ³))
Power consumption		16mA (Vcc=5V, f(BCLK)=20MHz) 25 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz, when wait mode) 0.7 μA (Vcc=3V, when stop mode)
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option ³) (Normal-ver.) -40 to 85°C (T-ver.) -40 to 105°C / -40 to 125°C (V-ver.)
Package		80-pin plastic mold QFP

Notes:

1. I²C Bus is a registered trademark of PHILIPS.
2. IE Bus is a registered trademark of NEC.
3. If you desire this option, please so specify.

Table 1.2.2. Performance outline of M16C/28 group (64-pin device)

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (Normal-ver./T-ver.) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (Normal-ver.) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (V-ver.)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port		55 lines
Multifunction timer		TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I ² C bus ¹ (option ³), or IE bus ² (option ³) 1 channel (SI/O3) Clock synchronous 1 channel (Multi-Master I ² C bus ¹ (option ³))
A-D converter		10 bits x 13 channels
DMAC		2 channels (trigger: 30 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		24 internal and 8 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits <ul style="list-style-type: none"> • Main clock • Sub-clock • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator)
Voltage detection circuit		Present (option ³)
Power supply voltage		Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (Normal-ver.) Vcc=2.7V to 5.5V (f(BCLK)=10MHz) Vcc=3.0V to 5.5V (T-ver.) Vcc=4.2V to 5.5V (V-ver.)
Flash memory	Program/erase voltage	2.7V to 5.5V (Normal-ver.) 3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option ³))
Power consumption		16mA (Vcc=5V, f(BCLK)=20MHz) 25 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz, when wait mode) 0.7 μA (Vcc=3V, when stop mode)
Operating ambient temperature		-20 to 85°C / -40 to 85°C (option ³) (Normal-ver.) -40 to 85°C (T-ver.) -40 to 105°C / -40 to 125°C (V-ver.)
Package		64-pin plastic mold QFP

Notes:

1. I²C Bus is a registered trademark of PHILIPS.
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3. If you desire this option, please so specify.

1.3 Block Diagram

Figure 1.3.1 is a block diagram of the M16C/28 group, 80-pin device.

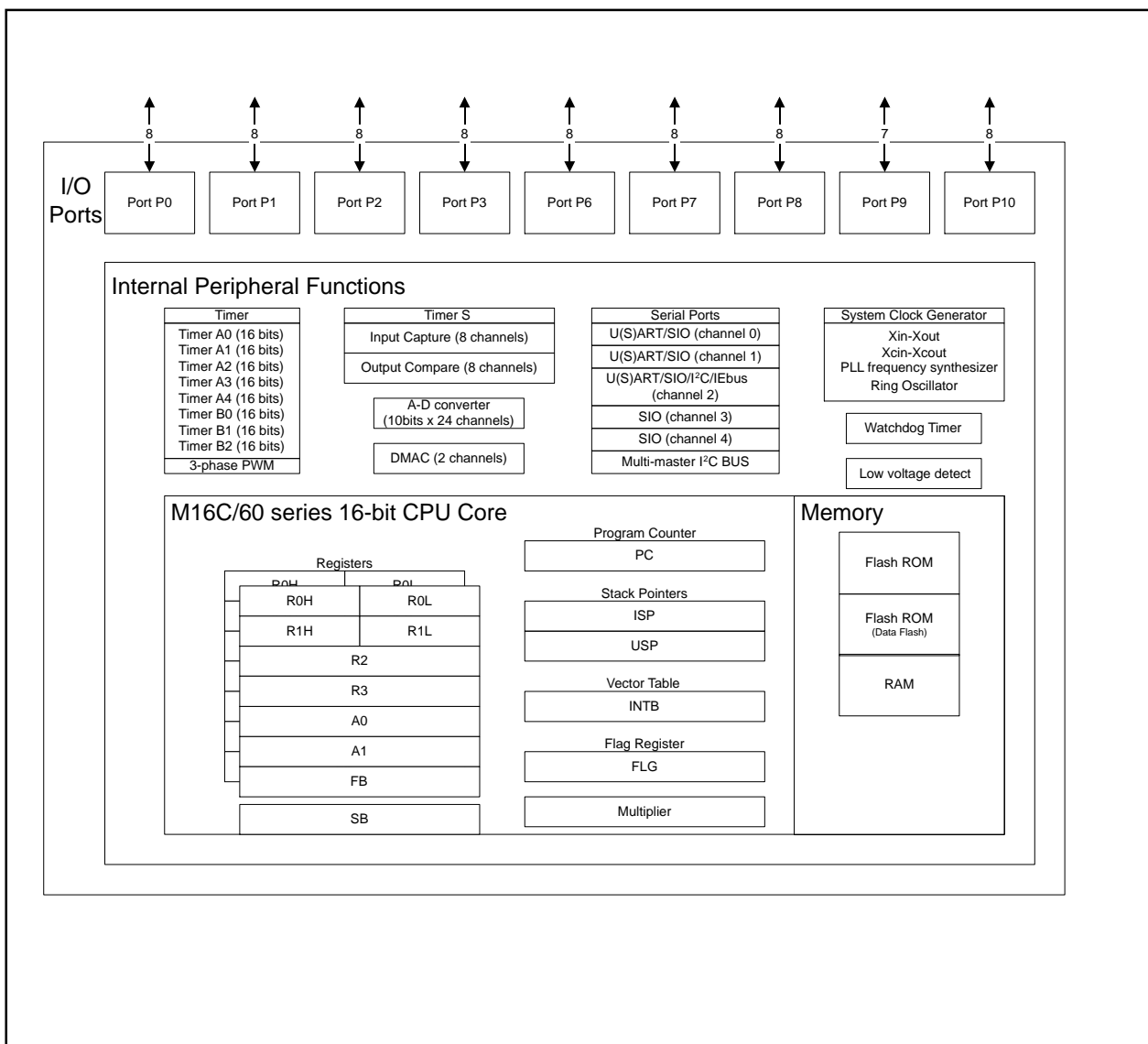


Figure 1.3.1. M16C/28 Group, 80-pin Block Diagram

Figure 1.3.2 is a block diagram of the M16C/28 group, 64-pin device.

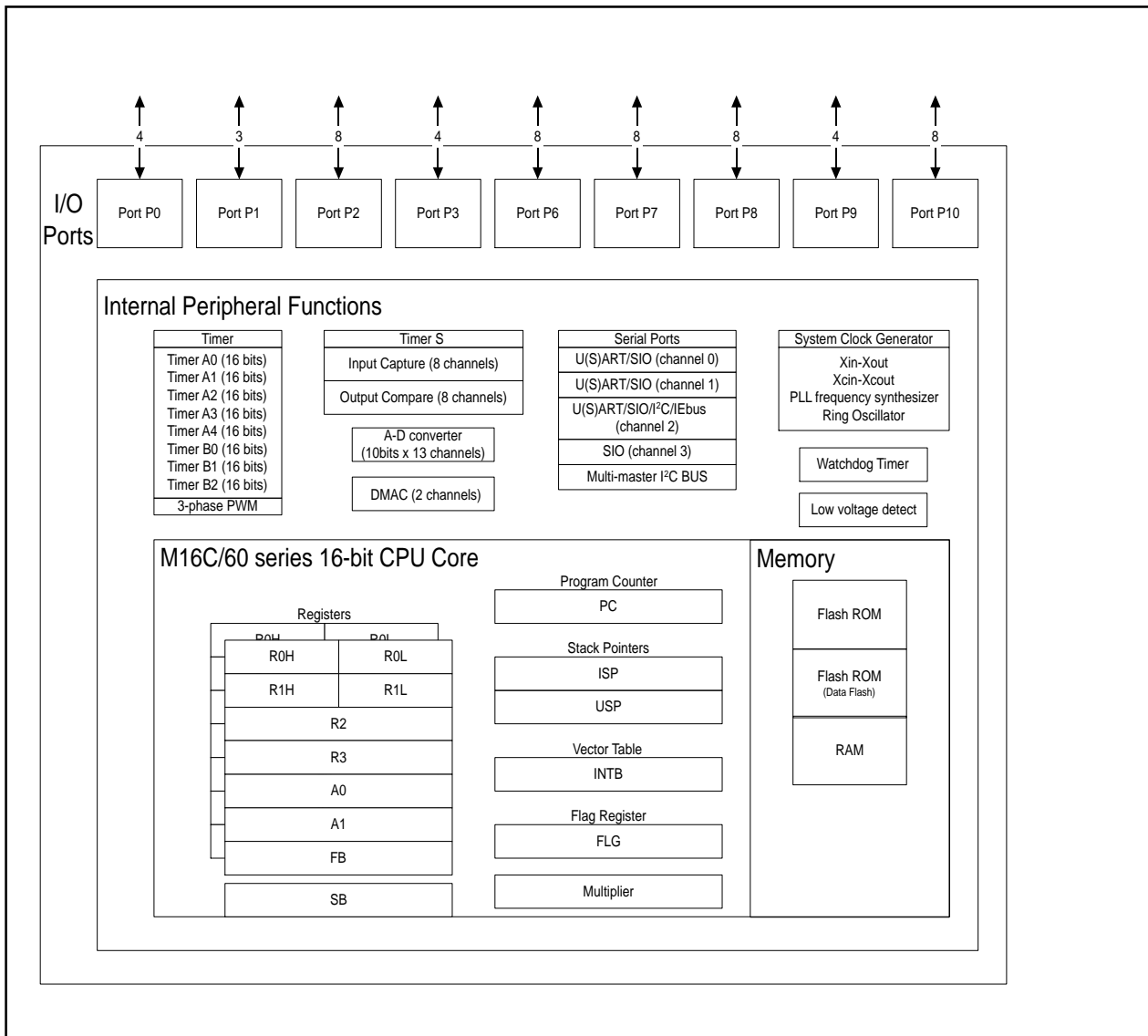


Figure 1.3.2. M16C/28 Group, 64-pin Block Diagram

1.4 Product List

Tables 1.4.1 to 1.4.3 list the M16C/28 group products and Figure 1.4.1 shows the type numbers, memory sizes and packages.

Table 1.4.1. Product List (1) -Normal Version

As of November 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30280F6HP **	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version
M30280F8HP **	64K + 4K byte	4K byte		
M30280FAHP **	96K + 4K byte	8K byte		
M30281F6HP **	48K + 4K byte	4K byte	64P6Q-A	
M30281F8HP **	64K + 4K byte	4K byte		
M30281FAHP **	96K + 4K byte	8K byte		
M30280M4-XXXHP *	32K byte	2K byte	80P6Q-A	Mask ROM Version
M30280M6-XXXHP *	48K byte	4K byte		
M30280M8-XXXHP *	64K byte	4K byte		
M30281M4-XXXHP *	32K byte	2K byte	64P6Q-A	
M30281M6-XXXHP *	48K byte	4K byte		
M30281M8-XXXHP *	64K byte	4K byte		

* : under planning

** : under development

Table 1.4.2. Product List (2) -T Version

As of November 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30280F6THP **	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version (T-version)
M30280F8THP **	64K + 4K byte	4K byte		
M30280FATHP **	96K + 4K byte	8K byte		
M30281F6THP **	48K + 4K byte	4K byte	64P6Q-A	
M30281F8THP **	64K + 4K byte	4K byte		
M30281FATHP **	96K + 4K byte	8K byte		
M30280M4T-XXXHP *	32K byte	2K byte	80P6Q-A	Mask ROM Version (T-version)
M30280M6T-XXXHP *	48K byte	4K byte		
M30280M8T-XXXHP *	64K byte	4K byte		
M30281M4T-XXXHP *	32K byte	2K byte	64P6Q-A	
M30281M6T-XXXHP *	48K byte	4K byte		
M30281M8T-XXXHP *	64K byte	4K byte		

* : under planning

** : under development

Table 1.4.2. Product List (3) -V Version

As of November 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30280F6VHP **	48K + 4K byte	4K byte	80P6Q-A	Flash ROM Version (V-version)
M30280F8VHP **	64K + 4K byte	4K byte		
M30280FAVHP **	96K + 4K byte	8K byte		
M30281F6VHP **	48K + 4K byte	4K byte	64P6Q-A	
M30281F8VHP **	64K + 4K byte	4K byte		
M30281FAVHP **	96K + 4K byte	8K byte		
M30280M4V-XXXHP *	32K byte	2K byte	80P6Q-A	Mask ROM Version (V-version)
M30280M6V-XXXHP *	48K byte	4K byte		
M30280M8V-XXXHP *	64K byte	4K byte		
M30281M4V-XXXHP *	32K byte	2K byte	64P6Q-A	
M30281M6V-XXXHP *	48K byte	4K byte		
M30281M8V-XXXHP *	64K byte	4K byte		

* : under planning

** : under development

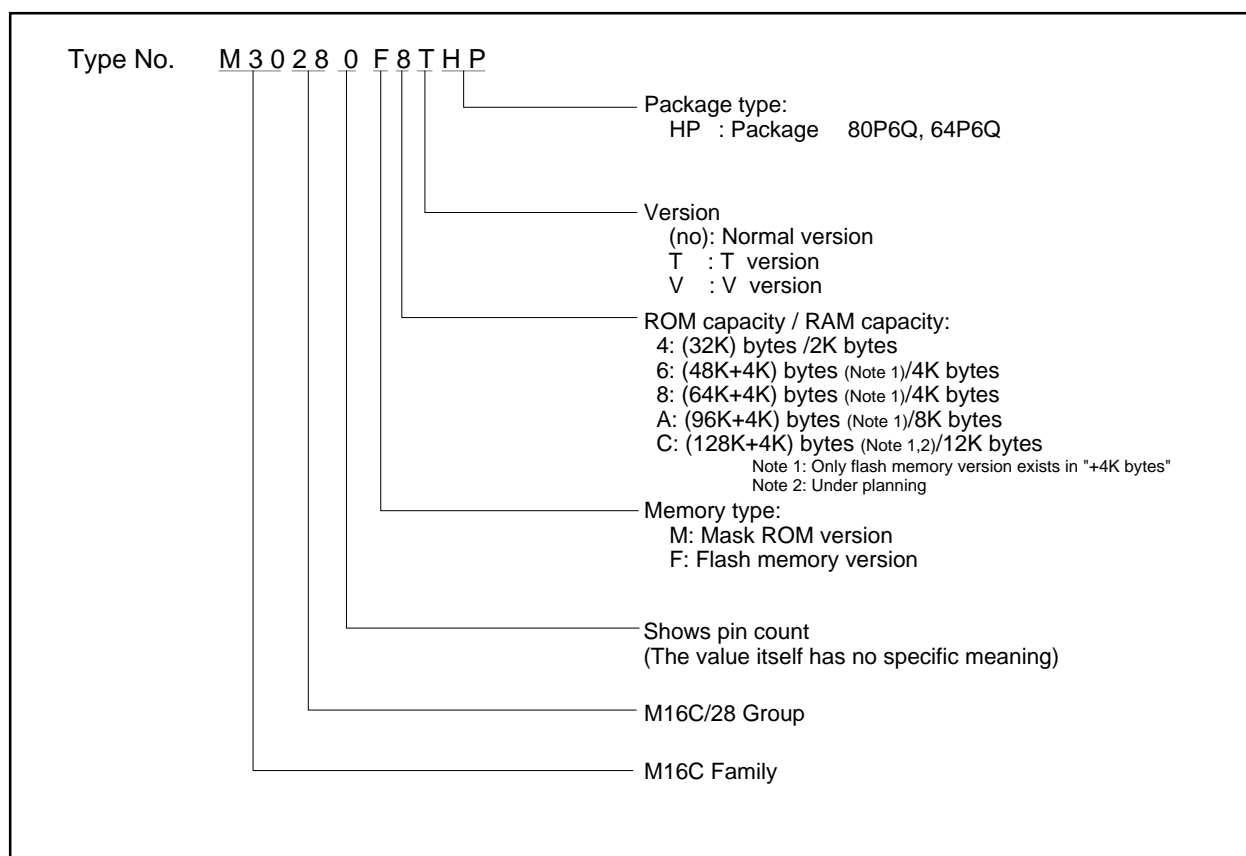


Figure 1.4.1. Type No., Memory Size, and Package

1.5 Pin Configuration

Figures 1.5.1 and 1.5.2 show the pin configurations (top view).

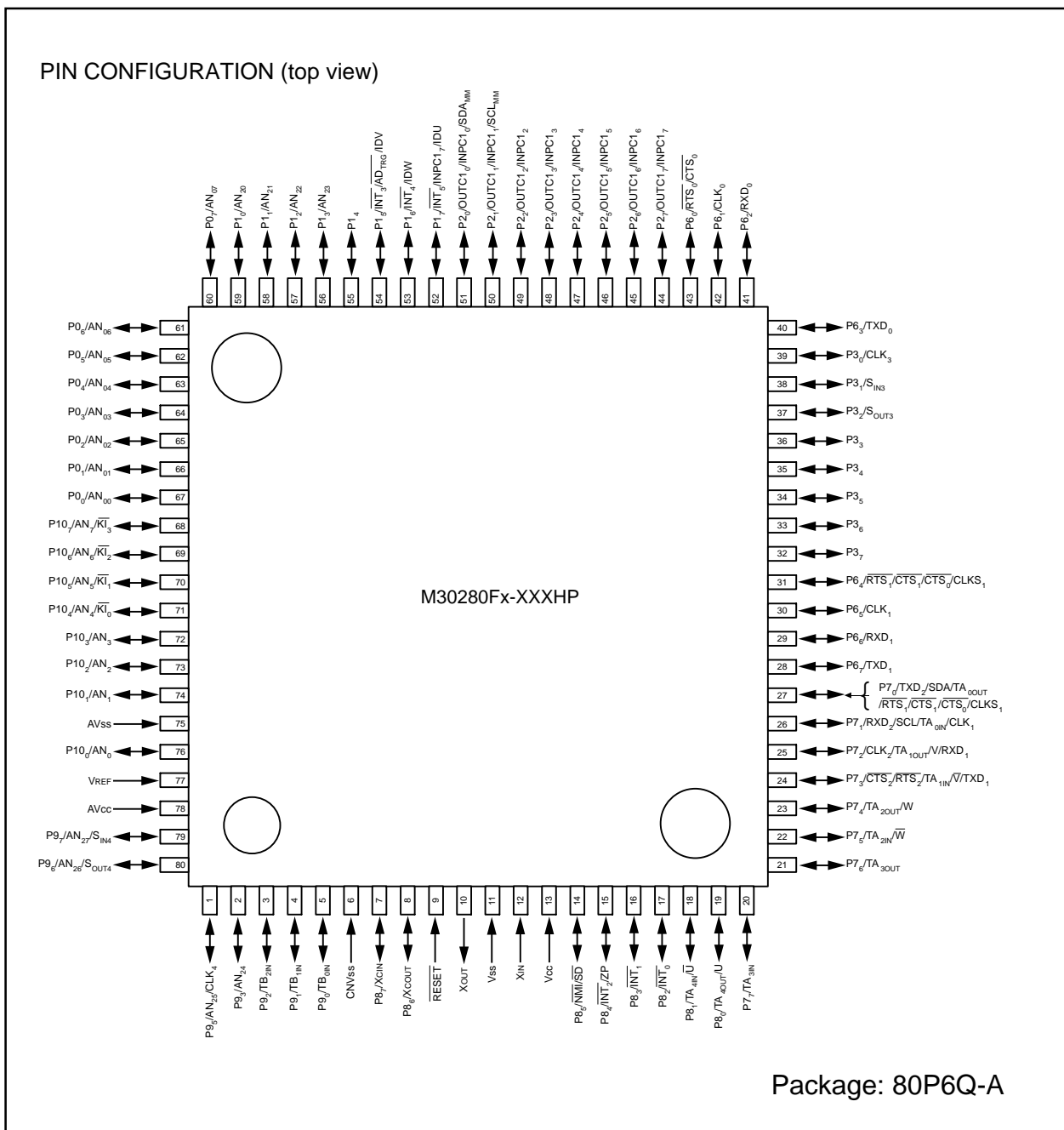


Figure 1.5.1. Pin Configuration (Top View) of M16C/28 Group, 80-pin Package

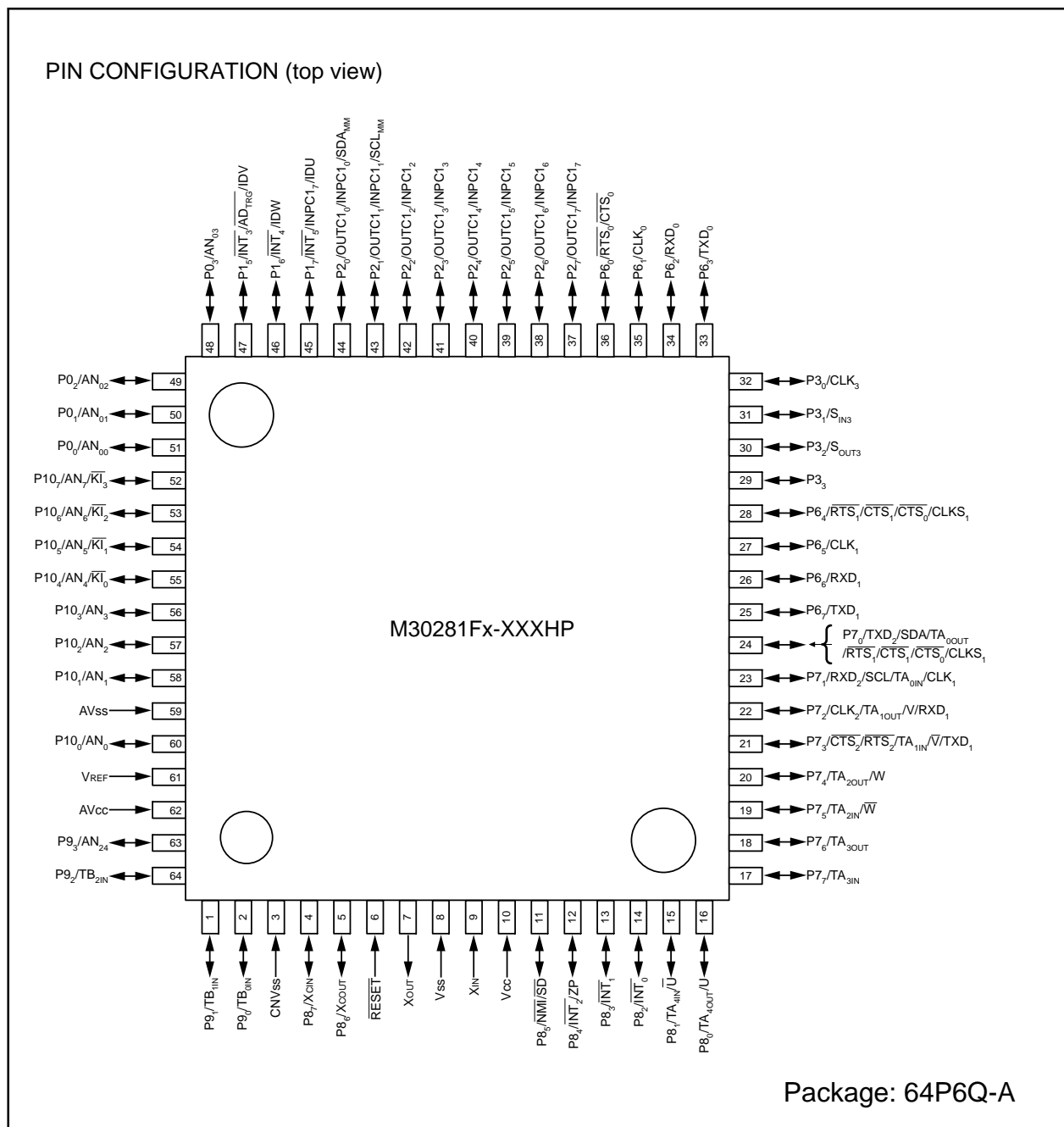


Figure 1.5.2. Pin Configuration (Top View) of M16C/28 Group, 64-pin Package

1.6 Pin Description

Table 1.6.1 and 1.6.2 describes the available pins.

Table 1.6.1 Pin Description(1)

Pin name	Signal name	I/O type	Function
V _{CC} , V _{SS}	Power supply input		Apply 0V to the V _{SS} pin, and the following voltage to the V _{CC} pin. 2.7 to 5.5V (Normal-ver.) 3.0 to 5.5V (T-ver.) 4.2 to 5.5V (V-ver.)
CNV _{SS}	CNV _{SS}	Input	Connect this pin to V _{SS} .
RESET	Reset input	Input	"L" on this input resets the microcomputer.
X _{IN} X _{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the X _{IN} and the X _{OUT} pins. To use an externally derived clock, input it to the X _{IN} pin and leave the X _{OUT} pin open. If X _{IN} is not used (for external oscillator or external clock) connect X _{IN} pin to V _{CC} and leave X _{OUT} pin open.
AV _{CC}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V _{CC} .
AV _{SS}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V _{SS} .
V _{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A-D converter.
P0 ₀ ~P0 ₇	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resistor option can be selected for the entire group of four pins. Software can also select this port to function as A-D converter input pins. P0 ₄ ~P0 ₇ is not in 64 pin version.
P1 ₀ ~P1 ₇	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. Additional software-selectable secondary functions are: 1) P1 ₀ to P1 ₃ can act as A-D converter input pins; 2) P1 ₅ to P1 ₇ can be configured as external interrupt pins; 3) P1 ₅ to P1 ₇ can be configured as position-data-retain function input pins, and; 4) P1 ₅ can input a trigger for the A-D converter. P1 ₀ ~P1 ₄ is not in 64 pin version.
P2 ₀ ~P2 ₇	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0. Software can also select this port to perform as I/O for the Timer S (all pins), and MultiMaster I ² C Bus (P2 ₀ and P2 ₁ only)
P3 ₀ ~P3 ₇	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0. P3 ₀ to P3 ₂ also function as SIO3 I/O, as selected by software. P3 ₄ ~P3 ₇ is not in 64 pin version.
P6 ₀ ~P6 ₇	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O, as selected by software.
P7 ₀ ~P7 ₇	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P0. P7 can also function as I/O for timer A0-A3, as selected by software. Additional programming options are: P7 ₀ to P7 ₃ can assume UART1 and UART2 I/O capabilities, and P7 ₂ to P7 ₅ can function as output pins for the three-phase motor control timer.

Table 1.6.2 Pin Description(2)

Pin name	Signal name	I/O type	Function
P8 ₀ ~P8 ₇	I/O port P8	Input/output	This is an 8-bit I/O port equivalent to P0. Additional software-selectable secondary functions are: 1) P8 ₀ and P8 ₁ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) P8 ₂ to P8 ₄ can be configured as external interrupt pins. P8 ₄ can be used for Timer A Zphase function; 3) P8 ₅ can be used as $\overline{\text{NMI/SD}}$. P8 ₅ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to P8 ₅ after setting the direction register for P8 ₅ to "0" when the three-phase motor control is enabled, and; 4) P8 ₆ and P8 ₇ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartz oscillator must be connected between P8 ₆ (X _{COU} T pin) and P8 ₇ (X _{CIN} pin).
P9 ₀ ~P9 ₃ , P9 ₅ ~P9 ₇	I/O port P9	Input/output	This is a 7-bit I/O port equivalent to P0. Additional software-selectable secondary functions are: 1) P9 ₀ to P9 ₂ can act as Timer B0~B2 input pins; 2) P9 ₃ , P9 ₅ to P9 ₇ can act as A-D converter input pins, and; 3) P9 ₆ to P9 ₇ can assume SI/O4 I/O. P9 ₅ to P9 ₇ is not in 64 pin version.
P10 ₀ ~P10 ₇	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P0. This port can also function as A-D converter input pins, as selected by software. Furthermore, P10 ₄ -P10 ₇ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

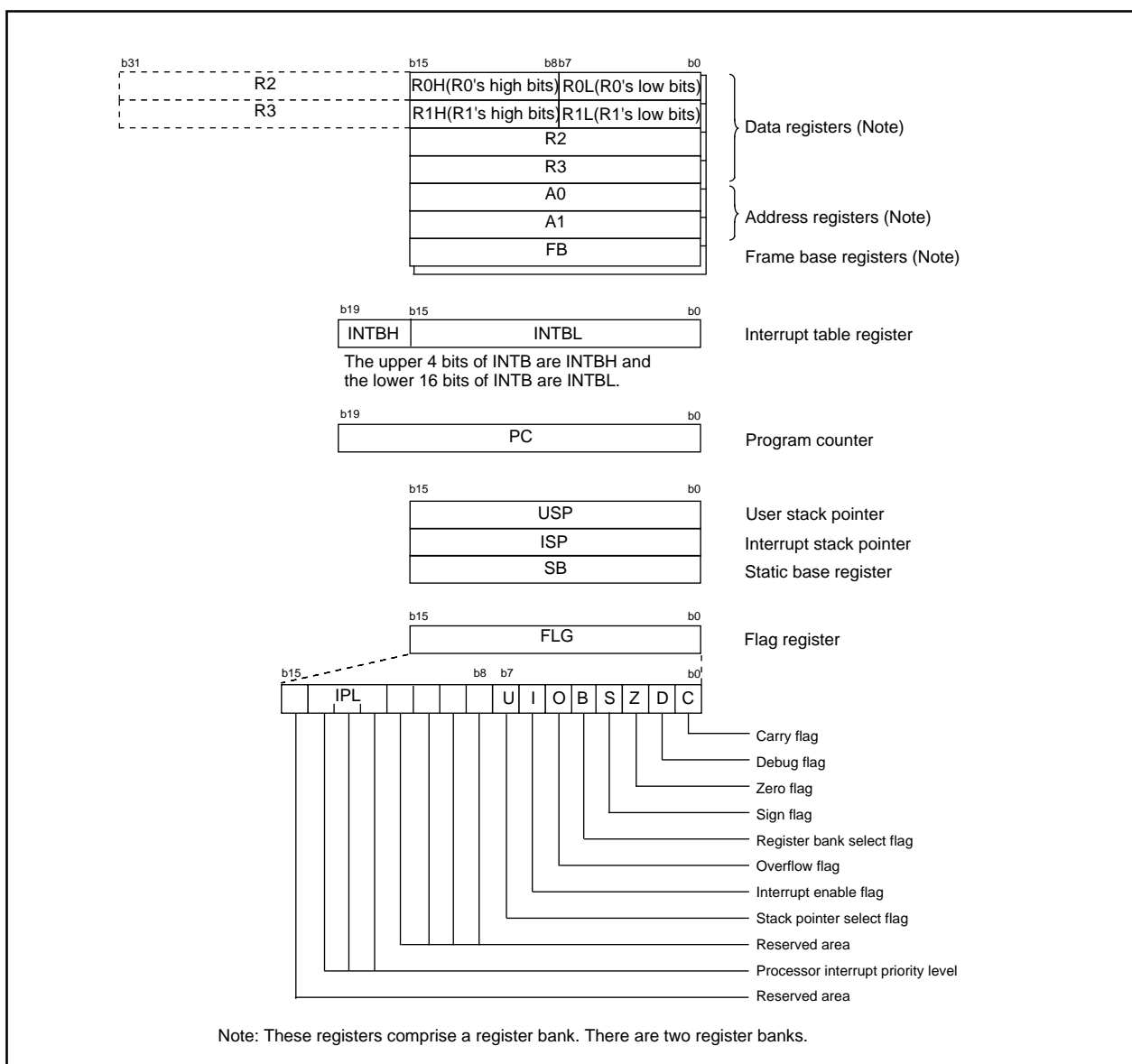


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/28 group. The linear address space of 1M bytes extends from address 00000₁₆ to FFFFF₁₆. From FFFFF₁₆ down is ROM. For example, in the M30280F8HP, there are 64 Kbytes of internal ROM from F0000₁₆ to FFFFF₁₆.

The vector table for fixed interrupts, such as Reset and NMI, is mapped from FFFDC₁₆ to FFFFF₁₆. The starting address of the interrupt routine is stored here.

The address of the vector table for timer interrupts, etc., can be set as desired using the interrupt table register (INTB). See the section on interrupts for details.

From 00400₁₆ up is RAM. For example, in the M30280F8HP, 4K bytes of internal RAM is mapped to the space from 00400₁₆ to 013FF₁₆. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from 0F000₁₆ to 0FFFF₁₆ on all versions.

The SFR area is mapped from 00000₁₆ to 003FF₁₆. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is allocated to the address from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

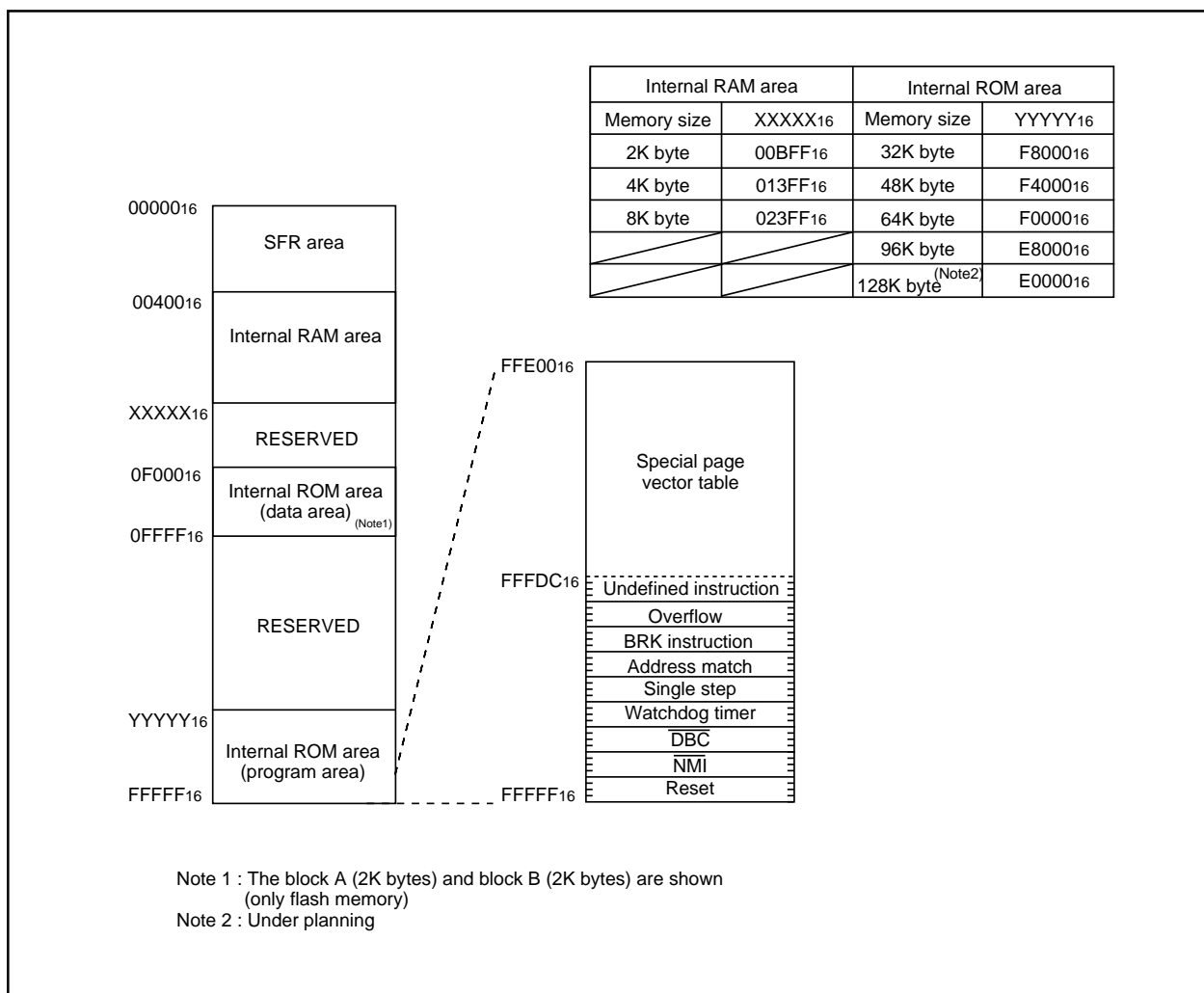


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register Name	Acronym	Value after Reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register (Note 2)	CM2	0X000010 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	?? ₁₆
000F ₁₆	Watchdog timer control register	WDC	00?????? ₂ (Note 3)
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 (Note 4)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 (Note 4)	VCR2	00 ₁₆
001B ₁₆			
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Voltage down detection interrupt register	D4INT	00 ₁₆
0020 ₁₆	DMA0 source pointer	SAR0	?? ₁₆
0021 ₁₆			?? ₁₆
0022 ₁₆			X? ₁₆
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	?? ₁₆
0025 ₁₆			?? ₁₆
0026 ₁₆			X? ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	?? ₁₆
0029 ₁₆			?? ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000?00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	?? ₁₆
0031 ₁₆			?? ₁₆
0032 ₁₆			X? ₁₆
0033 ₁₆			
0034 ₁₆	DMA1 destination pointer	DAR1	?? ₁₆
0035 ₁₆			?? ₁₆
0036 ₁₆			X? ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	?? ₁₆
0039 ₁₆			?? ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000?00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.
 Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
 Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltage at the Vcc pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1"(RAM retention limit detection circuit enable).
 Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Noting is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.1. SFR Map (1 of 7)

Address	Register Name	Acronym	Value after Reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00?0002
0045 ₁₆	IC/OC interrupt control register	ICOCIC	XXXX?0002
0046 ₁₆	IC/OC interrupt control register 1, I ² C-BUS interface interrupt control register	ICOC1IC, IICIC	XXXX?0002
0047 ₁₆	IC/OC interrupt control register 2, SCL/SDA interrupt control register	ICOC2IC, SCLDAIC	XXXX?0002
0048 ₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00?0002
0049 ₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00?0002
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?0002
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXX?0002
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXX?0002
004D ₁₆	Key input interrupt control register	KUPIC	XXXX?0002
004E ₁₆	A-D conversion interrupt control register	ADIC	XXXX?0002
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?0002
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXX?0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXX?0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXX?0002
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXX?0002
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXX?0002
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXX?0002
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXX?0002
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXX?0002
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXX?0002
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXX?0002
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXX?0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00?0002
005E ₁₆	INT1 interrupt control register	INT1IC	XX00?0002
005F ₁₆	INT2 interrupt control register	INT2IC	XX00?0002
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.2. SFR Map (2 of 7)

Address	Register Name	Acronym	Value after Reset
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
≈			≈
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 (Note 2)	FMR4	010000002
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0?2
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	??0000012
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
≈			≈
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆	Ring oscillator control register	ROCR	000001012
025D ₁₆	Pin assignment control register	PACR	0016
025E ₁₆	Peripheral clock select register	PCLKR	000000112
025F ₁₆			
≈			≈
02E0 ₁₆	I ² C0 data shift register	S00	??16
02E1 ₁₆	I ² C0 address register 2	S0D02	0016
02E2 ₁₆	I ² C0 address register	S0D0	0016
02E3 ₁₆	I ² C0 control register 0	S1D0	0016
02E4 ₁₆	I ² C0 clock control register	S20	0016
02E5 ₁₆	I ² C0 start/stop condition control register	S2D0	000110102
02E6 ₁₆	I ² C0 control register 1	S3D0	001100002
02E7 ₁₆	I ² C0 control register 2	S4D0	0016
02E8 ₁₆	I ² C0 status register	S10	0001000X2
02E9 ₁₆			
02EA ₁₆			
≈			≈
02FE ₁₆			
02FF ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.
 Note 2: This register is included in the flash memory version.

X : Noting is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.3. SFR Map (3 of 7)

Address	Register Name	Acronym	Value after Reset
0300 ₁₆ 0301 ₁₆	TM/WG register 0	G1TM0/G1PO0	?? ₁₆ ?? ₁₆
0302 ₁₆ 0303 ₁₆	TM/WG register 1	G1TM1/G1PO1	?? ₁₆ ?? ₁₆
0304 ₁₆ 0305 ₁₆	TM/WG register 2	G1TM2/G1PO2	?? ₁₆ ?? ₁₆
0306 ₁₆ 0307 ₁₆	TM/WG register 3	G1TM3/G1PO3	?? ₁₆ ?? ₁₆
0308 ₁₆ 0309 ₁₆	TM/WG register 4	G1TM4/G1PO4	?? ₁₆ ?? ₁₆
030A ₁₆ 030B ₁₆	TM/WG register 5	G1TM5/G1PO5	?? ₁₆ ?? ₁₆
030C ₁₆ 030D ₁₆	TM/WG register 6	G1TM6/G1PO6	?? ₁₆ ?? ₁₆
030E ₁₆ 030F ₁₆	TM/WG register 7	G1TM7/G1PO7	?? ₁₆ ?? ₁₆
0310 ₁₆	WG control register 0	G1POCR0	0X00X0002
0311 ₁₆	WG control register 1	G1POCR1	0X00X0002
0312 ₁₆	WG control register 2	G1POCR2	0X00X0002
0313 ₁₆	WG control register 3	G1POCR3	0X00X0002
0314 ₁₆	WG control register 4	G1POCR4	0X00X0002
0315 ₁₆	WG control register 5	G1POCR5	0X00X0002
0316 ₁₆	WG control register 6	G1POCR6	0X00X0002
0317 ₁₆	WG control register 7	G1POCR7	0X00X0002
0318 ₁₆	TM control register 0	G1TMCR0	00 ₁₆
0319 ₁₆	TM control register 1	G1TMCR1	00 ₁₆
031A ₁₆	TM control register 2	G1TMCR2	00 ₁₆
031B ₁₆	TM control register 3	G1TMCR3	00 ₁₆
031C ₁₆	TM control register 4	G1TMCR4	00 ₁₆
031D ₁₆	TM control register 5	G1TMCR5	00 ₁₆
031E ₁₆	TM control register 6	G1TMCR6	00 ₁₆
031F ₁₆	TM control register 7	G1TMCR7	00 ₁₆
0320 ₁₆	Base timer register	G1BT	?? ₁₆
0321 ₁₆			?? ₁₆
0322 ₁₆	Base timer control register 0	G1BCR0	00 ₁₆
0323 ₁₆	Base timer control register 1	G1BCR1	00 ₁₆
0324 ₁₆	TM prescaler register 6	G1TPR6	00 ₁₆
0325 ₁₆	TM prescaler register 7	G1TPR7	00 ₁₆
0326 ₁₆	Function enable register	G1FE	00 ₁₆
0327 ₁₆	Function select register	G1FS	00 ₁₆
0328 ₁₆	Base timer reset register	G1BTRR	?? ₁₆
0329 ₁₆			?? ₁₆
032A ₁₆	Divider register	G1DV	00 ₁₆
032B ₁₆			
032C ₁₆			
032D ₁₆			
032E ₁₆			
032F ₁₆			
0330 ₁₆	Interrupt request register 0	G1IR	?? ₁₆
0331 ₁₆	Interrupt enable register 0	G1IE0	00 ₁₆
0332 ₁₆	Interrupt enable register 1	G1IE1	00 ₁₆
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	P17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.4. SFR Map (4 of 7)

Address	Register Name	Acronym	Value after Reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	?? ₁₆
0343 ₁₆			?? ₁₆
0344 ₁₆	Timer A2-1 register	TA21	?? ₁₆
0345 ₁₆			?? ₁₆
0346 ₁₆	Timer A4-1 register	TA41	?? ₁₆
0347 ₁₆			?? ₁₆
0348 ₁₆	Three-phase PWM control register 0	INVC0	00 ₁₆
0349 ₁₆	Three-phase PWM control register 1	INVC1	00 ₁₆
034A ₁₆	Three-phase output buffer register 0	IDB0	00 ₁₆
034B ₁₆	Three-phase output buffer register 1	IDB1	00 ₁₆
034C ₁₆	Dead time timer	DTT	?? ₁₆
034D ₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	X? ₁₆
034E ₁₆	Position-data-retain function control register	PDRF	XXXX0000 ₂
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆			
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆	Interrupt request cause select register 2	IFSR2A	00XXXXXX ₂ (Note 2)
035F ₁₆	Interrupt request cause select register	IFSR	00 ₁₆
0360 ₁₆	SI/O3 transmit/receive register	S3TRR	?? ₁₆
0361 ₁₆			
0362 ₁₆	SI/O3 control register	S3C	01000000 ₂
0363 ₁₆	SI/O3 bit rate generator	S3BRG	?? ₁₆
0364 ₁₆	SI/O4 transmit/receive register	S4TRR	?? ₁₆
0365 ₁₆			
0366 ₁₆	SI/O4 control register	S4C	01000000 ₂
0367 ₁₆	SI/O4 bit rate generator	S4BRG	?? ₁₆
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X ₂
0376 ₁₆	UART2 special mode register 2	U2SMR2	X0000000 ₂
0377 ₁₆	UART2 special mode register	U2SMR	X0000000 ₂
0378 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0379 ₁₆	UART2 bit rate generator	U2BRG	?? ₁₆
037A ₁₆	UART2 transmit buffer register	U2TB	??????? ₂
037B ₁₆			XXXXXXXX ₂
037C ₁₆	UART2 transmit/receive control register 0	U2C0	00001000 ₂
037D ₁₆	UART2 transmit/receive control register 1	U2C1	00000010 ₂
037E ₁₆	UART2 receive buffer register	U2RB	??????? ₂
037F ₁₆			?????XX ₂

Note 1: The blank areas are reserved and cannot be accessed by users.
 Note 2: Write "1" to bit 0 after reset.

X : Nothing is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.5. SFR Map (5 of 7)

Address	Register Name	Acronym	Value after Reset
0380 ₁₆	Count start flag	TABSR	0016
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX2
0382 ₁₆	One-shot start flag	ONSF	0016
0383 ₁₆	Trigger select register	TRGSR	0016
0384 ₁₆	Up-down flag	UDF	0016
0385 ₁₆			
0386 ₁₆	Timer A0 register	TA0	??16
0387 ₁₆			??16
0388 ₁₆	Timer A1 register	TA1	??16
0389 ₁₆			??16
038A ₁₆	Timer A2 register	TA2	??16
038B ₁₆			??16
038C ₁₆	Timer A3 register	TA3	??16
038D ₁₆			??16
038E ₁₆	Timer A4 register	TA4	??16
038F ₁₆			??16
0390 ₁₆	Timer B0 register	TB0	??16
0391 ₁₆			??16
0392 ₁₆	Timer B1 register	TB1	??16
0393 ₁₆			??16
0394 ₁₆	Timer B2 register	TB2	??16
0395 ₁₆			??16
0396 ₁₆	Timer A0 mode register	TA0MR	0016
0397 ₁₆	Timer A1 mode register	TA1MR	0016
0398 ₁₆	Timer A2 mode register	TA2MR	0016
0399 ₁₆	Timer A3 mode register	TA3MR	0016
039A ₁₆	Timer A4 mode register	TA4MR	0016
039B ₁₆	Timer B0 mode register	TB0MR	00?00002
039C ₁₆	Timer B1 mode register	TB1MR	00?X00002
039D ₁₆	Timer B2 mode register	TB2MR	00?X00002
039E ₁₆	Timer B2 special mode register	TB2SC	X00000002
039F ₁₆			
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	0016
03A1 ₁₆	UART0 bit rate generator	U0BRG	??16
03A2 ₁₆	UART0 transmit buffer register	U0TB	???????2
03A3 ₁₆			XXXXXXX2
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	000010002
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	000000102
03A6 ₁₆	UART0 receive buffer register	U0RB	???????2
03A7 ₁₆			?????XX2
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	0016
03A9 ₁₆	UART1 bit rate generator	U1BRG	??16
03AA ₁₆	UART1 transmit buffer register	U1TB	???????2
03AB ₁₆			XXXXXXX2
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	000010002
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	000000102
03AE ₁₆	UART1 receive buffer register	U1RB	???????2
03AF ₁₆			?????XX2
03B0 ₁₆	UART transmit/receive control register 2	UCON	X00000002
03B1 ₁₆			
03B2 ₁₆			
03B3 ₁₆			
03B4 ₁₆			
03B5 ₁₆			
03B6 ₁₆			
03B7 ₁₆			
03B8 ₁₆	DMA0 request cause select register	DM0SL	0016
03B9 ₁₆			
03BA ₁₆	DMA1 request cause select register	DM1SL	0016
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
 ? : Value indeterminate at reset

Figure 4.6. SFR Map (6 of 7)

Address	Register Name	Acronym	Value after Reset
03C0 ₁₆ 03C1 ₁₆	A-D register 0	AD0	????????? XXXXXXXX???
03C2 ₁₆ 03C3 ₁₆	A-D register 1	AD1	????????? XXXXXXXX???
03C4 ₁₆ 03C5 ₁₆	A-D register 2	AD2	????????? XXXXXXXX???
03C6 ₁₆ 03C7 ₁₆	A-D register 3	AD3	????????? XXXXXXXX???
03C8 ₁₆ 03C9 ₁₆	A-D register 4	AD4	????????? XXXXXXXX???
03CA ₁₆ 03CB ₁₆	A-D register 5	AD5	????????? XXXXXXXX???
03CC ₁₆ 03CD ₁₆	A-D register 6	AD6	????????? XXXXXXXX???
03CE ₁₆ 03CF ₁₆	A-D register 7	AD7	????????? XXXXXXXX???
03D0 ₁₆ 03D1 ₁₆			
03D2 ₁₆	A-D trigger control register	ADTRGCON	XXXX00002
03D3 ₁₆	A-D convert status register 0	ADSTAT0	00000X002
03D4 ₁₆ 03D5 ₁₆	A-D control register 2	ADCON2	0016
03D6 ₁₆	A-D control register 0	ADCON0	00000????
03D7 ₁₆	A-D control register 1	ADCON1	0016
03D8 ₁₆ 03D9 ₁₆ 03DA ₁₆ 03DB ₁₆ 03DC ₁₆ 03DD ₁₆ 03DE ₁₆ 03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	??16
03E1 ₁₆	Port P1 register	P1	??16
03E2 ₁₆	Port P0 direction register	PD0	0016
03E3 ₁₆	Port P1 direction register	PD1	0016
03E4 ₁₆	Port P2 register	P2	??16
03E5 ₁₆	Port P3 register	P3	??16
03E6 ₁₆	Port P2 direction register	PD2	0016
03E7 ₁₆	Port P3 direction register	PD3	0016
03E8 ₁₆ 03E9 ₁₆ 03EA ₁₆ 03EB ₁₆			
03EC ₁₆	Port P6 register	P6	??16
03ED ₁₆	Port P7 register	P7	??16
03EE ₁₆	Port P6 direction register	PD6	0016
03EF ₁₆	Port P7 direction register	PD7	0016
03F0 ₁₆	Port P8 register	P8	??16
03F1 ₁₆	Port P9 register	P9	???X?????
03F2 ₁₆	Port P8 direction register	PD8	0016
03F3 ₁₆	Port P9 direction register	PD9	000X00002
03F4 ₁₆ 03F5 ₁₆	Port P10 register	P10	??16
03F6 ₁₆	Port P10 direction register	PD10	0016
03F7 ₁₆ 03F8 ₁₆ 03F9 ₁₆ 03FA ₁₆ 03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	0016
03FD ₁₆	Pull-up control register 1	PUR1	0016
03FE ₁₆	Pull-up control register 2	PUR2	0016
03FF ₁₆	Port control register	PCR	0016

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Noting is mapped to this bit
 ? : Value indeterminate at reset

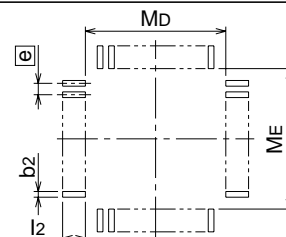
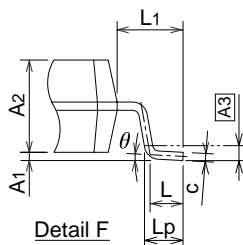
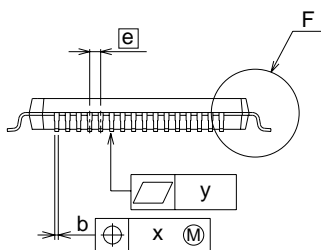
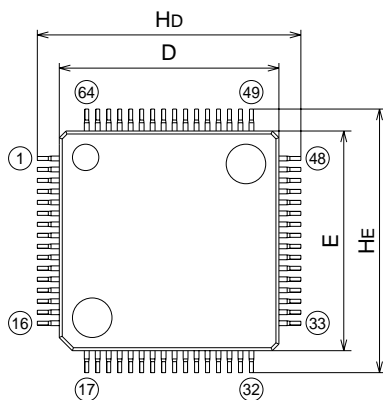
Figure 4.7. SFR Map (7 of 7)

5. Package

64P6Q-A (MMP)

Plastic 64pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	-	-	Cu Alloy



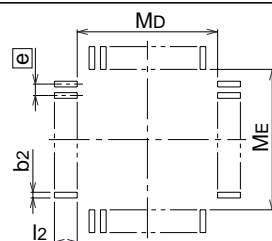
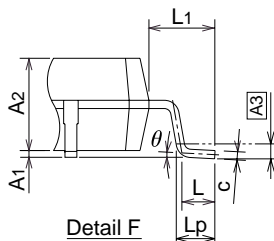
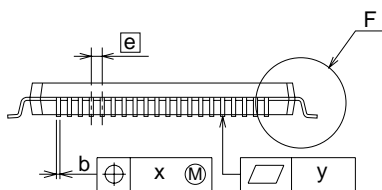
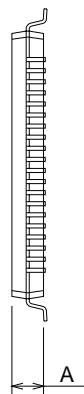
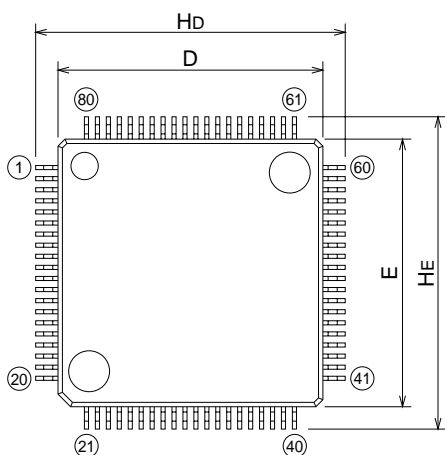
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	-	0.5	-
Hd	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	1.0	-	-
Md	-	10.4	-
ME	-	10.4	-

80P6Q-A (MMP)

Plastic 80pin 12X12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	-	0.47	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	-	0.5	-
Hd	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	12.4	-
ME	-	12.4	-

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Keep safety first in your circuit designs!

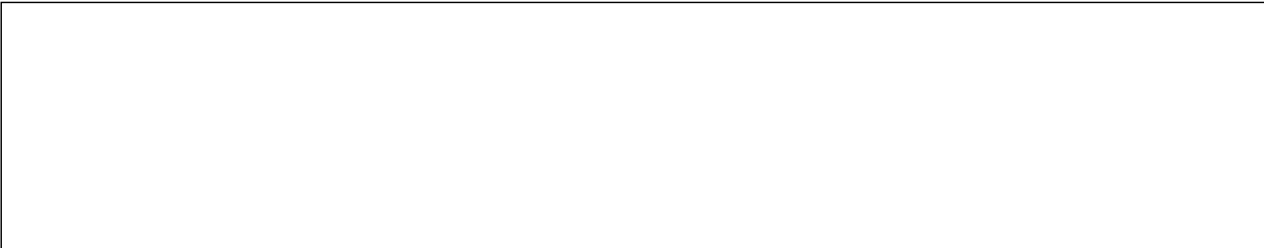
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