20C12 HART™ MODEM

Introduction

HART is a trade mark of Rosemount Corporation.

The NCR 20C12 (Highway Addressable Remote Transducer) HART low power FSK modem is a single chip CMOS model that operates at the Bell 202 standards.

The NCR 20C12 HART modem is ideally suited for factory automation, especially in areas that require ultra low power such as intrinsically safe environments.

Features

- Operates at the Bell 202 Standard Forward Bit Rate of 1200 bits/sec
- Uses the Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- Transmit Modulation of 1200 Baud
- Receive Modulation of 1200 Baud
- Single Chip Frequency -Shift-Keying (FSK)
- Optimal for Intrinsically Safe Applications
- Singel 5-V Power Supply
- CMOS and TTL Compatible
- Reliable CMOS Technology
- 16 pin DIP or 28-pin PLCC packages available

General Description

The NCR 20C12 (Highway Addressable Remote Transducer) HART low power FSK Modem is a single-chip, CMOS modem for use in process control instruments or other low power equipment. The modem circuitry is digital. It provides only the modulating and demodulating functions and is intended to be used with external circuits which may amplify, filter, and shape the media signals.

The modem operates at the Bell-202 standard upper (forward) bit rate of 1200 bits/sec and uses the Bell-202 shaft frequencies of nominally 1200 Hz and 2200 Hz. With proper conditioning of them media, it can communicate with other Bell-202 modems.

To conserve power, the demodulator is stopped while the modulator operates and vice versa. Therefore, operation is half-duplex. The modem is packaged in a standard 16-pin Dual In-line Package (DIP) or in a 28-pin Plastic Leaded Chip Carrier (PLCC). The HART modem operates from a single 5-volt supply and requires an externally generated clock fo 460.8 kHz.

The modem provides an active low carrier detect output and a 19.2 kHz clock output. No external adjustments or special biasing are required.

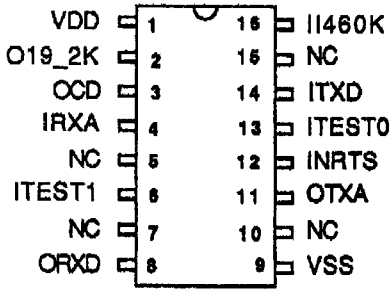
Pin Description

SIGNAL	INPUT or OUTPUT	PIN #		DESCRIPTION
		DIP	PLCC	
VDD	-	1	1	+ 5 V power supply
O19_2k	O	2	2	User clock. Nominally 19.2 kHz (16 times bit rate).
CCD	O	3	3	Carrier Detect is low (0) when carrier is present.
IRXA	I	4	4	Demodulator Input accepts 1200 (2200) Hz square wave FSK modulated carrier.
NC	-	5	5-12	No internal connection.
ITEST1	I	6	13	Test Input One must be connected to VSS during normal operation.
NC	-	7	-	No Internal Connection.
ORXD	O	8	14	Demodulator Output provides a logic 1 (0) in response to a 1200 (2200) Hz FSK square wave signal at IRXA. Demodulation takes place only when INRTS is a high (1). With INRTS low (0) the ORXD output is not defined.
VSS	-	9	15	Power supply ground.
NC	-	10	-	No Internal connection.
OTXA	O	11	16	Modulator Output provides a square wave FSK output 1200 (2200) Hz in response to a logic 1 (0) applied to ITXD. OTXA is active when INRTS is low (0). It goes to a high-impedance state when INRTS is high (1).
INRTS	I	12	17	Request To Send selects operation of the modulator when low (0) and the demodulator when high (1), causing OTXA to go to a high-impedance state when high (1).
ITEST0	I	13	26	Test Input Zero must be connected to VSS during normal operation.
ITXD	I	14	27	Modulator Input accepts input data (logic 1 or 0) for modulating the carrier output at OTXA.
NC	-	15	18-25	No Internal Connection.
I1460K	I	16	28	Input Clock clocks the modem circuitry; the frequency is nominally 460.8 kHz.

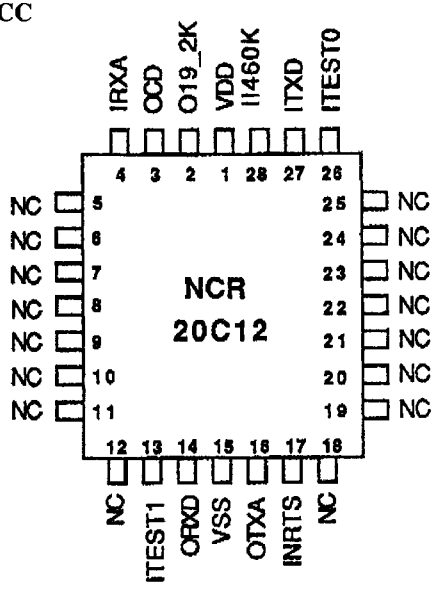
Note: Signal names starting with 'I' are inputs and signal names starting with 'O' are outputs.

Pin Out

16 Pin Dip



28 Pin PLCC



Electrical Characteristics

The conditions for the following electrical characteristics apply to the full operating temperature range with a supply voltage of 5.0 volts.

DC Characteristics

Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
TSTG	Storage Temperature	-65	150	°C
TA	Operating Free-air Temperature	-40	+85	°C
VDD	Supply Voltage (non-operating)		7	V

Cautions

1. CMOS Devices are damaged by high energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating.
2. Remove power before insertion or removal of this device.
3. Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operation conditions specified in this document is not implied.

Operating Conditions

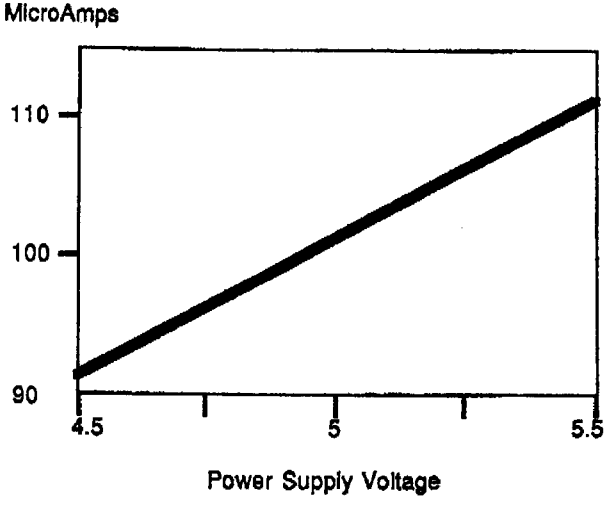
SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VDD	Supply Voltage	4.5	5.5	V	
VIN	Input Voltage	VSS -0.3	VDD +0.3	V	
VIH	Logical 1 Input Voltage	2.0	VDD +0.3	V	
VIL	Logical 0 Input Voltage	VSS -0.3	0.8	V	
VOL	Output Low Voltage		0.4	V	Output Sink Current=4.0mA
VOH	Output High Voltage	2.4	VDD -0.3	V	Output Source Current=4.0mA
IDD*	Supply Current		437	µA	During Demodulation
			101	µA	During Modulation
IIN	Input Leakage Current		+/-1	µA	VIN=VDD or VSS
ITO	High-Impedance Output Leakage Current		+/- 10 µA typical		Applies only to OTXA
CIN	Input Capacitance		10pF typical		

*** IDD NOTES:**

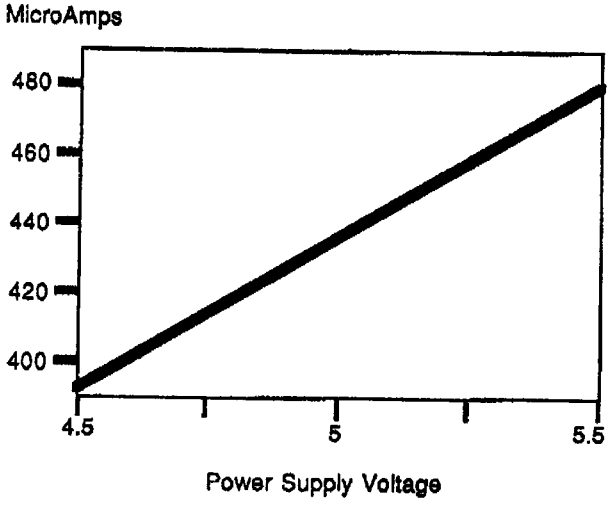
- 50pF load on all outputs
- All input rise and fall time requirements satisfied
- Clock (II460K) freq=460.8kHz +/-0.1%
- See the following Current vs Voltage Charts for more information.

Current vs Voltage Charts

Modulation



Demodulation



AC Characteristics

Clock Frequency (at the II460K pin):	460.8 kHz +/- 0.1%
Clock Pulse Widths:	high level = 150 nanoseconds min. low level = 150 nanoseconds min.
Clock Rise and Fall Time:	10 nanoseconds max.
IRXA Input Rise and Fall Time:	200 nanoseconds max.
Other Inputs Rise and Fall Time:	50 nanoseconds max.
Output Rise and Fall Time*:	10 nanoseconds max.

*Condition: 50 pF capacitance on all outputs.

Modem Characteristics

Carrier Detect

Carrier Detect Frequency Range: This is the range of frequencies applied at IRXA over which OCD must go low (logic 0). Conditions: 1) Clock (II460K) frequency of 460.8 kHz +/- 0.1%. 2) Input (IRXA) asymmetry of 5% max.	1000 Hz to 2575 Hz.
Time From Carrier Input To Carrier Detect: This is the time from the start of a valid carrier signal at IRXA until OCD goes to logic low (0).	Minimum = 9.0 millisec. Maximum = 15.0 millisec.
Time From Carrier Loss To Carrier Undetect: This is the time from the loss of a valid carrier signal at IRXA until OCD goes to a logic high (1).	1 millisecond maximum
User Clock (O19_2K) Frequency: This clock frequency is proportional to the 460.8kHz clock at II460K.	19.2 kHz nominal.

Modulator

Modulator Output Frequency (at the OTXA pin):
Nominal high frequency (logic 0 applied to ITXD) = 2194.3 Hz
Nominal low frequency (logic 1 applied to ITXD) =1196.9 Hz
The modulator output frequencies are proportional to the input clock frequency (applied to the II460K pin).

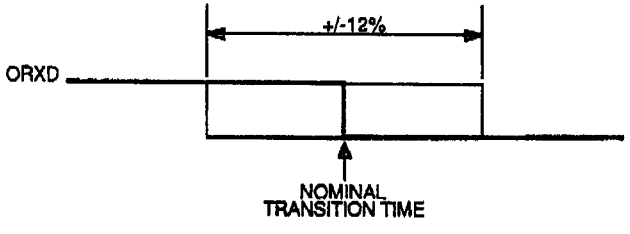
Modulator phase continuity error: +/- 10 degrees maximum.

Demodulator

Maximum Demodulator Jitter: +/- 12% of one bit time

Conditions:
1) Input frequencies at 1200 Hz +/- 10 Hz and 2200 Hz +/- 20 Hz.
2) Clock (II460K) frequency of 460.8 kHz +/- 0.1 %.
3) Input (IRXA) asymmetry = 0.

Representation of Jitter:



Functional Description

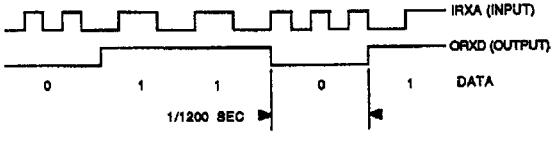
The modem uses shift frequencies of nominally 1200 Hz (representing a digital one) and 2200 Hz (digital zero). The bit rate is nominally 1200 bit/second. There are four major functional blocks: clocks, demodulator, modulator and carrier detect.

Clocks

The clock section accepts a digital input frequency of 460.8 kHz from an external source. This is used in various counter arrangements to generate several internal clocks. One internal clock at a nominal frequency of 19.2 kHz is also brought to an output pin for use in reconstructing the data in circuits external to the modem. All circuit operations can be performed with a master clock frequency of 460.8 kHz. This is considerably lower than the clock frequencies used in existing single-chip modems and contributes to a low current consumption. Various sections of the model are shut down (not clocked) when not being used. This further reduces power consumption.

Demodulator

The demodulator accepts an FSK signal at its IRXA input and reproduces the original modulating signal at its ORXD output. Both the input and output are digital signals as illustrated below.



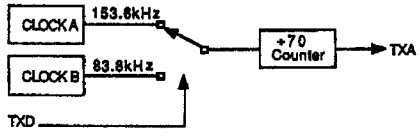
Demodulator Signals

Modulator

The modulator accepts digital data in NRZ form at its ITXD input and generates the FSK modulated signal at its OTXA output. An additional requirement for the modulator is that it provide phase continuous modulation. That is, when switching from one to the other of the shift frequencies, the phase angle of the modulated signal is preserved.

A simplified modulator block diagram is shown below. It works by counting down one or the other of two clocks, A or B, depending on whether the input signal is high or low. Clock A (153.6 kHz) is derived by dividing the 460.8 kHz oscillator frequency by 3. Clock B (83.78) kHz is derived by dividing the 460.8 kHz oscillator frequency by 5.5. The counter in the diagram is a divide-by-70. This means that the two shift frequencies are 1196.9 Hz and 2194.3 Hz.

Since the modulator works by counting down clocks, its output transitions are quantized as to when they can occur. The maximum timing error due to quantization is 12 microseconds, which is the period of the slower of the two clocks, A and B. At the higher of the two shift frequencies (2200 Hz), the phase error is 9.5 degrees, and at the lower of the two shift frequencies the phase error is 5.2 degrees.



Modulator Block Diagram

Carrier Detect

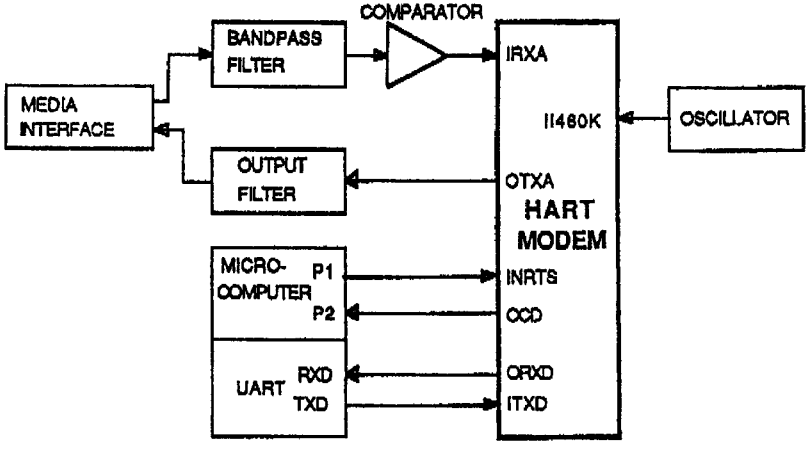
The active low carrier detect works by looking for incoming signal frequencies in the approximate range of 1200 Hz to 2200 Hz. This is done by measuring interval times between input transitions. If several successive interval time measurements fall within specific limits, carrier detect is indicated, and the carrier detect output is asserted. If, after the carrier has been detected, the measured interval time falls outside of these limits for some length of time, the carrier detect output is unasserted.

Typical Application

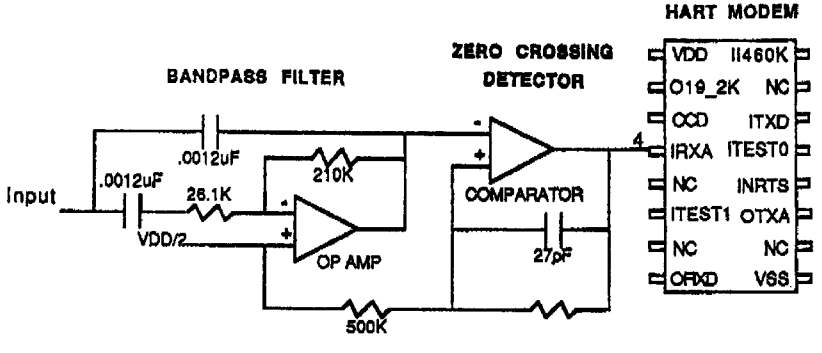
The modem will usually be applied as shown in the block diagram below. The received signal is filtered to reduce noise. The filter should include the band of frequencies from about 900 Hz to 2.5 kHz. The output of the filter is applied to the input of a comparator to provide the required signalling levels to the modem. Additional amplification may be required ahead of the filter to provide sufficient signal to the comparator. Be sure that the comparator switches at the zero crossings of the incoming waveform and is glitch free.

Depending on the application, the output filter may not be necessary. Omitting it will cause square waves to be applied to the signalling media.

A schematic showing a typical applications follows the block diagram.



Block Diagram of a Typical Application

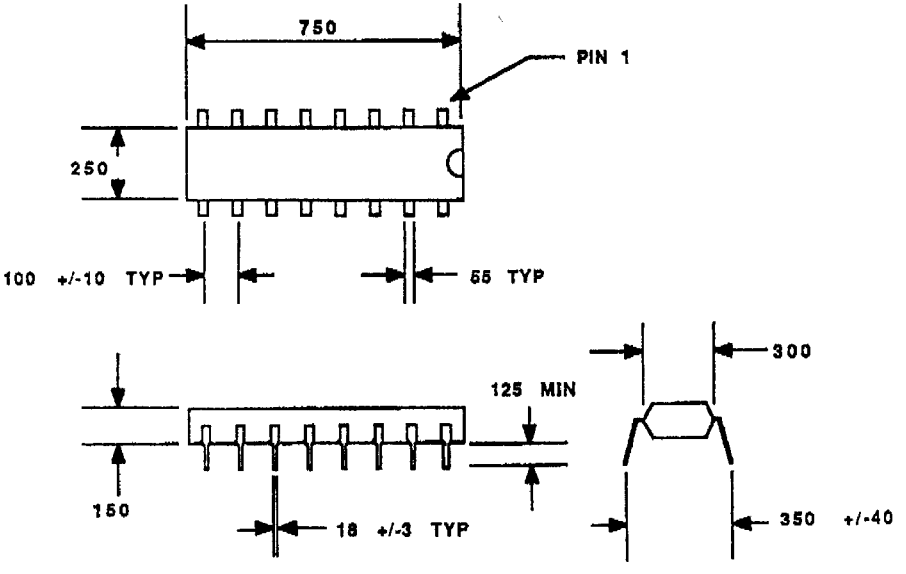


Schematic of a Typical Application

Mechanical Drawings

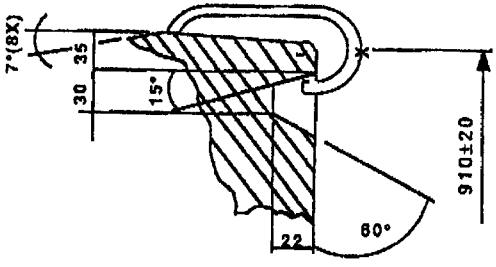
16-Pin Dual In-line Package (DIP)

Note: All units are 1/1000 inches



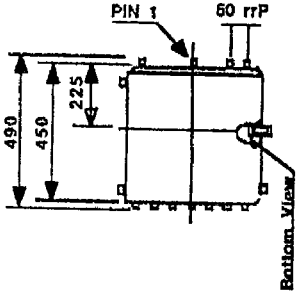
28-Pin Plastic Leaded Chip Carrier (PLCC) Package

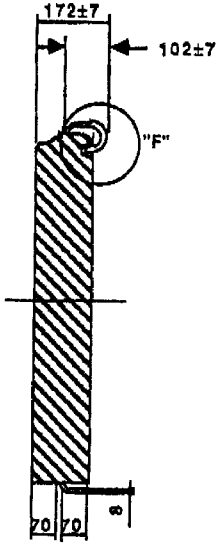
Note: All units are 1/1000 inches

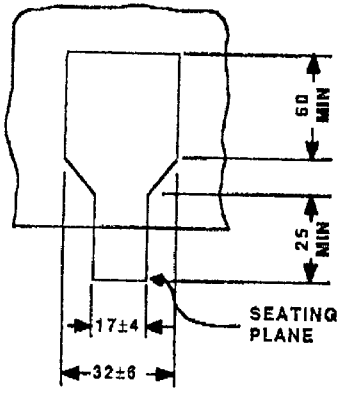


DETAIL OF "F"

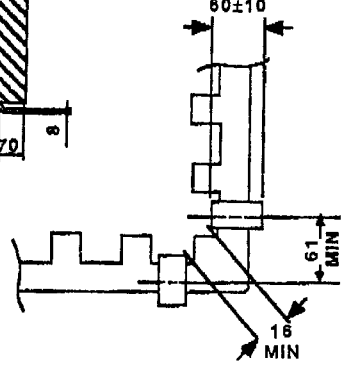
X: SURFACE MOUNT POINT







SIDE VIEW



BOTTOM VIEW

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