
 ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ FireWire, SCSI & USB
- ✓ Audio/Video Inputs
- ✓ xDSL Interfaces
- ✓ Cellular Phone Terminals

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Gnd) & Level 3(Line-Line)

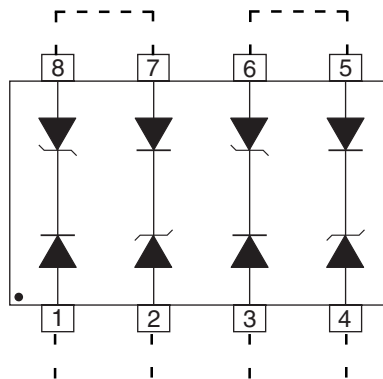
FEATURES

- ✓ 500 Watts Peak Pulse Power per Line (tp=8/20 μ s)
- ✓ Bidirectional Configuration
- ✓ Available in Multiple Voltage Types Ranging From 3V to 24V
- ✓ Protects Two (2) Lines
- ✓ ESD Protection > 40 kilovolts
- ✓ **ULTRA LOW CAPACITANCE: 5pF**
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8 Package
- ✓ Weight 70 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Logo, Marking Code, Date Code & Pin One Defined By Dot on Top of Package



PIN CONFIGURATION


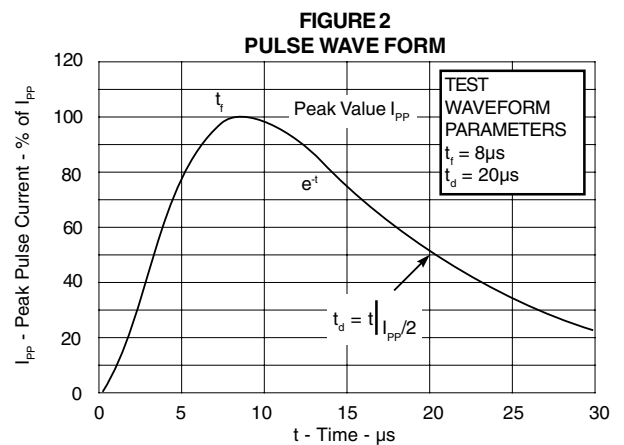
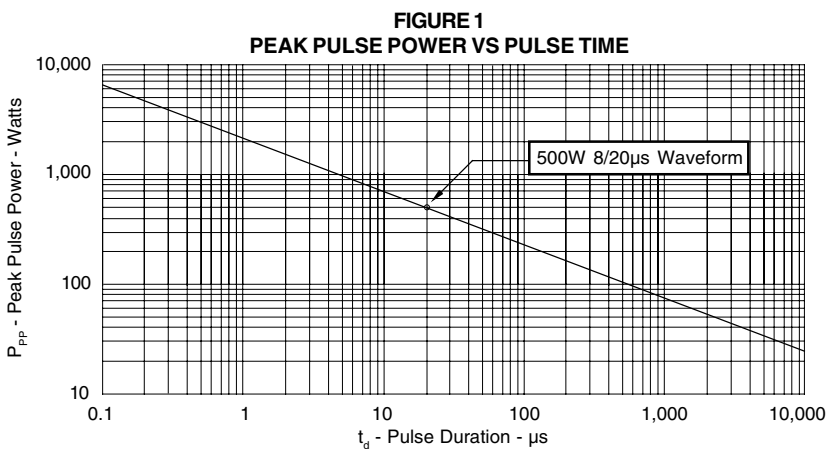
DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM LEAKAGE CURRENT	MAXIMUM CAPACITANCE (See Note 2)
		V_{WM} VOLTS	@ 1mA $V_{(BR)}$ VOLTS	@ $I_p = 1A$ V_C VOLTS	@ 8/20 μs $V_C @ I_{PP}$	@ V_{WM} I_D μA	@ 0V, 1 MHz C pF
PLCDA03	SGA	3.3	4.5	7.0	10.9V @ 43.0A	125	5
PLCDA05	SGB	5.0	6.0	9.8	13.5V @ 42.0A	20	5
PLCDA08	SGF	8.0	8.5	13.4	16.0V @ 34.0A	10	5
PLCDA12	SGC	12.0	13.3	19.0	25.9V @ 21.0A	1	5
PLCDA15	SGD	15.0	16.7	24.0	30.0V @ 17.0A	1	5
PLCDA24	SGE	24.0	26.7	43.0	49.0V @ 12.0A	1	5

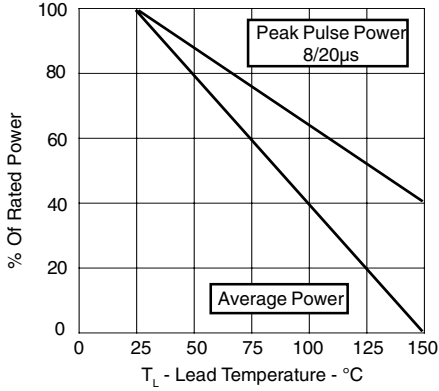
Note 1: Devices are designed to be used in parallel (See Circuit Diagram). For other applications, contact the factory. Do not apply surge in the "forward" direction of the TVS.

Note 1: Do not surge from pins 8 to 1, 2 to 7, 6 to 3 and 4 to 5. PIV typically greater than 100V for each rectifier die. Electrical characteristics apply to pins 1 to 8, 7 to 2, 3 to 6 and 5 to 4.

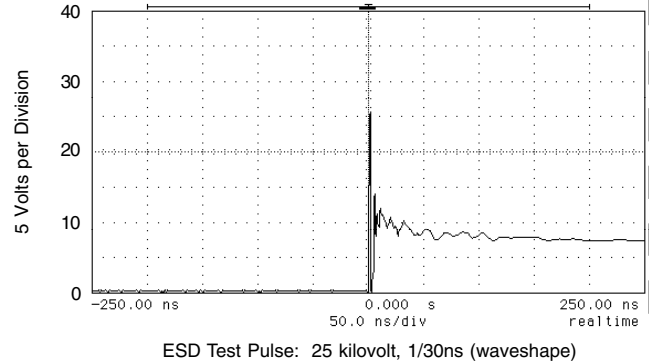


GRAPHS

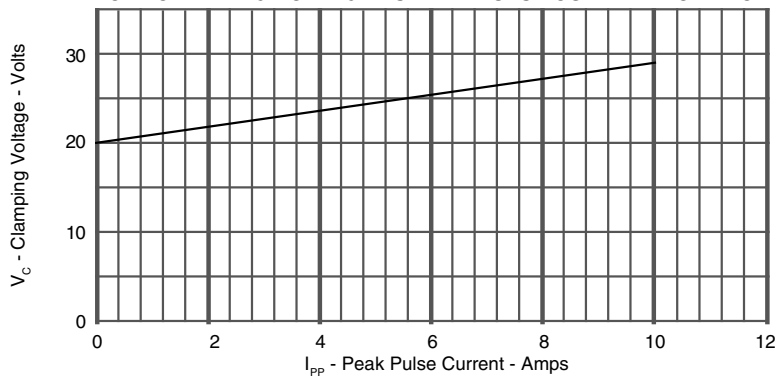
**FIGURE 3
POWER DERATING CURVE**



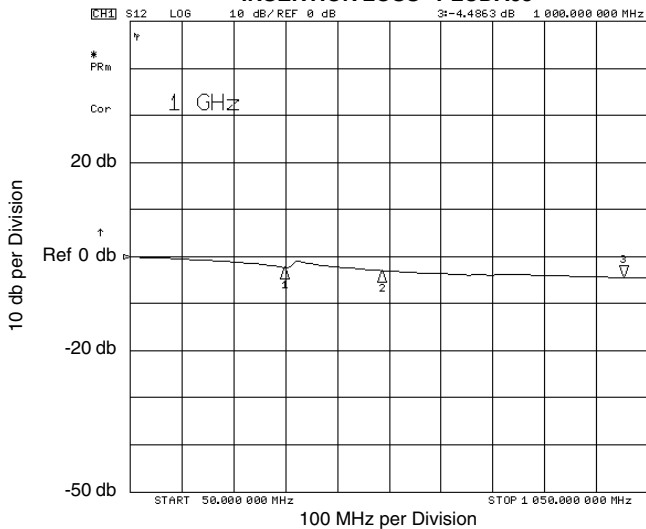
**FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PLCDA05**



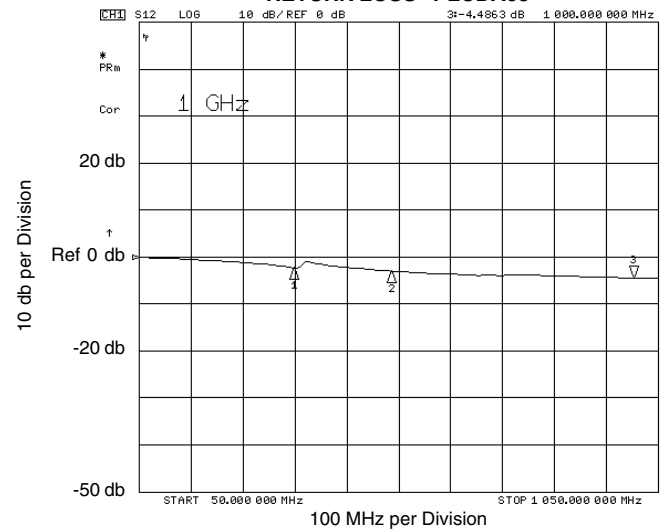
**FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PLCDA15**



**FIGURE 6
INSERTION LOSS - PLCDA05**



**FIGURE 7
RETURN LOSS - PLCDA05**



APPLICATION NOTE

The PLCDA Series are low capacitance, bidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{PP} per line for an 8/20 μ s waveshape and offers ESD protection > 40kv.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

Ideal for use in USB applications, the PLCDA Series provides up to two (2) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

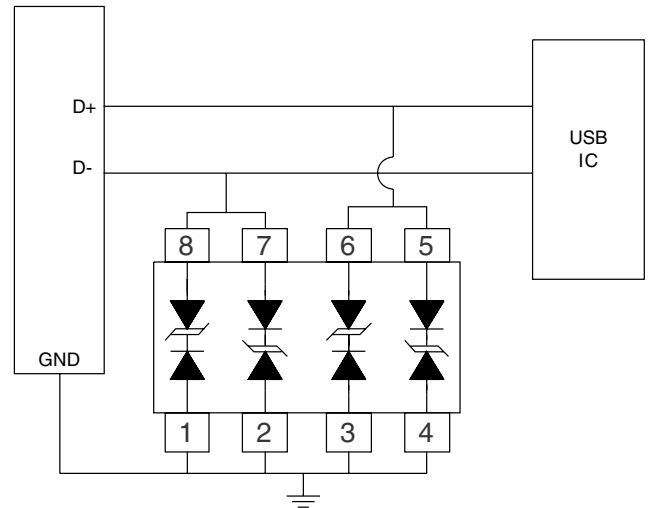
- ✓ Pins 1 & 2 and 3 & 4 are connected to Ground
- ✓ Pins 5 and 6 are connected to I/O Line D+
- ✓ Pins 7 and 8 are connected to I/O Line D-

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

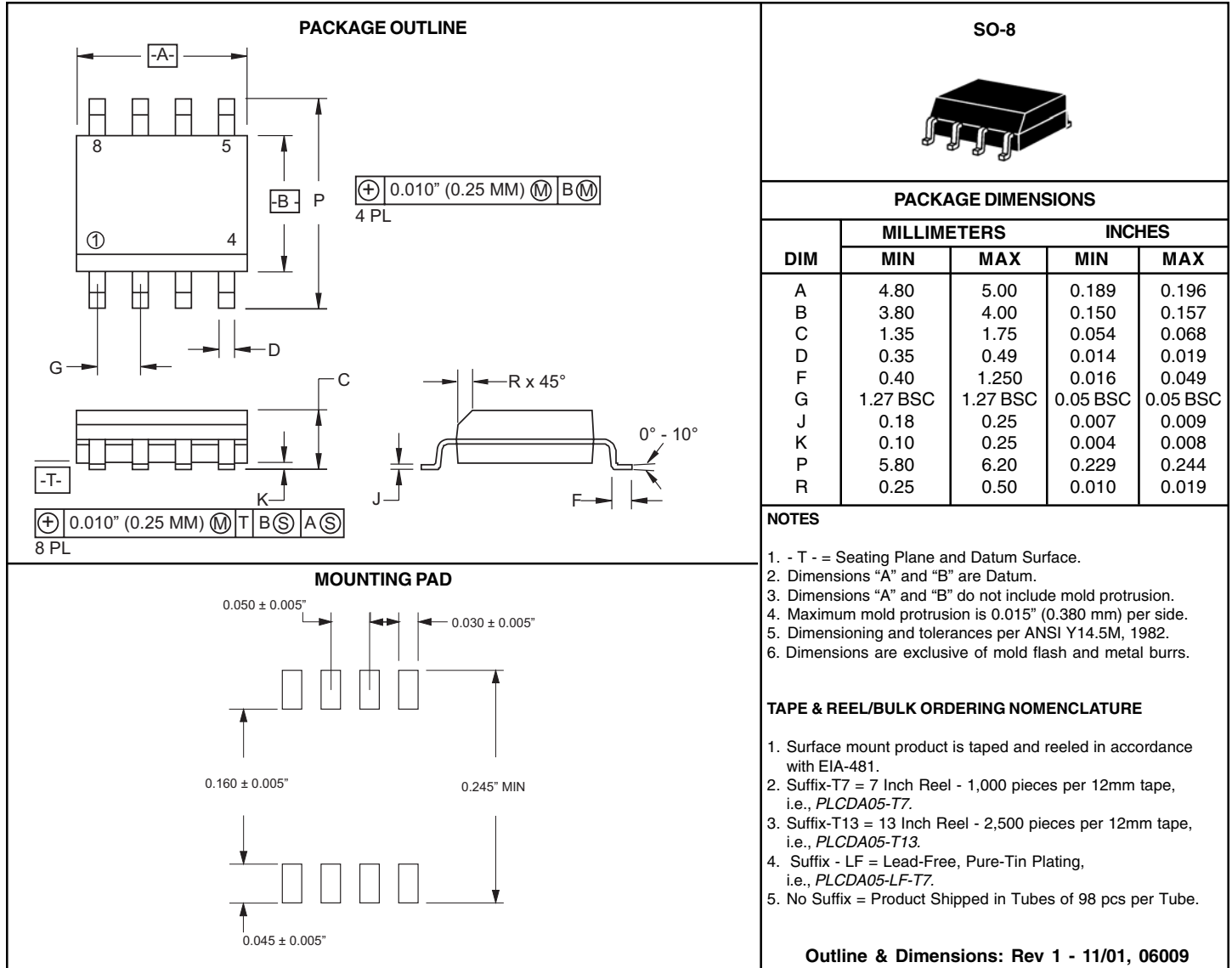
Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Typical Common-Mode USB Protection Circuit



PACKAGE OUTLINE & DIMENSIONS



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ProTek Devices

2929 South Fair Lane, Tempe, AZ 85282

Tel: 602-431-8101 Fax: 602-431-2288

E-Mail: sales@protekdevices.com

Web Site: www.protekdevices.com