

**LB1813M****FDD Spindle Motor Driver****Overview**

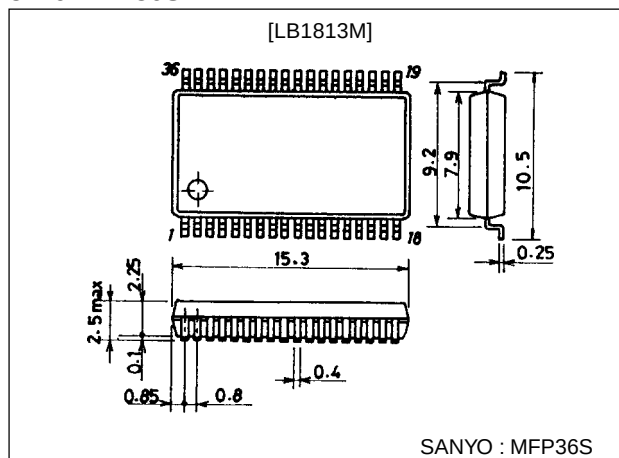
The LB1813M is 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

Features

- Three phase total wave linear driver.
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply)
- On-chip digital speed control : $f_{osc} = (1024 \times f_{FG}) / D$
When SL1=high D=5/8
SL1=low D=6/8
- Start/Stop circuit.
- Rotation speed switching.
- Current limiter circuit.
- On-chip index comparator (single hysteresis)
- On-chip index delay circuit.
- AGC circuit.
- Thermal protection circuit.

Package Dimensions

unit:mm

3129-MFP36S**Specifications****Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \max}$		7.0	V
Maximum output current	$I_O \max 1$	$t \leq 0.5s$	1.0	A
Steady maximum output current	$I_O \max 2$		0.7	A
Allowable power dissipation	$P_d \max$	Independent IC	1	W
Operating temperature	T_{opr}		-20 to +80	°C
Storage temperature	T_{stg}		-40 to +150	°C

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		4.2 to 6.5	V

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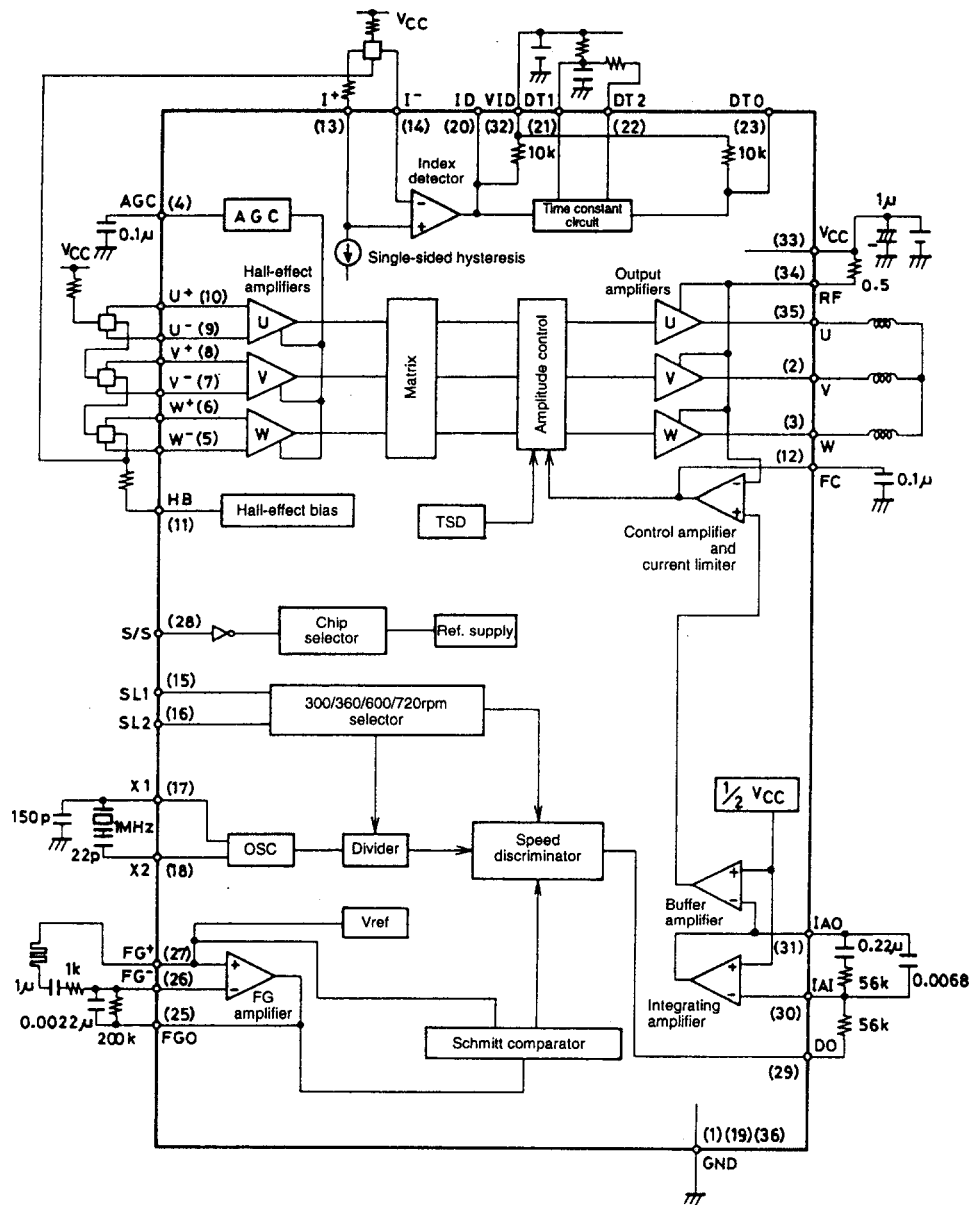
Electrical Characteristics at Ta = 25°C, VCC=5V

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Current drain	I _{CCO1}	V _{CC} =5.0V (Stop)			0.4	mA	
	I _{CC1}	V _{CC} =5.0V (Steady)		20	30	mA	
Time changeover bias current	I _{SL}				0.4	mA	
Time changeover input voltage1	V _{SLL}		0		0.8	V	
Time changeover input voltage2	V _{SLH}		2.0		V _{CC}	V	
S/S bias current	I _{S/S}				0.1	mA	
S/S start voltage	V _{S/S}		0		0.8	V	
S/S stop voltage	V _{S/S}		2.0		V _{CC}	V	
Hall-effect bias amplifier input current	I _{HB}				20	μA	
In-phase input voltage range	V _h		2.2		V _{CC} -0.7	V	
Differential input voltage range	V _{dif}		70		200	mVp-p	
Input offset voltage	V _{ho}				±10	mV	*
Hall-effect output voltage	V _H	I _H =5mA		1.5	1.8	V	
Leak current	I _{HL}	Stop			±10	μA	
Output saturation voltage (sink plus source)	V _{sat1}	I _O =0.35A, V _{CC} =4.2V		1.2	1.4	V	
	V _{sat2}	I _O =0.70A, V _{CC} =4.2V		1.5	2.0	V	
Output leak current	I _{OL}				±1.0	mA	
Current limiter	V _{ref1}		0.27	0.30	0.33	V	
Control amplifier voltage gain	G _C			-6		dB	
Voltage gain phase differential	ΔG _C				±1	dB	
Integrated amplifier internal reference voltage	V _{ref2}			V _{CC} /2		V	
Integrated amplifier bias current	I _{ib}				±1	μA	
Integrated output voltage amplitude	V _i ⁺	I _i =-0.5mA with reference of V _{ref2}		0.75		V	
	V _i ⁻	I _i =0.5mA with reference of V _{ref2}		-1.4		V	
Gain band width				1000		kHz	*
FG amplifier input voltage range	V _{FG}		5		100	mVp-p	
FG amplifier voltage gain	G _{FG}	Open loop		60		dB	
FG amplifier input offset	V _{FG0}				±10	mV	
FG amplifier internal reference voltage	V _{FGB}		2.20	2.50	2.80	V	
Schmitt hysteresis width	ΔV _{sh1}	High→Low		25		mV	*
	ΔV _{sh2}	Low→High		25		mV	*
Schmitt input operation level	V _{sh}		1		V _{CC} -1	V	
Speed disk recount number	N			1042			
Disk recount out low level voltage	V _{DL}	I _D =-0.5mA			0.3	V	
Disk recount out high level voltage	V _{DH}	I _D =0.5mA	V _{CC} -0.4			V	
Disk recount out leak current	I _{D1}				±1.0	μA	
Disk recount operation frequency	F _D				1.0	MHz	*
Oscillation range	F _{OSC}				1.0	MHz	*
Index bias current	I _{IDB}				±10	μA	
In-phase input voltage range	V _{ID}		1.5		V _{CC} -0.5	V	
Hysteresis setting current range	I _{IDO}		5	10	15	μA	
Index output low level voltage	V _{IDL}	V _{ID} =5V			0.4	V	
Index output high level voltage	V _{IDH}	V _{ID} =5V	4.5			V	
Brak-down voltage	V _{DLDC}	V _{ID} =5V		2.50		V	
Delay output low level voltage	V _{DLL}	V _{ID} =5V			0.4	V	
Delay output high level voltage	V _{DLH}	V _{ID} =5V	4.5			V	
Thermal shutdown operating temperature	TSD		150	180		°C	*
Hysteresis width	ΔTSD			40		°C	*

Note : *) Marked values are guaranteed by the design itself and therefore do not require measurement.

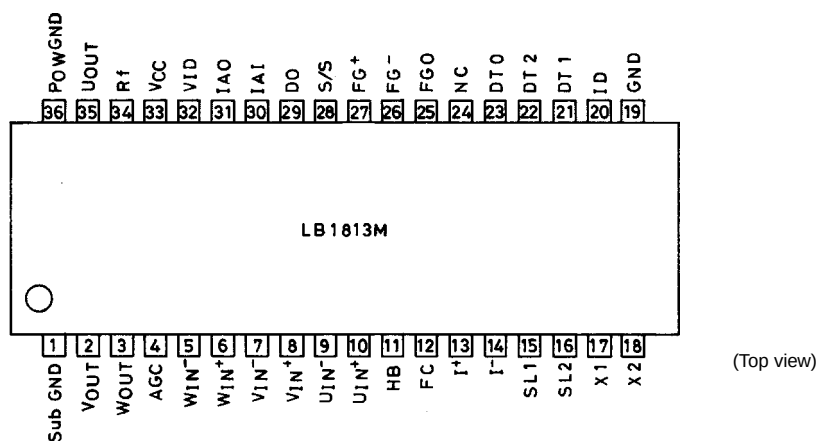
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Block Diagram



Unit (reissitace : Ω , capacitance : F)

Pin Assignment



(Top view)

Truth Table

	Source→Sink	Hall-Effect Input		
		U	V	W
1	V-phase →W-phase	H	H	L
2	V-phase →U-phase	L	H	L
3	W-phase →U-phase	L	H	H
4	W-phase →V-phase	L	L	H
5	U-phase →V-phase	H	L	H
6	U-phase →W-phase	H	L	L

When an high level exists for Hall-effect input.

$U^+ > U^-$
 $V^+ > V^-$
 $W^+ > W^-$

Pin Description

Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function									
5 6 7 8 9 10	W ⁻ W ⁺ V ⁻ V ⁺ U ⁻ U ⁺	2.2V min V _{CC} -0.7V max		- W-phase Hall-effect input pin. W⁺>W⁻ is established when logic is at an high level. - V-phase Hall-effect input pin. V⁺>V⁻ is established when logic is at an high level. - U-phase Hall-effect input pin. U⁺>U⁻ is established when logic is at an high level.									
11	HB	1.5V typ I _H =5mA		Minus pin for Hall-effect bias, When stopped, switches open and Hall-effect bias severs.									
12	FC			Frequency characteristics revision pin. By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.									
13 14	I ⁺ I ⁻	1.5V typ V _{CC} -0.5V max		Index input pin. When the I⁺ pin is at an low level, I1 operates with the fixed current of I1=10μA and when at an high level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I⁺ pin.									
15	SL1	High : 2.0V min Low : 0.8V max		Time changeover pin. fosc=1MHz <table border="1"><tr><th>SL2 \ SL1</th><th>H</th><th>L</th></tr><tr><th>H</th><td>600rpm</td><td>300rpm</td></tr><tr><th>L</th><td>720rpm</td><td>360rpm</td></tr></table> FG : 60pulse/round	SL2 \ SL1	H	L	H	600rpm	300rpm	L	720rpm	360rpm
SL2 \ SL1	H	L											
H	600rpm	300rpm											
L	720rpm	360rpm											
16	SL2	High : 2.0V min Low : 0.8V max											

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Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
17	X1			• Reference clock generating pin.
18	X2			
19	GND			• Ground pin. Grounded as with pins 1 and 36.
20	ID	High : 4.5V min Low : 0.4V max (When $V_{ID}=5V$)		• Index pulse output pin.
21	DT1			• Pin Connecting the external CR for the delay time constant circuit.
22	DT2			• Break-down current setting pin for the delay time constant circuit.
23	DTO	High : 4.5V min Low : 0.4V max (When $V_{ID}=5V$)		• Index delay pulse output pin.
25	FG0			• FG amplifier output pin.
26	FG ⁻			• FG amplifier negative input pin.
27	FG ⁺	2.48V (When $V_{ID}=5V$)		• FG amplifier positive input pin. Generates reference voltage within IC.

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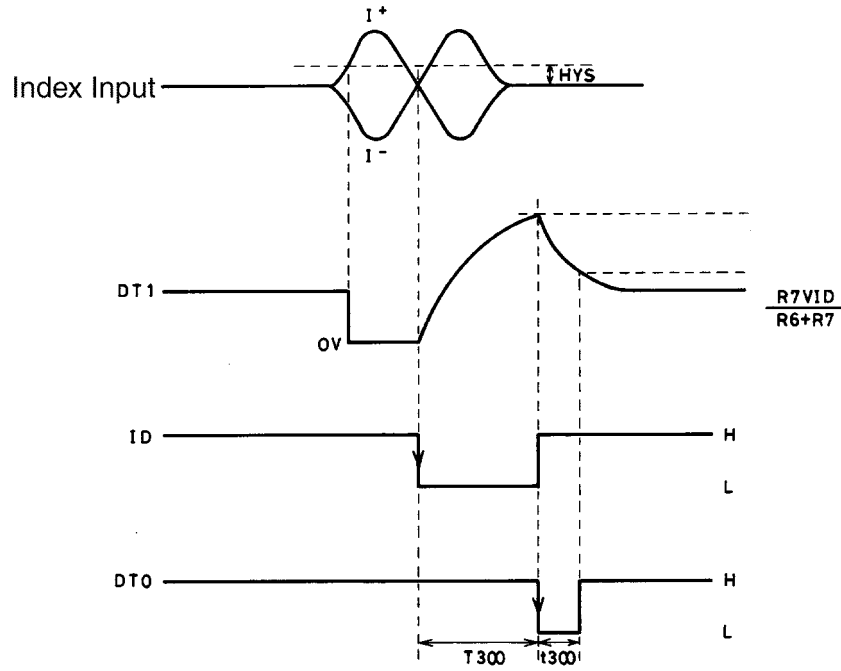
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Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
28	S/S	High : 2.0V min Low : 0.8V max		Start/Stop changeover pin. Low level active.
29	DO			Speed discriminator output pin.
30	IAI			Integrated amplifier input pin.
31	IAO			Integrated amplifier output pin.
32	VID			Index pulse output and index delay pulse output power supply pin. For applications when V_{CC} equals 5V, $V_{CC}=V_{ID}=5V$.
33	V_{CC}			Total power supply voltage pin except for V_{ID}. Voltage must be stable and free of ripple and noise interference.
34	R_f			Output current detection pin. By installing an R_f resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin activates the current limiter.
35	U_{OUT}			U-phase output pin.
36	Pow GND			Output transistor ground pin.
1	Sub GND			Ground pin. Ground as with pins 19 and 36.
2	V_{OUT}			V-phase output pin.
3	W_{OUT}			W-phase output pin.
4	AGC			AGC (Automatic gain control) pin. Confrds Hall-effect amplifier gain in response to Hall-effect input-frequency.

Index and Timing Chart



When SL1=high level

$$\cdot T300 \approx 0.693CR6$$

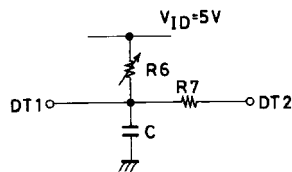
$$\cdot t300 \approx \frac{CR6R7}{R6+R7} \left\{ 0.405 + \ln \left(\frac{R6-R7}{R6-2R7} \right) \right\}$$

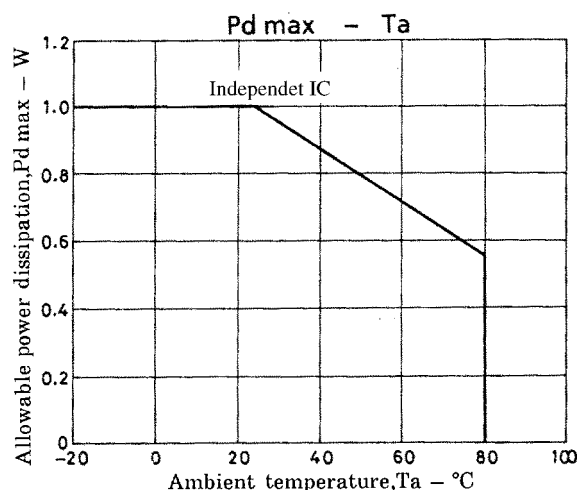
When SL1=low level.

$$\cdot T360 \approx 0.577CR6$$

$$\cdot t360 \approx \frac{CR6R7}{R6+R7} \left\{ 0.522 + \ln \left(\frac{0.781R6-R7}{R6-2R7} \right) \right\}$$

Using only the ID pulse involves shorting DT1 and DT2.





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