PM5347

Suggestions for S/UNI-155-PLUS Board Layout

Issue 2: September, 1997

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SUGGESTIONS FOR S/UNI-PLUS BOARD LAYOUT:

(1) Decoupling Capacitors on Analog Power

Decoupling capacitors (0.1 µF Ceramic X7R) are recommended for each analog power pin (TAVD1, TAVD2, TAVD3, TXVDD, RAVD1, RAVD2, RAVD3, RAVD4) placed as close to the package pin as possible according to the layout recommendation in figure 1 below. **In particular, separate decoupling capacitors are strongly recommended for the TAVD1, TAVD2, RAVD1 and RAVD2 pins.** Separate decoupling is recommended to prevent transmit from coupling transient noise into the receiver. TAVD1 and RAVD1 are power supplies for voltage reference circuitry for the transmit and receive PLLs respectively. There must be separate decoupling of TAVD2 from TAVD1; RAVD2 must be separately decoupled from RAVD1. This prohibits transients from coupling into the references (i.e., RAVD1 and TAVD1).

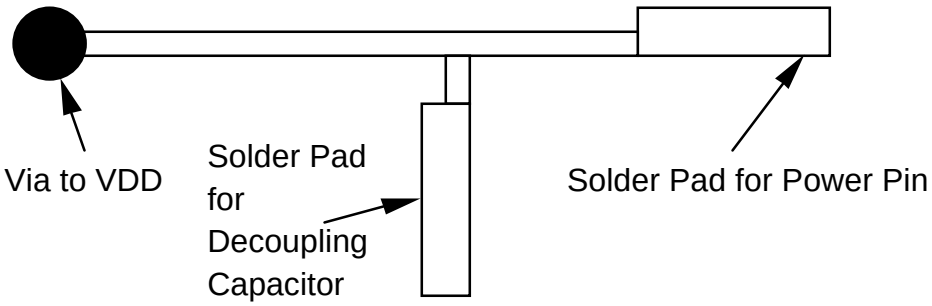
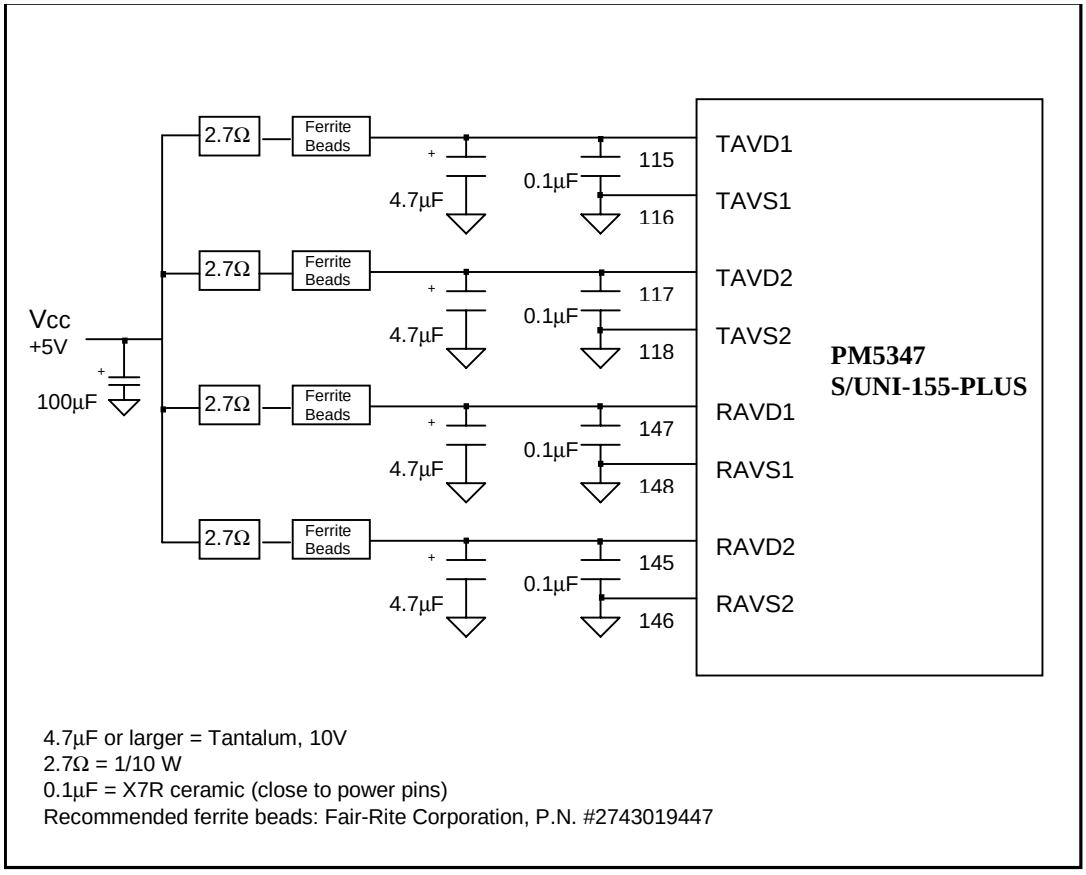


Fig. 1: Recommended Layout for VDD Decoupling Connection to Analog Power Pins

It is also desirable to include a low frequency power supply filter circuit especially if the S/UNI-PLUS is powered by a switching power supply. The circuit below is recommended for reducing noise seen by the S/UNI-PLUS analog power pins, TAVD1, TAVD2, RAVD1, and RAVD2. Ferrite beads are recommended for high frequency noise protection.



(2) Power and Ground Connections

In a 4 layer board, when only two planes are available for power and ground, it is advisable to separate the S/UNI-PLUS transmit power/ground pins from the receive power/ground pins by splitting[1] the power and ground planes in the area surrounding these pins as shown in figure 2.

Alternatively, when more planes are available on the PCB, the best methodology for power supply connection is to provide a separate plane for each of the transmit analog power/ground pins, receive analog power/ground pins and the digital power/ground pins. In such a case, no plane cuts are necessary to form isolated analog power and ground areas.

[1] The isolation of the power and ground planes as recommended in figure 2 is based on the experience PMC-Sierra has gained in developing reference designs based on the S/UNI-LITE.

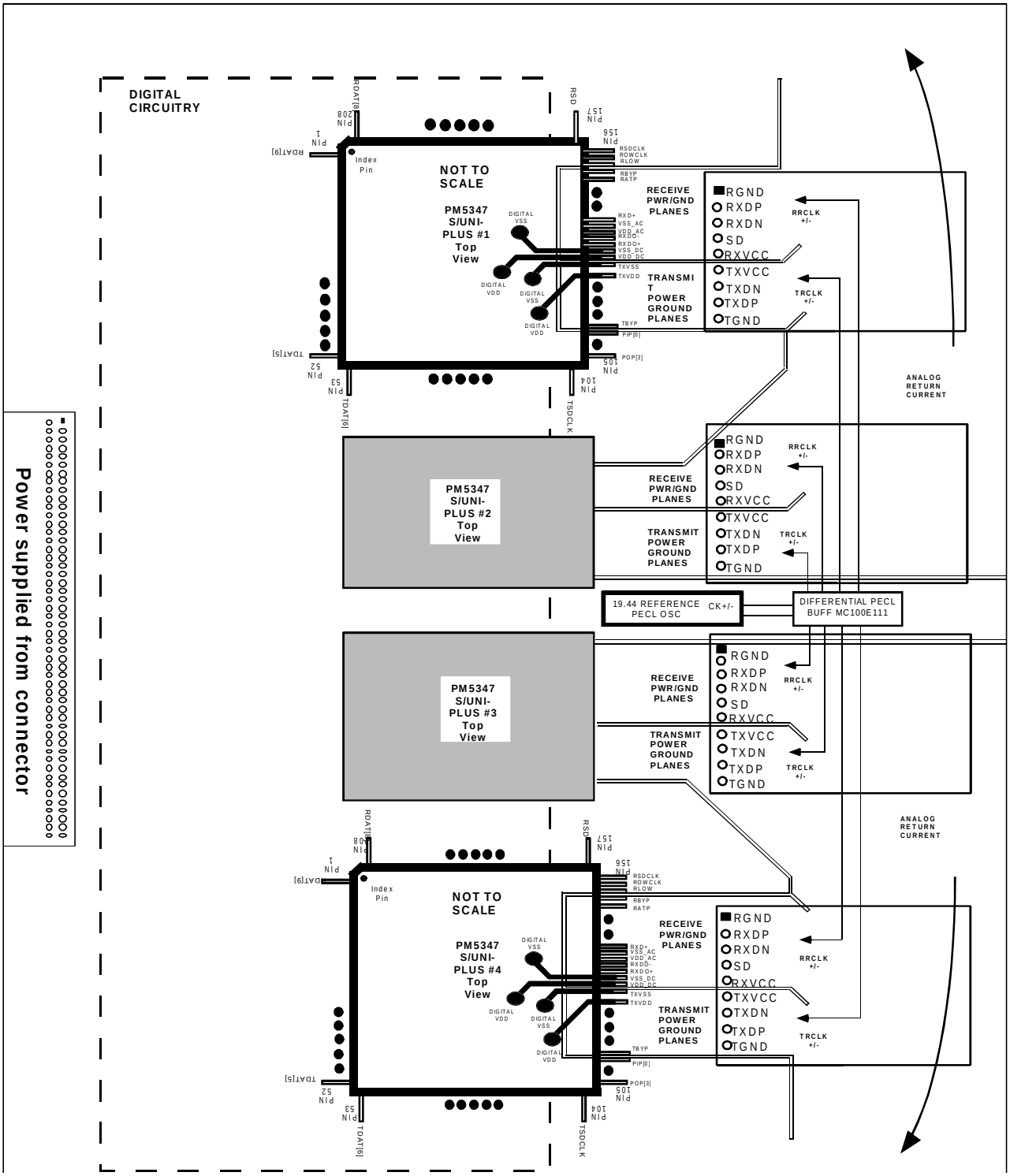


Figure 2: Recommended Layout & Power/Ground Plane Isolation On a Limited Layer Board.

The general high speed layout of the devices should remain the same as shown in figure 2, keeping the analog and digital circuitry segregated away from each other. As an example, the top layer can be assigned to Receive analog signals and the bottom layer can be assigned to Transmit analog signals. Digital signals can be assigned to all signal layers taking care not to traverse over or close to sensitive analog signals. The second and third layers can be assigned to Receive analog ground and Receive analog power respectively. Similarly, the two layers adjacent to the bottom layer can be assigned to Transmit analog power and ground (with the ground layer being closest to the bottom layer). The digital power and ground layers should be assigned to some layers in the middle. The exact details of this configuration are shown in figure 3. Note that the transmit signals (routed on the bottom layer) need to via up to the S/UNI-PLUS creating a discontinuity in the controlled impedance transmission lines. This in turn has a detrimental effect on the signal quality on the transmit stream. The degradation due to a single vias placed at the end of the trace is tolerable but any additional vias placed along the same trace may increase the degradation to an intolerable level.

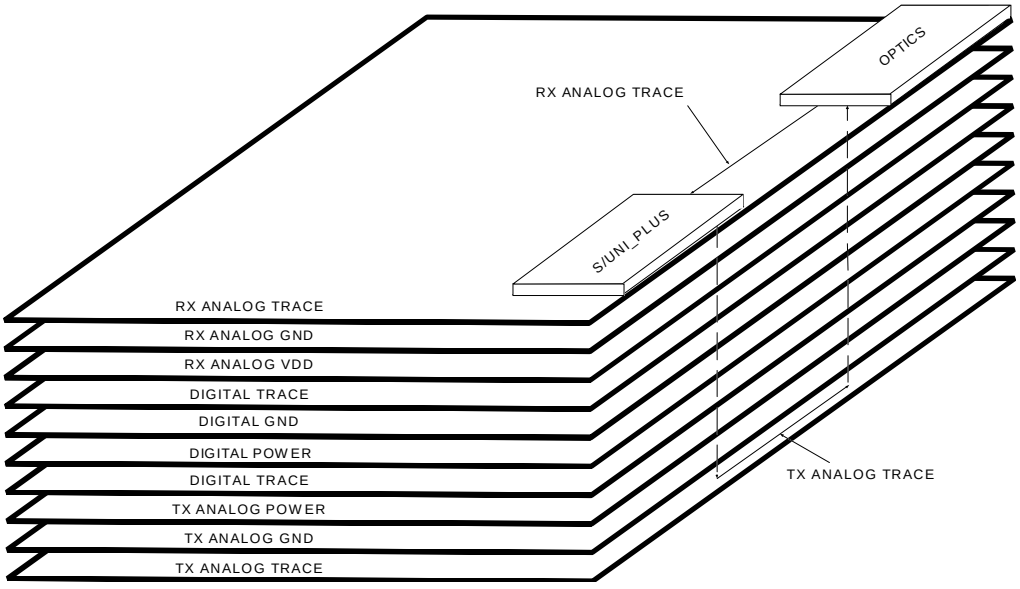


Figure 3: Recommended Power/Ground Plane Connection on a Ten Layer Board

Generally, Power and Ground requirements are a function of the noise environment on a board and the performance target of the board. Ground and power supply noise will degrade the bit error performance of the S/UNI-PLUS and introduce intrinsic jitter on the transmitted data. Table 1 is a summary of all power and ground connections for the S/UNI-PLUS. The “Supply Noise Sensitivity” column highlights pins that are sensitive to perturbations on the supply rails. The “Current” column identifies the current consumption for a particular pin as either dynamic (fluctuating over time) or static (constant over time). The “Layout Consideration” column provides further detail regarding the layout requirements for each pin.

Table 1: S/UNI-PLUS Power/Ground Pins

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
RAVS1	Ground	High	Static	148	The ground (RAVS1) pin for analog voltage reference circuitry
RAVS2	Ground	High	Dynamic	146	The ground (RAVS2) pin for receive loop filter and VCO.
RAVS3	Ground	High	Dynamic	139	The ground (RAVS3) pin for the RXD+/- & ALOS+/- PECL inputs.
RAVS4	Ground	High	Dynamic	144	The ground (RAVS4) pin for the RRCLK+/- PECL inputs.
TAVS1	Ground	High	Static	116	The ground (TAVS1) pin for analog voltage reference circuitry
TAVS2	Ground	High	Dynamic	118	The ground (TAVS2) pin for the transmit clock synthesizer VCO.
TAVS3	Ground	High	Dynamic	122	The ground (TAVS3) pin for the transmit PECL (TRCLK+/-) Inputs.
TXVSS	Ground	High	Dynamic	128	The transmit pad ground (TXVSS) is the return path for the TXC+/- and TXD+/- outputs. TXVSS is physically isolated from the other device ground pins and should be noise free for good performance.
VSS_DC1 VSS_DC2 VSS_DC3 VSS_DC4 VSS_DC5 VSS_DC6 VSS_DC7 VSS_DC8 VSS_DC9 VSS_DC10 VSS_DC11	Ground	Low	Dynamic	8 30 38 61 79 99 130 161 178 198 207	The core ground (VSSI1 – VSSI3) pins should be connected to GND in common with VSS_AC1 to VSS_AC8.

VSS_AC1 VSS_AC2 VSS_AC3 VSS_AC4 VSS_AC5 VSS_AC6 VSS_AC7 VSS_AC8	Ground	Low	Dynamic	5 34 83 100 134 166 184 201	The pad ring ground (VSS_AC1 - VSS_AC8) pins should be connected to GND in common with VSS_DC1 to VSS_DC11.

Table 1: S/UNI-PLUS Power/Ground Pins - cont'd

Pin Name	Type	Supply Noise Sensitivity	Current	Pin No.	Layout Consideration
RAVD1	Power	High	Static	147	The power (RAVD1) pin for analog voltage reference circuitry.
RAVD2	Power	High	Dynamic	145	The power (RAVD2) pin for receive loop filter and VCO.
RAVD3	Power	High	Dynamic	140	The power (RAVD3) pin for the RXD+/- and ALOS+/- PECL inputs.
RAVD4	Power	High	Dynamic	141	The power (RAVD4) pin for the RRCLK+/- PECL inputs.
TAVD1	Power	High	Static	115	The power (TAVD1) pin for analog voltage reference circuitry.
TAVD2	Power	High	Dynamic	117	The power (TAVD2) pin for the transmit clock synthesizer VCO.
TAVD3	Power	High	Dynamic	119	The power (TAVD3) pin for the transmit PECL inputs.
TXVDD	Power	High	Dynamic	123	The transmit pad power (TXVDD) supplies the TXC+/- and TXD+/- outputs. TXVDD is physically isolated from the other device power pins and should be a well regulated +5 V DC and noise free for good performance.
VDD_DC1 VDD_DC2 VDD_DC3 VDD_DC4 VDD_DC5 VDD_DC6 VDD_DC7 VDD_DC8 VDD_DC9 VDD_DC10 VDD_DC11	Power	Low	Dynamic	7 29 37 60 80 98 129 160 177 197 206	The core power (VDD_DC1 - VDD_DC11) pins should be connected to a well decoupled +5 V DC in common with VDD_AC.

VDD_AC1 VDD_AC2 VDD_AC3 VDD_AC4 VDD_AC5 VDD_AC6 VDD_AC7 VDD_AC8	Power	Low	Dynamic	4 33 82 97 133 165 183 200	The pad ring power (VDD_AC1 - VDD_AC8) pins should be connected to a well decoupled +5 V DC in common with VDD_DC.

(3) Ferrite Beads on Digital Power Supply

Power supply isolation using Ferrite beads is not advisable in digital switching circuits as dI/dt noise is introduced into the power rail. Sufficient capacitive decoupling on all digital power pins is recommended.

(4) Ferrite Beads on Analog Power Supply

Ferrite beads for power supply isolation can be used in analog (and ECL) circuitry where there is no dI/dt noise due to single ended switching currents. If this is not the case, or it is uncertain that the circuitry is operating in a balanced fashion, then using RC filtering or local bulk decoupling to filter local dI/dt noise is recommended.

(5) Regulating the Analog Power Supply (Optional)

In applications that provide a +12V supply, a 5V regulator can be used to supply a low-noise analog power supply. The regulator should supply all analog power pins (TAVD1-4 and RAVD1-4); the total current draw of the analog circuitry in the S/UNI-PLUS is less than 30mA. At a minimum, the regulator should power RAVD1, RAVD2, TAVD1, and TAVD2.

(6) Analog Test Pins

The Analog test pins must be grounded. RATP should be connected to the Receive analog ground plane. TATP should be connected to the Transmit analog ground plane.

(7) Loop Filter Components

The loop filter components should be placed such that they sit over the Receive analog ground plane. In a design using multiple S/UNI-PLUS's, the loop filter components should be placed on the Receive analog ground plane of the S/UNI-PLUS that they connect to.

(8) Unused Input Pins

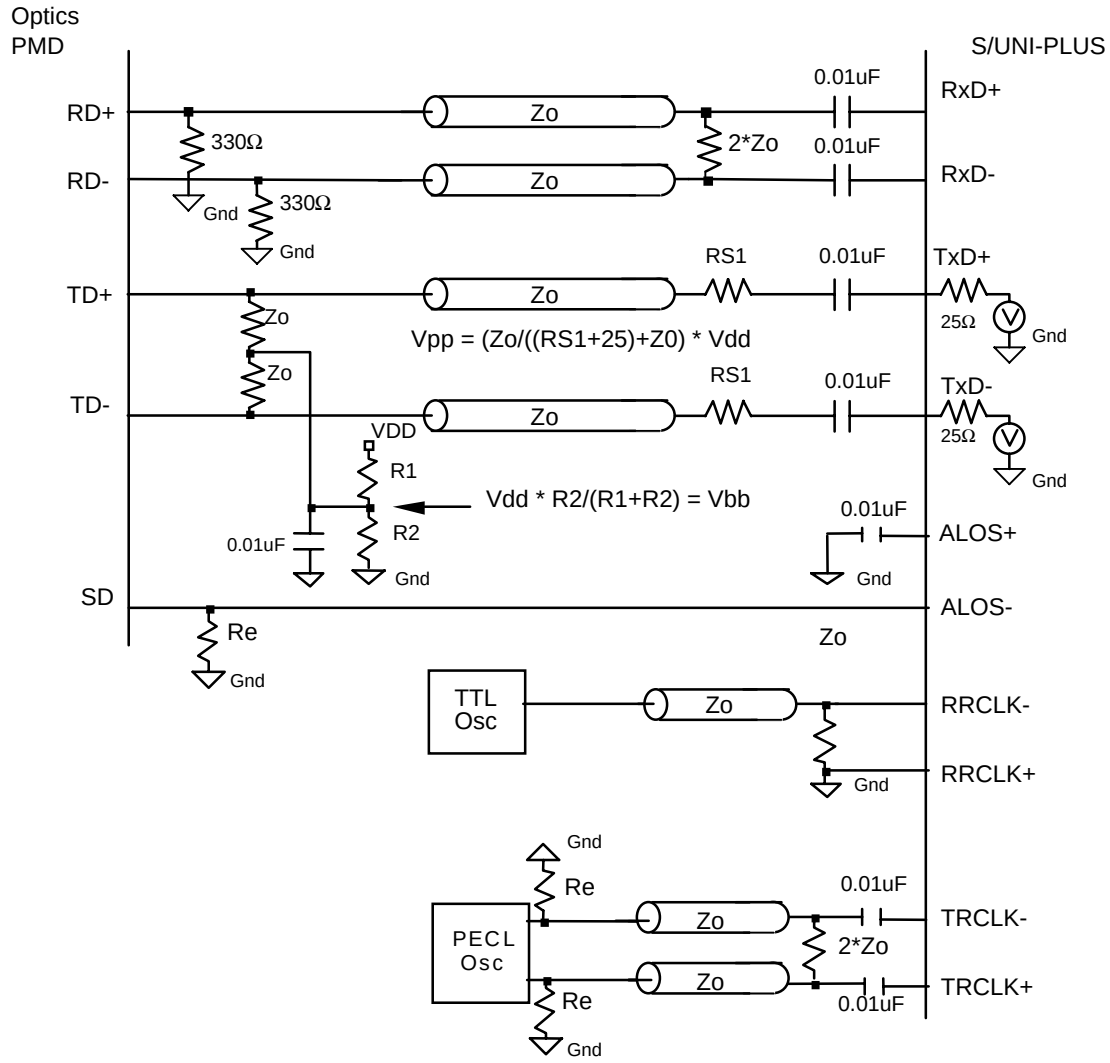
All unused input pins should be tied to their appropriate inactive level.

(9) Dealing with high-speed return currents

At low speeds, return current follows the path of least resistance back to the driver. At high speeds, however, the return current follows the path of least inductance which lies on the plane directly under the signal trace, as the total loop area between the outgoing and returning paths is minimized. In other words, the high-speed return current follows a path that is almost the "mirror image" of the signal trace on the plane underneath the trace. This tight coupling provides good flux cancellation so that common-mode current is reduced. High speed traces should not cross cuts or heavily perforated areas (where tight spacing through-hole components reside) on the power and ground planes, as any cuts on these planes may interrupt the return currents, causing them to seek alternative paths back to the driver. The different routes taken by the outgoing and return currents will both induce common-mode noise on other nearby signal traces. In addition, by routing high speed signals over continuous power planes, the return current paths of these signals are known and other signals will not cross over these return currents, reducing the possibility of noise coupling. Detailed discussions on high-speed design are provided by the references.

SUGGESTIONS FOR S/UNI-PLUS PECL TERMINATIONS:

(1) S/UNI-PLUS to PMD and Reference Oscillator Terminations



Notes: Vpp is minimum input swing required by the optical PMD device.

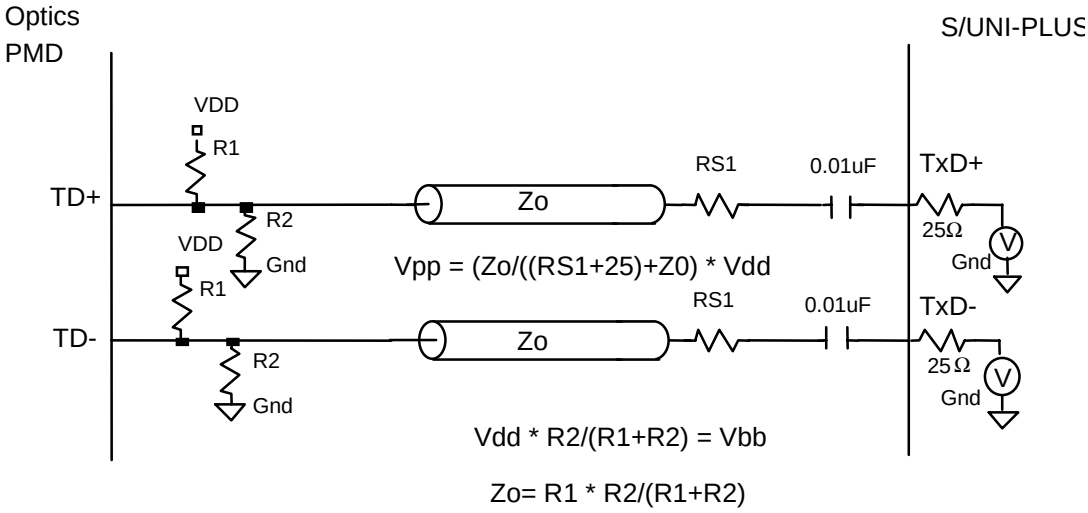
Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)
Vpp is Voh - Vol (typically 800 mVolts)

The value of Re is dependent on the signal trace characteristic impedence and the ECL or PECL supply voltage (-4.5 V, + 5 V). Values in the range of 200-330 Ω are recommended

A single oscillator can be used to drive both RRCLK and TRCLK. Two interchangable options are shown for the supply of the TRCLK+/- and RRCLK+/- inputs.

(2) S/UNI-PLUS TxD to PMD

The TxD outputs from the S/UNI-PLUS may also use Thévenin termination resistors that provide the Vbb bias voltage rather than the resistor-divider shown above. While this circuit uses one less component (0.01 µF decoupling capacitor), it is more susceptible to common mode noise.

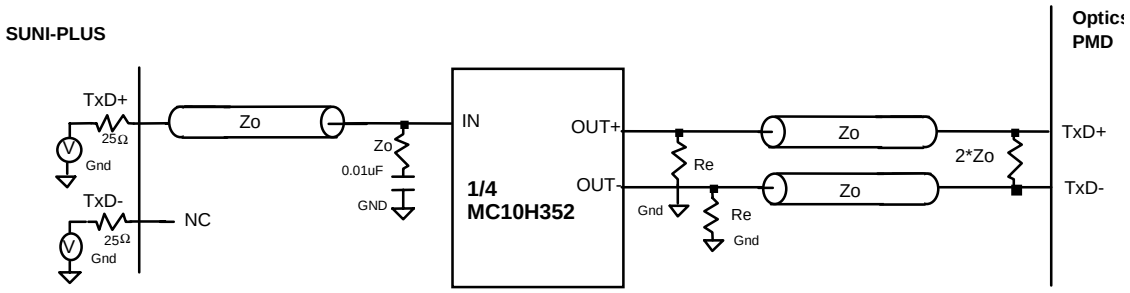


Notes: Vpp is minimum input swing required by the optical PMD device.
Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)
Vpp is Voh - Vol (typically 800 mVolts)

For Zo = 50 Ω, R1=67 Ω, R2 = 192.3 Ω,
RS1=237Ω
Resistor Tolerence ±5%.

(3) S/UNI-PLUS buffered with MC10H352 to PMD and Terminations

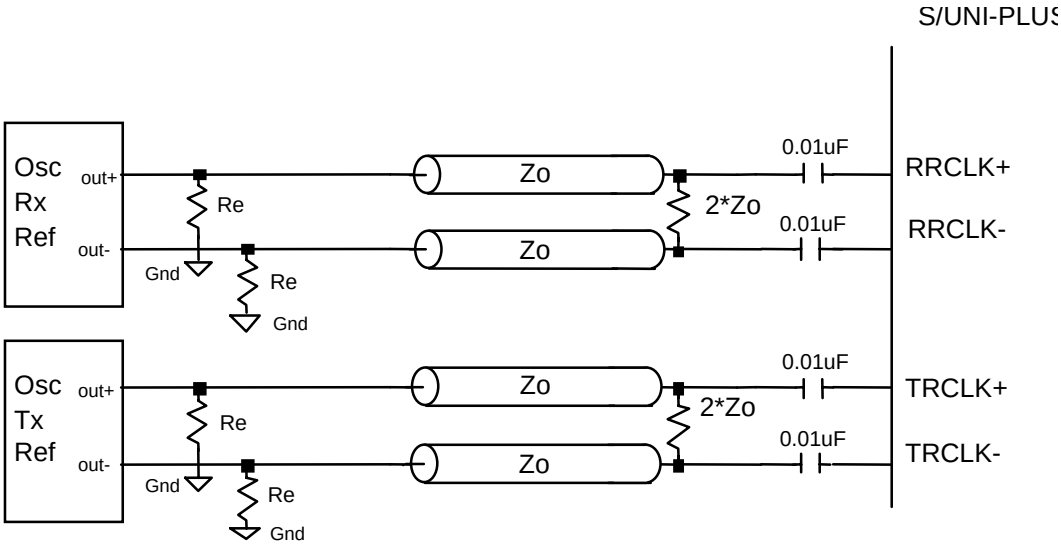
Schemes (1) and (2) above use AC-coupling capacitors on the TXD+/- S/UNI-PLUS outputs. A disadvantage of this scheme is that Diagnostic LOS (DLOS register bit) can no longer be used because the AC-coupled all zero transmit data will cause the PMD inputs to float to the Vbb threshold. This can result in the PMD transmitting pulses due to board noise. A way to eliminate this is to use a CMOS to PECL converter, such as the MC10H352 Quad CMOS to PECL, between the S/UNI-PLUS TXD+/- outputs and the ODL. Make sure the converter is located right at the S/UNI-PLUS TXD output.



The value of Re is dependent on the signal trace characteristic impedence and the ECL or PECL supply voltage (-4.5 V, + 5 V). Values in the range of 330 Ω are recommended

(4) Differential Reference Oscillator Terminations

For optimum jitter performance on the transmit side and noise immunity on the receive side the reference clocks should be connected differentially as shown below.



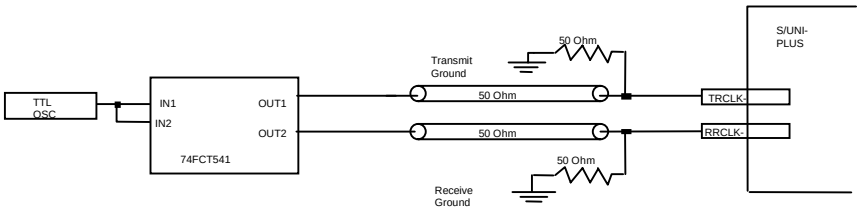
The value of Re is dependent on the signal trace characteristic impedence and the ECL or PECL supply voltage (-4.5 V, + 5 V). Values in the range of 200-330 Ω are recommended

(5) Single TTL/CMOS Oscillator Driving Both RRCLK and TRCLK

If a single TTL or CMOS oscillator is used to drive these inputs, the RRCLK- and TRCLK- inputs can be used while RRCLK+ and TRCLK+ signals are connected to their respective grounds. The single clock signal must be properly terminated, however, it is not a good idea to connect the clock trace to either RRCLK- or TRCLK- and then run the trace to the other input and terminate at the far end. The transmit and receive grounds are isolated by

channels cut into the ground plane, so potential differences between transmit and receive grounds will affect one of the reference clock inputs. For example, if the reference clock signal is run to the TRCLK input and then is terminated to the receive ground near the RRCLK input, the TRCLK input (which is referenced to the transmit ground) will require the clock swing to be large enough to accommodate the difference between grounds. Otherwise, the TRCLK input will be more sensitive to noise than the RRCLK input. A second problem may arise if the clock signal trace crosses the cuts in the ground plane (i.e. from transmit ground island to receive ground island). In that case the ground return current from the receive side cannot follow the signal trace back to the driver. Instead, it will seek an alternative path of least inductance. Consequently, this ground current will induce common-mode noise on signals nearby.

The solution is to run two separate reference clock signals and terminate them at each input[2]. The following diagram illustrates how to use a single TTL level oscillator to drive the RRCLK- & TRCLK- signals via a 74FCT541 buffer. The TRCLK+ and RRCLK+ signals are connected to their respective grounds.



The TTL oscillator should be placed as close to the buffer as possible as it is unterminated. The TTL oscillator is used to match the 74FCT541's TTL input level in order to avoid duty cycle distortion caused by differences in output levels and input switching thresholds.

(6) Internal Selection of Transmit Timing Reference Clock

A final option is to provide a reference clock input as shown in option 4 or 5 above and to program the S/UNI-PLUS such that the source of the transmit reference clock is from the receive RRCLK+/- inputs. In order to select the RRCLK+/- inputs as the master timing reference for the transmit circuitry, the TTIME[1:0] bits must be set to binary 01.

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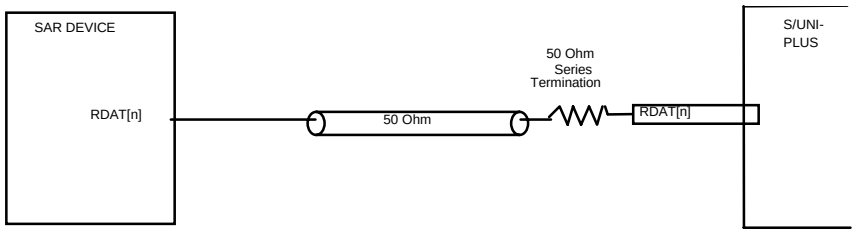
[2] A layout alternative could be to run a 50 ohm clock trace to the vicinity of the RRCLK- & TRCLK- inputs and then split into two 100 ohm traces. Each one of these two traces could then be connected to the RRCLK- or TRCLK- input and each terminated with 100 ohm to the receive or transmit analog ground respectively. However, this is not recommended because the resulting width of a 100 Ohm trace is very narrow (less than 3 mil). This width will be difficult for board manufacturers to fabricate accurately and reliably. Inaccuracy in the trace impedance will cause the signals to be improperly terminated.

S/UNI-PLUS SCI-PHY BUS TERMINATIONS

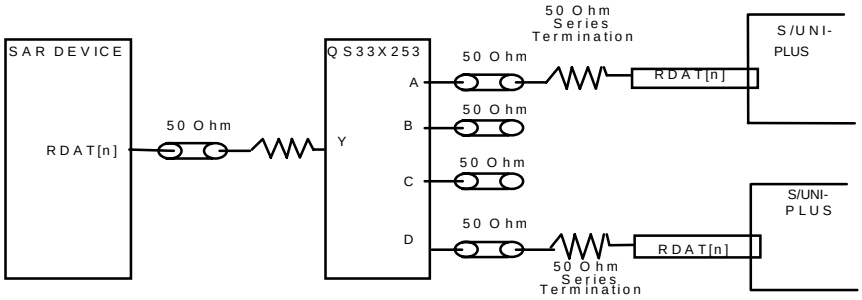
Terminating The RDAT data Bus.

Transmission line effects on this bus become a problem due to the fast edge rates of the data bus. These effects become more pronounced if the interconnect is long (as is the case when four S/UNI-PLUS's are connected in a multi-phy configuration) or if the interconnect goes off board via connectors. In order to solve this problem the RDAT[15:0] bus must be appropriately terminated.

Using the normal termination at the end of the line (50 Ohms or Z_0 to ground) is acceptable for a single signal, but when there are 16 such signals terminated in this way the DC current draw can be in the order of 1.6 Amps. This is unacceptable since the S/UNI-PLUS package cannot tolerate such a power draw. Therefore an alternative termination scheme must be used. PMC-Sierra has chosen series termination after evaluating various techniques through spice simulation. To implement this scheme, the design must control the RDAT bus characteristic impedance (Z_0) and the signal should include a series resistor of the same value at the source end as shown in the next diagram.



A modified version of this termination scheme must be used when a multi-phy SAR bus is connected to more than one S/UNI-PLUS. This is shown in the next diagram.



The QS33X253 acts like a 4-1 multiplexer and each interconnect can be thought of as a single point to point connection terminated by a series resistor.

The series resistor value shown in the diagrams assumes that the output resistence of the drivers is zero. In practice, the series resistor must be less than the value shown by an amount equal to the inherent output resistance of the output drivers.

S/UNI-PLUS CLOCK RECOVERY LOOP FILTER COMPONENTS:

Loop Filter Components[4] .

The loop filter values were chosen to achieve maximum jitter transfer and jitter tolerance performance for the WAN environment.

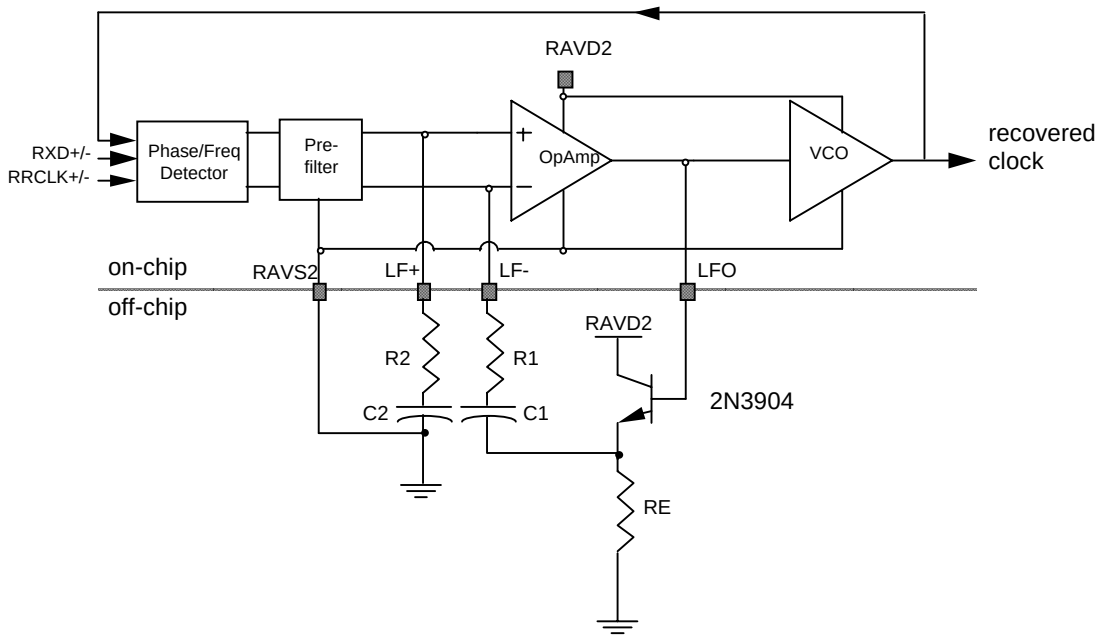
All resistors are 1% metal film (1/8 watt) resistors and all capacitors should be 10% non-polarized capacitors. These capacitors should be non-polarized to avoid being reverse biased at approximately 2.0V while the S/UNI-PLUS is held in reset. Therefore, X7R monolithic ceramic capacitors are recommended for values 15µF and 4.7µF. Ceramic surface mount capacitors for these values are available from ATC, AVX, muRata, and NEC.

Table 2 - Recommended Component Values

Line Rate (Mbit/s)	R1 (Ω ± 1%)	R2 (Ω ± 1%)	C1, C2 (µF) min	RE (Ω +/- 1%)
155.52	68.1	90.9	4.7	100
51.84	68.1	90.9	15	100

A 15 µF capacitor (or higher) is recommended so that the same loop filter values can be used for both the 155.52 Mbit/s and the 51.84 Mbit/s rates. If only a 155.52 Mbit/s line rate is used, the capacitor value can be reduced to 4.7µF (since this may be easier to get than the higher values) and the jitter transfer peaking will still be below the 0.1 dB level.

4 These loop filter values are preliminary, based on the testing performed on a S/UNI-PLUS prototype device. These values may change once characterization has been completed on a production quality S/UNI-PLUS device.



The capacitor values are the minimum recommended values; larger values of capacitance can be used on any of the line rates without affecting performance of the SUNI-PLUS.

REFERENCES

1) PMC-Sierra, Inc., PM5347 S/UNI-PLUS Data Sheet, Issue 4, September, 1995.

2) Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", Second Edition, John Wiley & Sons.

3) Montrose, Mark I., "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press, 1995.

4) Graham, Martin and Johnson, Howard W., "High-Speed Digital Design: A Handbook of Black Magic", PRT Prentice-Hall Inc, 1993.

NOTES

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