PM5948

S/UNI-155-DUAL™

DART BOARD

S/UNI-DUAL ATM REFERENCE TRANSCEIVER BOARD

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CONTENTS

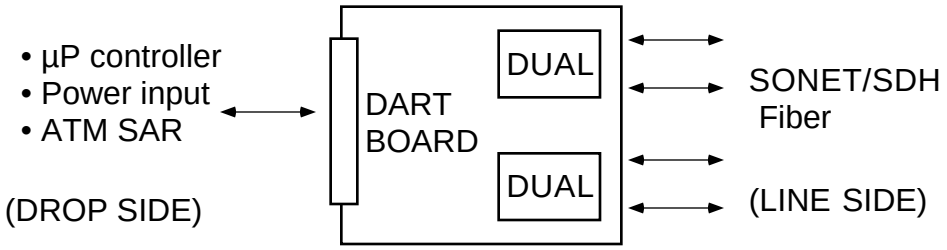
1. OVERVIEW

The DART board is a 6 layer PCB subassembly that contains two PM5348 S/UNI-DUAL IC's, 19.44 MHz crystal oscillator clock reference, power supply decoupling, fiber optic transceiver devices and a 140 pin drop-side system connector.

These devices are typically used to implement the core of an ATM user Network Interface. Each PM5348 contains two logical ATM interfaces, and therefore the DART board has a total of four such ATM SONET/SDH interfaces.

The board also contains the optical serial fiber transceivers. For normal operation, the optical RX/TX fiber and the 140-pin edge connector (to the local µP controller, and the drop side assembly/disassembly SAR) are required.

Fig. 1 DART board overview



This 6 layer PCB contains two S/UNI-DUAL PM5348 chips. On the line side, each S/UNI-DUAL processes two, full duplex ATM packed, SONET/SDH 155 Mbit/s STS-3c/STM-1, or 51.8 Mbit/s (STS-2) data streams. This gives four logical ATM devices, each operating up to 155 Mbit/s in both receive and transmit directions for a board aggregate full duplex rate of 622 Mbit/s.

The line side requires a stable 19.44 MHz (or 6.48 MHz for STS-2) reference clock to both PM5348 ICs. Clock jitter must be carefully controlled and, depending on the design, special attention must be given to buffers, propagation delays, clock skew, power supply decoupling, trace impedance and termination.

The drop side provides a Saturn a Compliant Interface - PHYsical layer (SCI-PHY) 16-bit Rx and 16 bit Tx bus. It may be clocked up to 50 MHz for an aggregate parallel transfer bandwidth of 800 megabits (16 bits x 50 MHz) in both receive and transmit directions.

Configuration, control and status monitoring of the two S/UNI-DUAL chips is accomplished via the 140 pin connector using an 8-bit microcontroller on the external motherboard controller.

2. DART board IMPLEMENTATION

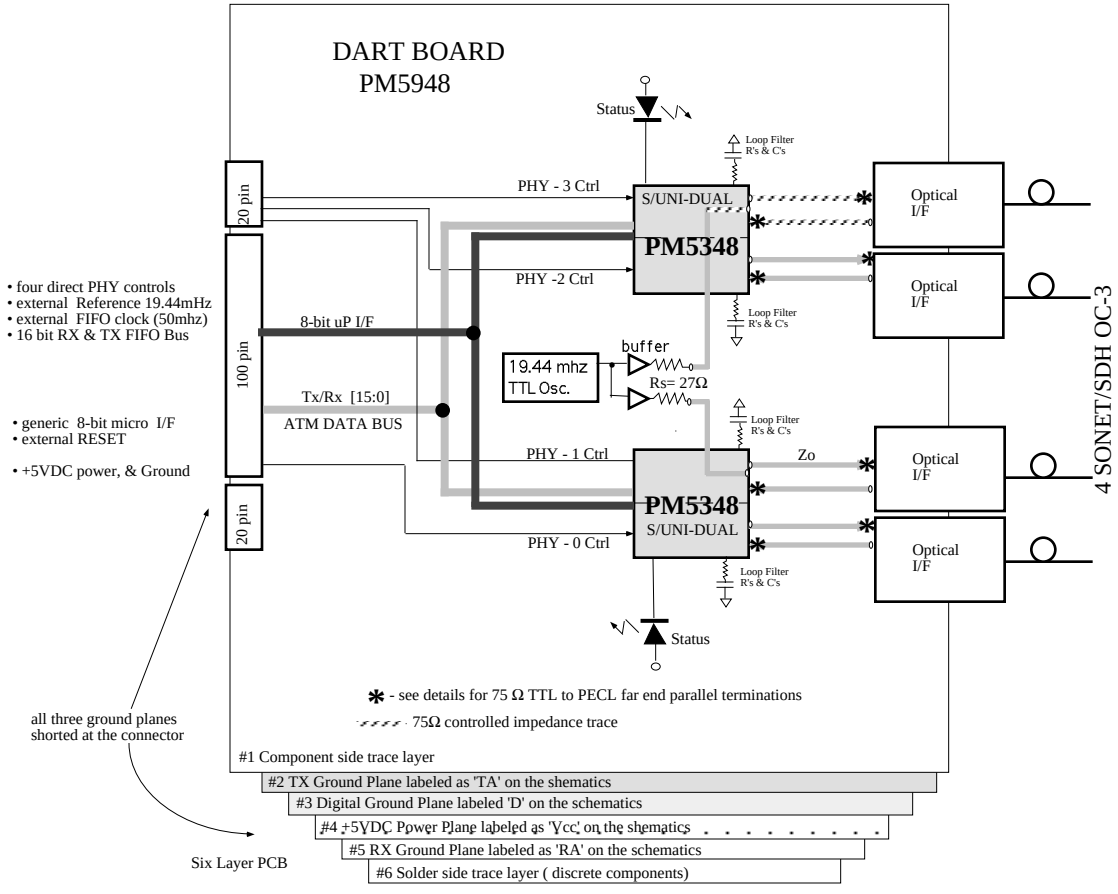
2.1. Important implementation principles

To reduce digital and analog power/ground noise on the DART board, a multi-layer PCB with three ground planes is required. This simplifies design and reduces time to market. The 19.44 MHz reference TTL (not PECL) oscillator is buffered with a 74FCT541. A series transmission line termination method was used to reduce drive current and system noise.

Transmission line traces of 75Ω characteristic impedance are implemented for the 19.44 Mhz reference clock. A compromise between 50Ω and 100Ω so that the traces are wide enough to be repeatable in manufacturing, and also have a high enough Zo to keep currents as low as possible. The connections used for the 155.52 Mbit/s PECL data, between the DUAL and the PMD, are wider 50Ω traces.

2.2. Block diagram

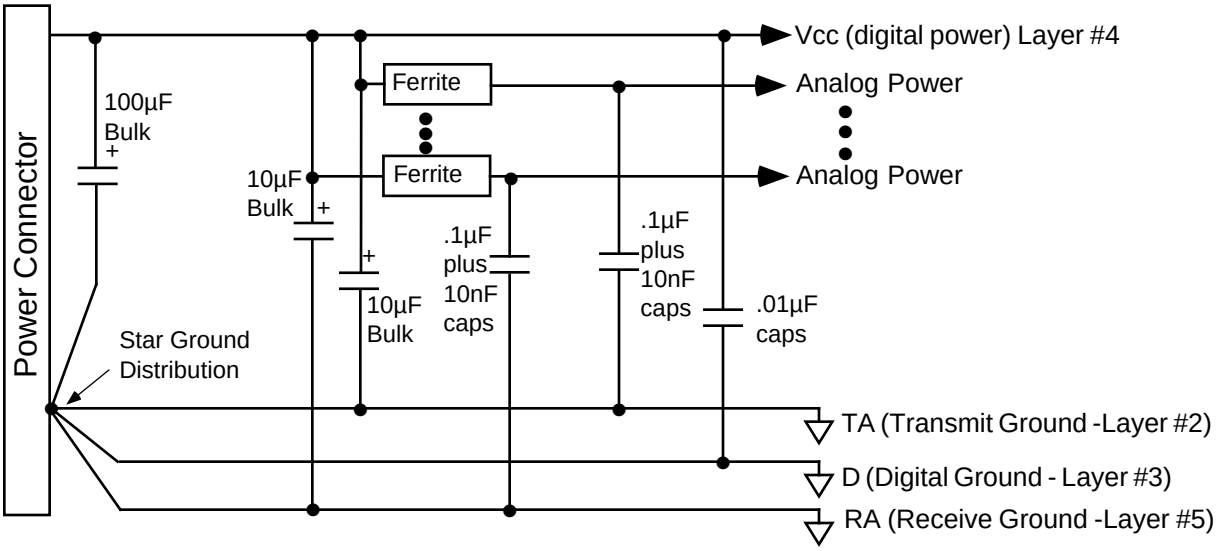
Fig. 2 DART board block diagram



2.3. Power supply and ground layers

The power supply is carefully distributed via power and ground planes. One power plane supplies the digital circuits directly and ferrite series elements are used to generate the other analog supplies. In addition, there are three separate ground planes that originate from the main drop side connector: Digital ground (D), line side Transmit Analog Ground (TA) and line side Receive Analog Ground (RA). To optimize jitter tolerance, the separate ground planes isolate the noisy digital circuits (grounds) from the more sensitive analog receive and transmit blocks.

Fig. 3 Power and ground distribution



2.4. Optical line side interface

The serial line side utilizes four PMD (Physical Media Device) Optical Transceiver modules.

The receive optics are connect directly to the S/UNI-DUAL RXD+/- inputs. To ensure that there is a clock in the absence of optical input, the signal detect (SD) output of the optics is connected to the ALOS- input of the S/UNI-DUAL (the ALOS+ input is grounded). In normal operation (good incoming signal) the S/UNI-DUAL device recovers the clock from the incoming data. In a loss of signal condition, the S/UNI-DUAL will squelch the data on the receive data (RXD+/-) pins and the phase lock loop will switch to the reference clock (19.44 MHz) to keep the recovered clock in range. This technique guarantees that the S/UNI-DUAL will generate a SONET LOS indication if the Optical Transceiver loses optical input.

The transmit line interface consists of the S/UNI-DUAL CMOS transmit outputs which are AC-coupled, attenuated, terminated, level shifted and fed into the transmit optics.

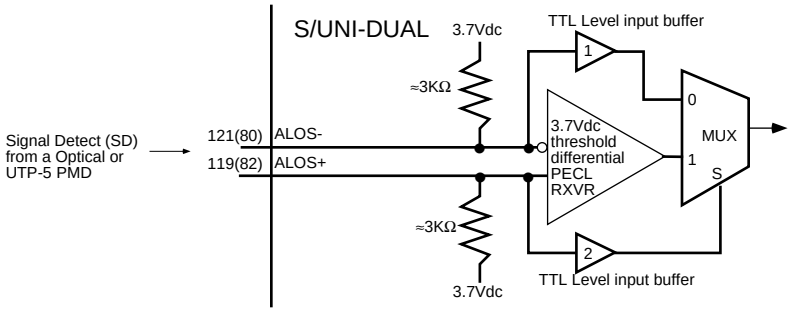
Optical transceivers having a standard 9-pin duplex SC receptacle are used.

In non-loop timed mode, the 155.52 MHz transmit clock source is synthesized from the local 19.44 MHz oscillator and the 155.52 MHz receive clock is recovered from the incoming data.

2.5. ALOS+/- inputs

The S/UNI-DUAL analog Loss Of Signal inputs are designed to accept inputs from either a single ended PECL , balanced differential PECL, or single ended TTL or CMOS voltage source. These are true differential inputs, and they sense the difference between the ± inputs. Grounding the ALOS+ input, causes the ALOS- to be a single ended TTL threshold input. The 3.7V bias is derived internally from power and ground. Since SD (Signal Detect output from Optical Transceiver) is not a high speed signal, it's important, but not critical, that power and ground be in common and noise free with the PMD (Optics or UTP-5 I/F module). TTL threshold level gates are also added and the equivalent input structure looks like this:

Fig. 4 ALOS± block diagram



These inputs would typically receive very slow changing signals. You would not expect SD (Signal Detect outputs from the optical PMD) to be changing a lot during normal operation. If ALOS is asserted, it means there is something drastically wrong with the signal source, (e.g. fiber loop is cut). ALOS a DC function and hence this signal must not be AC coupled. Also since the SD source is not high speed, the ALOS inputs do not require transmission line controlled impedance traces or termination schemes.

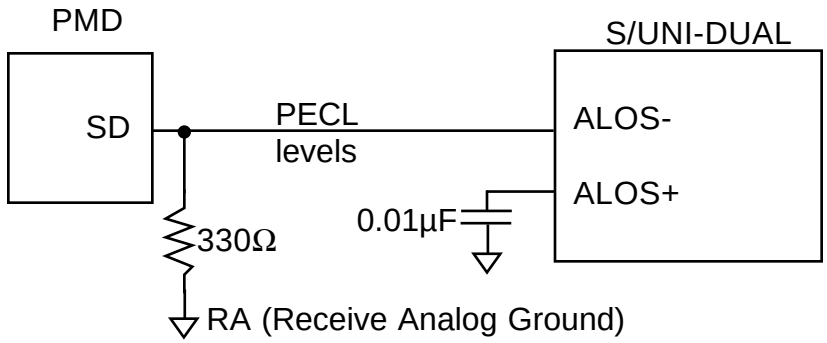
Also connected to these input pins are two gates with their input thresholds set to traditional TTL levels. That is, a low is less than 0.8 V and a high is greater than 2V. To operate the inputs as a single ended TTL threshold inputs, the ALOS+ input must be grounded and the ALOS- pin must be connected to the TTL SD output. In this case, TTL gate #2 detects a logic low at ALOS+ and selects the '1' input which comes from ALOS-.

When operating with PECL, the PECL signal is always >2.0 VDC. Therefore, the TTL gate #2 selects the MUX input '1', which comes from the differential PECL RXVR.

a) Interfacing a single ended PECL SD output (most common)

If the source of SD is a single ended PECL voltage level, then the ALOS+ must be AC coupled to RA (Receive Analog Ground, Layer #5) via a 0.01 µF capacitor, and the SD is connected to the ALOS- input, with the appropriate 330Ω PECL pulldown close to the PMD. Notice that the PMD's analog signal detector output is labeled as SD (Signal Detect). The DUAL's input is labeled ALOS (Analog Loss Of Signal). These have inverse logic labels. However, a logic high means that there is sufficient signal level, and a logic low, means that the input signal is too low.

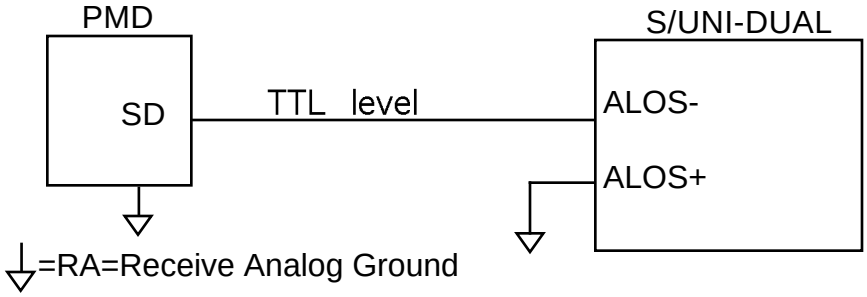
Fig. 5 ALOS- driven from a single ended PECL source



b) Interfacing to a TTL level SD output

A PMD (OPTICS or UTP-5 interface) device with a single ended TTL level SD output can be connected as shown below.

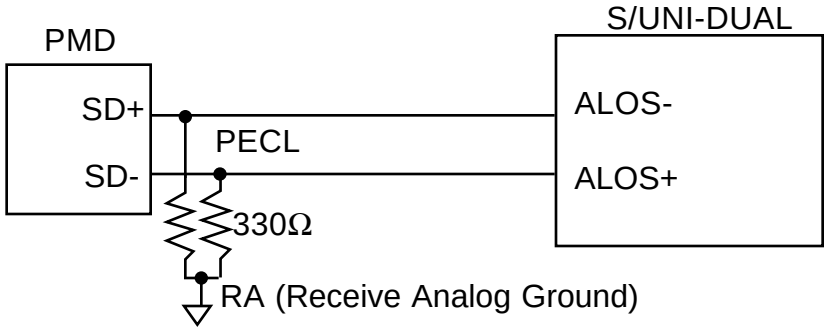
Fig. 6 ALOS- driven from a TTL source



c) Interfacing differential PECL SD outputs

Notice that both pins are internally self biased to 3.7 Vdc via a 3KΩ source impedance. The PECL inputs are high-Z CMOS differential structures. A PMD with traditional two PECL outputs can be connected as shown with 330Ω pulldowns close to the PMD to bias the PECL drivers.

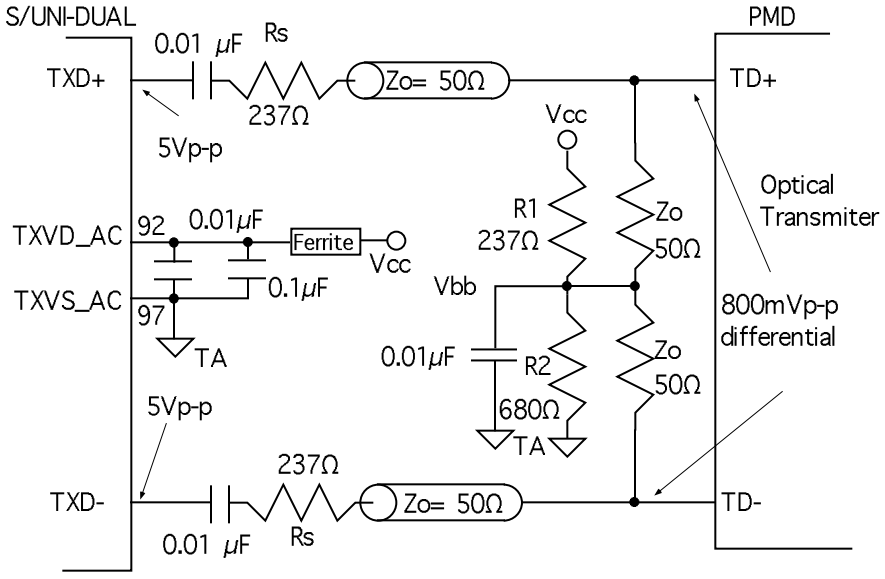
Fig. 7 ALOS± driven from a differential PECL± source



2.6. Interfacing TXD+/- outputs

TXD+/- are high speed data outputs running at 155.52 Mbit/s at worst case. If the data is alternate ones and zeros, a 77.26 MHz signal will result. TXD and RXD are the fastest signals on the board and proper attention must be taken to minimize jitter.

Fig. 8 TXD± driving a PMD with PECL inputs



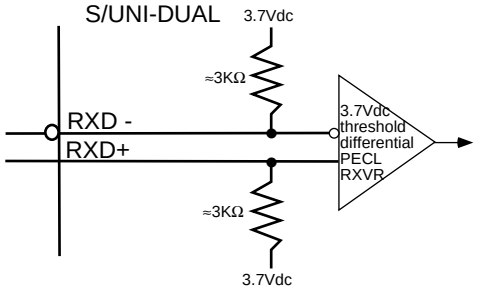
The 237 ohm and 50 ohm resistors reduce the 5 Vp-p TXD to a safe 800 mVp-p PECL level. Ceramic 0.01µF capacitors are used to AC couple and level shift these CMOS output to proper PECL levels. The transmission line effects are addressed with a 50 ohm PCB trace and the 50Ω Zo terminating resistors. The terminating 50Ω resistors are terminated into a locally generated Vbb of 3.7 Vdc.

2.7. RXD+/- inputs

RXD+/- are high speed data inputs running at 155.52 Mbit/s at worst case. If the data is alternate ones and zeros, a 77.26 MHz signal will result. RXD and TXD are the fastest signals on the board and proper attention must be taken to minimize jitter. These inputs should be driven with a balanced PECL± source.

The S/UNI-DUAL has differential RXD± inputs with common mode rejection. The DC bias voltage for these inputs is internally set to 3.7 Vdc, through a Thévenin 3KΩ impedance. These resistors are tied to the power R1AVD1 and ground R1AVS1 pins. Hence, noise on these power pins may alter the 3.7 switching bias point. Proper decoupling of this supply is important for optimum jitter tolerance. Also, these PECL inputs have to be AC coupled else the 3.7V DC bias will be affected.

Fig. 9 RXD± block diagram



The DART board incorporates an HP optical PMD with PECL level RXD± outputs. The following points were observed:

1) Bias the PECL outputs with 330 Ω resistors to ground

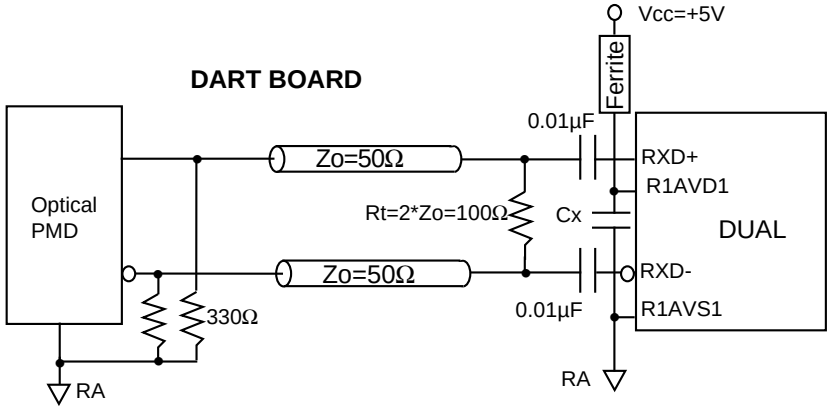
2) Route the signal to the DUAL along proper PCB traces:
   - controlled trace impedance, 50Ω on the DART board
   - no vias or no sharp turns

3) 100Ω resistor termination between the two signals close to the DUAL.

4) AC couple to RXD+/- with 0.01uF ceramic high frequency capacitors.

5) Decouple R1AVD1 to R1AVS1 as shown with a series ferrite and capacitors Cx (two capacitors in parallel, 0.1 µF with 0.01 µF).

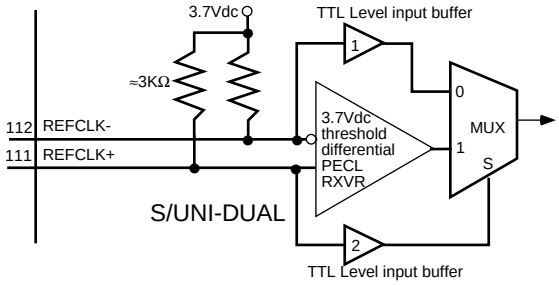
Fig. 10 Terminating RXD± PECL signal



2.8. REFCLK +/- 19.44 MHz inputs

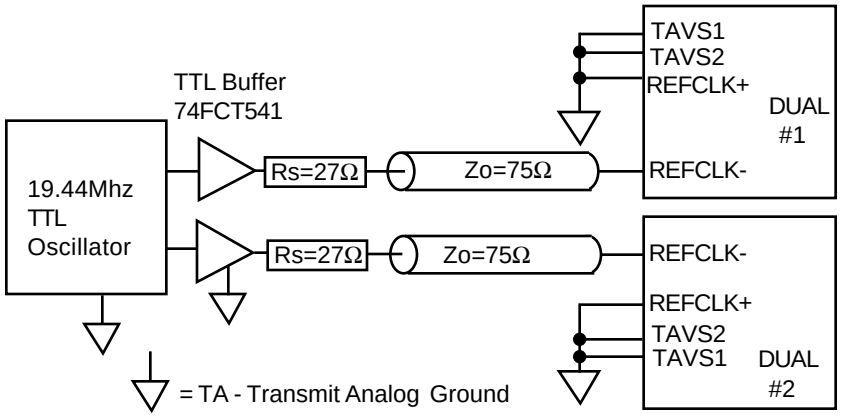
The DUAL reference clock inputs are different than in the S/UNI-LITE PM5346. The DUAL IC has programmable inputs. You can drive these with either a two wire PECL or a single ended TTL or CMOS source. These inputs have the same input structure as the DUAL ALOS+/- inputs. A PECL two wire signal can be connected between REFCLK+ and REFCLK-. Or, TTL input mode can be selected by grounding REFCLK+. A TTL low input to TTL gate #2 forces the MUX to select the output of TTL gate #1.

Fig. 11 REFCLK± input block diagram



The DART board utilized a TTL (vs. PECL) 20ppm oscillator and a 74FCT541 high speed single ended TTL buffer. Fast slew rate FCT buffer is required to reduce clock jitter. A source series termination of 27Ω was used to DC drive the 75 ohm transmission line. The REFCLK+ is strapped to ground to enable single ended REFCLK- operation.

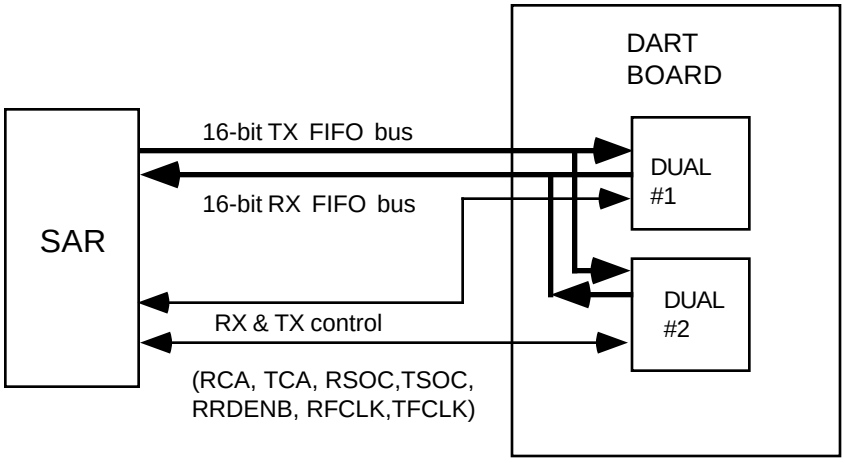
Fig. 12 REFCLK± as implemented on the DART board



2.9. Drop side 50 MHz FIFO bus

The drop side refers to the parallel FIFO Receive and Transmit data bus and its associated handshake control signals as shown below: The FIFO RFCLK and TFCLK clock can be 50 MHz and can present careful timing and termination design to ensure error free operation. Please refer to the data sheet for detail timing information. Please note the output electrical specs and that driving a DC termination load of 50Ω or even 100Ω is not possible. Series source terminations of about 27Ω could be used or if timing permits (ie. clock speeds slower than 50 MHz), a bus driver could be used for driving off-board.

Fig. 13 Drop side - PHY Interface block diagram



The associated drop side PHY bus timing is illustrated below. For complete detailed timing information, please refer to the S/UNI-DUAL, PM5348 Data Book, PN# PMC-950919.

Fig. 14 Multi-PHY mode timing 16-bit, TX FIFO near empty option

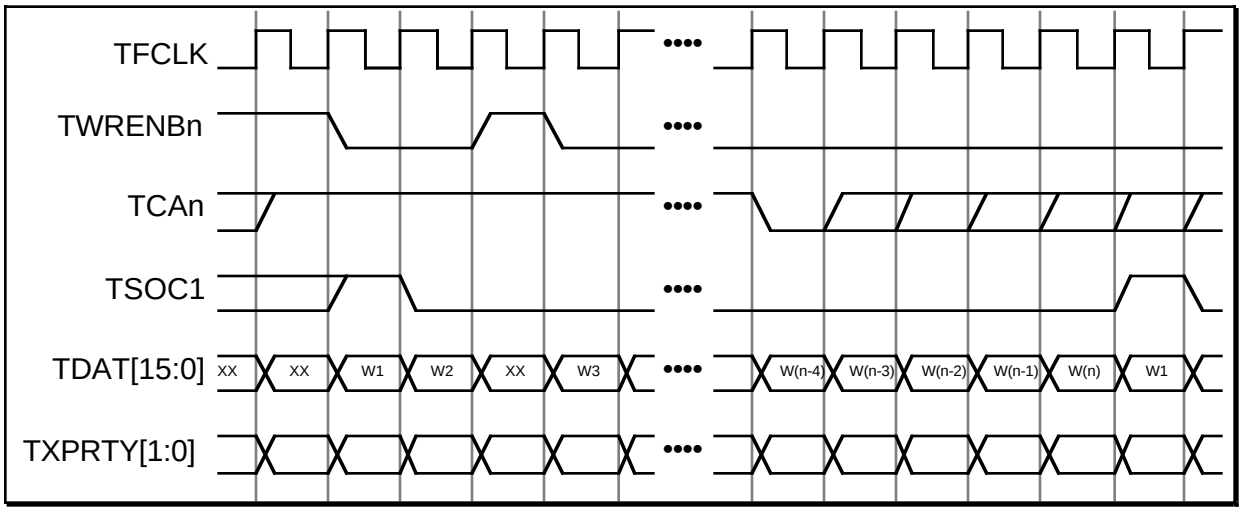
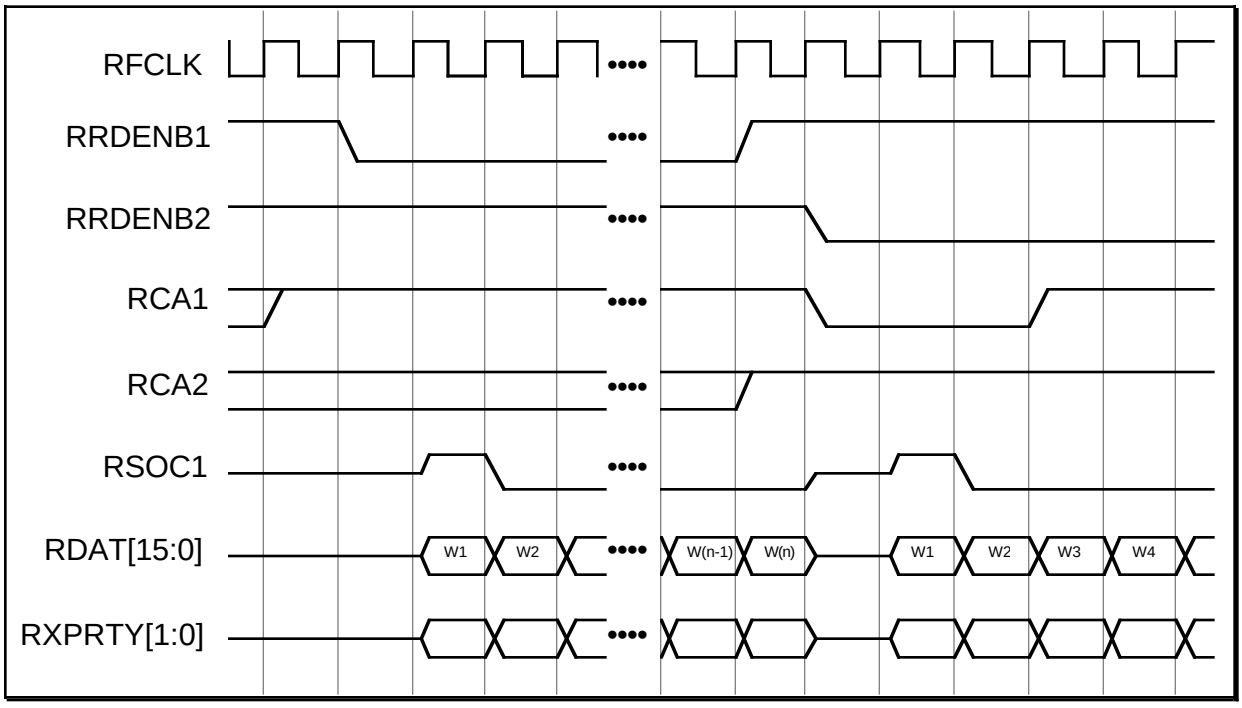


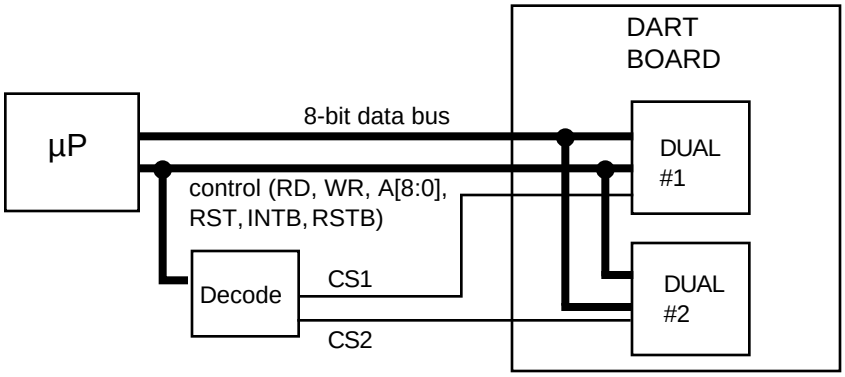
Fig. 15 Multi-PHY Mode Timing, 16-bit, receive FIFO empty and Tri-state options



2.10. Drop side microcontroller interface

The S/UNI-DUAL powers up in a 'basic' default state and is ready to receive and transmit ATM cells. A microprocessor is required if one requires the ability to read or write to the internal status or control registers. Please refer to the PM5348 data sheet for µP interface specifications. Relative to the RXD+/-, or the drop side FIFO interface, this is a slow bus and normal digital design rules should be followed.

Fig. 16 DART board µP interface



2.11. Decoupling for Intrinsic Jitter on the DART board

To optimize intrinsic jitter on this reference design, it is beneficial to decouple the 5 Vdc power pins, TAVD1 and TAVD2 as shown in the enclosed schematics. A series ferrite is required with a 1.0µF Tantalum in parallel with a 0.01µF ceramic decoupled to their respective analog ground pins, RAVD1 and RAVD2.

3. DESIGN CONSIDERATIONS

3.1. When do you use PECL/ECL instead of TTL/CMOS?

The faster the digital signal, the faster the technology one must use (implies fast slew rates also) to maintain data integrity. Also, the longer the traces, the more reliable the transmission technology required. The S/UNI-DUAL is a mixed mode CMOS semiconductor with high speed analog and digital circuits. Since PECL/ECL is more complex and expensive to use, it should be used only where necessary.

In normal short distance layouts the 19.44 MHz REFCLK can be a single ended TTL or CMOS type as long as transmission line design rules are adhered to. Controlled impedance traces with proper termination are recommended.

The RXD± and TXD± signals must be PECL due to the speed and jitter integrity.

3.2. What are the main concerns of using PECL over ECL?

As ECL uses the upper rail of the supply as the reference for the I/O and internal switching, a negative supply with the ground being the reference is a natural choice, as it is easier to keep the ground plane quieter than the power rail. Since ECL requires a negative power supply and most designers mixing TTL/CMOS with ECL only want a single supply, PECL (positive ECL) became a common choice. PECL operates the same as ECL but now has the noisier +5 Volt rail as the reference. PECL devices are differential; the noise on the inputs will be common mode noise and will not affect a differential input, but it will affect the internal reference, especially if the power supplying the transmitting device is not in common with the receiver.

The S/UNI-DUAL RXD± and REFCLK± are differential inputs with common mode rejection. These inputs will decode a voltage difference between the input, and not with respect to ground. However the DC bias voltage is internally set to 3.7 Vdc through a Thévenin 3KΩ impedance. These resistors are tied to the power R1AVD1 and ground R1AVS1 pins. Hence, noise on these power pins may alter the 3.7 switching bias point. Proper decoupling of this supply is important to optimize jitter tolerance. Also, these PECL inputs have to be AC coupled, otherwise the 3.7V DC bias will be affected.

3.3. What PECL termination scheme is the best to use?

"Termination" applies to terminating a signal propagating down a transmission line to the characteristic impedance of line. If the line is not terminated to its characteristic impedance, there will be reflection back down the line. The amount of reflection at the load (receiver) is given by the load reflection coefficient:

$$\rho L = (R_T - Zo)/(R_T + Zo)$$

where R_T is the load impedance and Zo is the characteristic impedance of the line. The amount of reflection at the source (transmitter) is given by the source reflection coefficient:

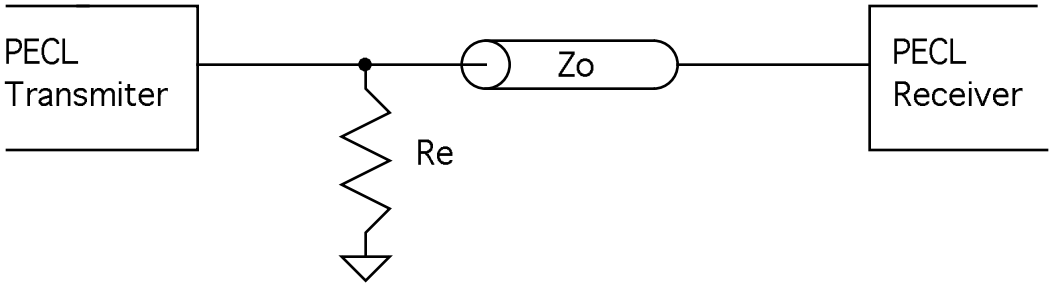
$$\rho S = (R_S - Zo)/(R_S + Zo)$$

where R_S is the source impedance and Zo is the characteristic impedance of the line. The reflected signal propagates back and forth until the "ringing" dies out.

There are 4 basic types of terminations used for PECL (or ECL): Open line termination, series termination, parallel termination, and Thévenin parallel termination. Since PECL (or ECL) signals only drive high, external biasing is need to pull the PECL signal low. This biasing has to be incorporated into the termination scheme.

Unterminated lines (open line) should only be used for very short line lengths (less than 1/4 of an inch), or for low frequency signals. An unterminated line is shown below with resistor **Re** used to pull the PECL signal low:

Fig. 17 Unterminated transmission line



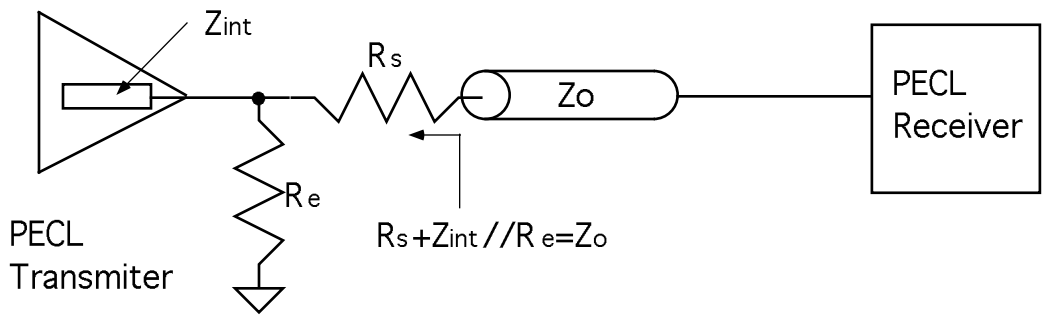
The maximum unterminated line length is given by the following equation :

$$L\max = 0.5 * (\sqrt{(C_D / C_O)^2 + (t_R / T_{PD})^2}) - C_D / C_O)$$

where **L** = line length, $\mathbf{t_R}$ = rise time, $\mathbf{T_{PD}}$ = propagation delay per unit length, $\mathbf{C_O}$ = capacitance per unit length, and $\mathbf{C_D}$ = the distributed capacitance. The above equation assures that the undershoot will be limited to 15% of the full logic swing.

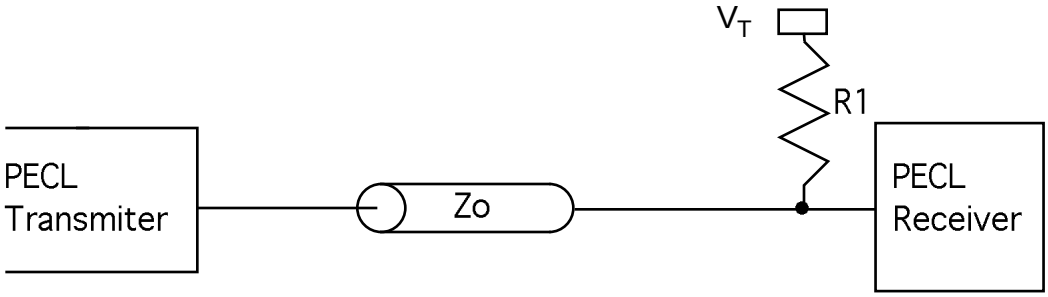
Series terminated lines can be used when the interconnect distances are long or there are discontinuities in the characteristic impedance lines. A series resistor at the output of the driver reduces the voltage swing of the logic signal in half. The 1/2 amplitude signal propagates down the transmission line. At the end of the characteristic impedance line, the voltage doubles since the reflection coefficient is unity due to the unterminated line. The half amplitude swing along the transmission line reduces crosstalk, but if the distance between the end of the transmission line and the receiver input is not kept short as in Lmax above, the reflection is added to the signal and propagates back to the transmitter. A series terminated line is shown below where **Rs + Zint//Re must equal Zo.**

Fig. 18 Series terminated transmission line



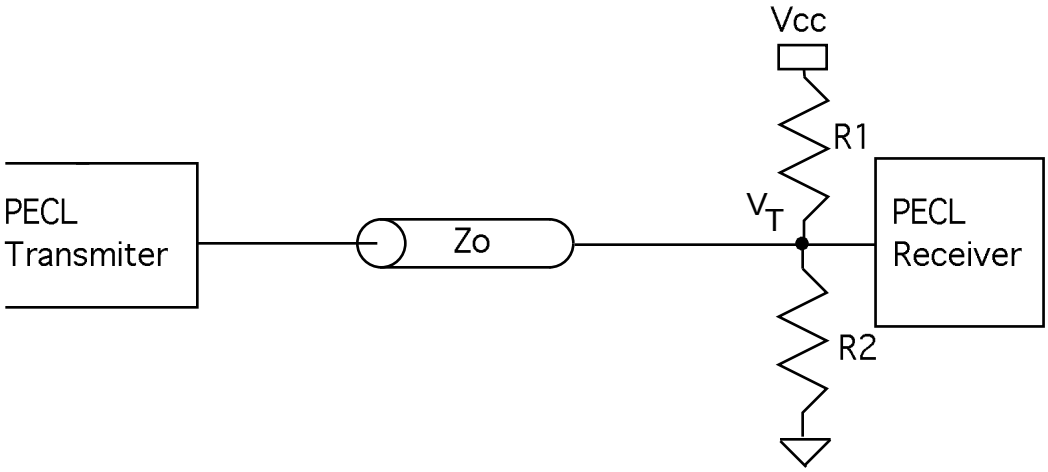
Parallel terminated lines offer the best terminations for speed and power consumption. The receiver end of the transmission line terminates and biases the signal. The terminating resistor is the same value as the characteristic impedance of the transmission line. Unfortunately this requires another voltage supply as the terminating voltage (V_T) is Vcc - 2 Volts. A parallel terminated line is shown below where $\mathbf{R_T}$ equals **Zo**:

Fig. 19 Parallel terminated transmission line



Thévenin terminated lines terminate the lines to the characteristic impedance and sets the terminating (V_T) voltage. A Thévenin equivalent parallel termination is shown below:

Fig. 20 Parallel Thévenin terminated transmission line



The resistors R1 and R2 in parallel must equal Zo and the voltage at the input must pull the output of the transmitting gate to **Vcc - 2** Volts. Working out the equations for Zo = 50Ω and PECL Vcc +5 Volt supply gives:

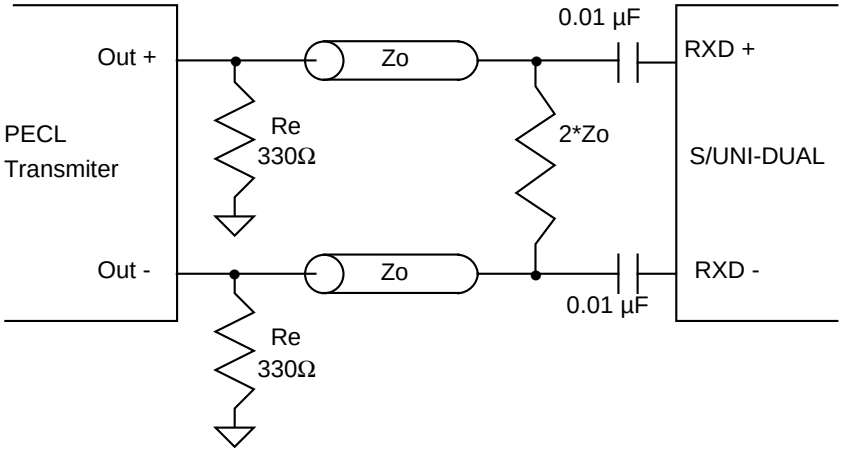
$$\mathbf{R2 = 2.5 * Zo}$$

$$\mathbf{R1 = R2*2/3}$$

Note that the above examples show only one of the differential inputs. With the Thévenin termination care must be taken so that the Vcc and grounds of the differential signals are taken in close proximity of each other or the noise on Vcc and ground will not be in common with each other.

Since the S/UNI-DUAL's PECL (pseudo ECL) inputs are internally self-biased, a hybrid of the parallel termination can be used which has minimum current draw and the terminating voltage (V_T) is not required. By AC-coupling into the S/UNI-DUAL, the S/UNI-DUAL sets the internal switching threshold. A resistor $2 * Zo$ is placed between the differential outputs at the terminating end as shown below to terminate the line:

Fig. 21 S/UNI-DUAL RXD± driven by PECL PMD

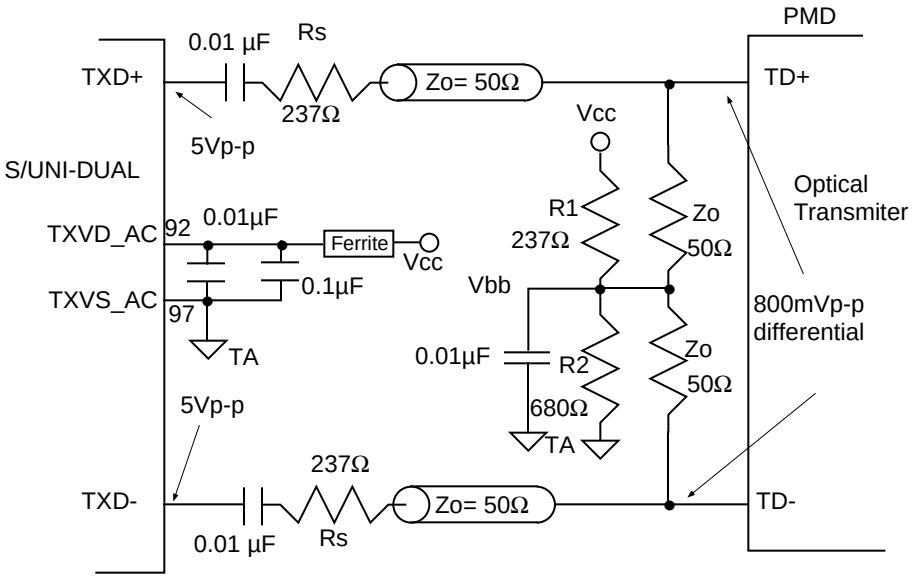


The **Re** 330Ω resistors are placed close to the drivers and are required to properly bias the PECL output structures since PECL drives high only.

3.4. How to convert the S/UNI-DUAL CMOS outputs to PECL levels?

The S/UNI-DUAL high speed CMOS outputs have to be AC-coupled, attenuated, level shifted and terminated into a PECL optical transmitter input. This can be done with a CMOS to PECL converter like a Motorola MC10H352, however a more cost effective way is shown below:

Fig. 22 DUAL's TXD± driving PECL input PMD



The TxD+/- outputs are AC-coupled and then the series resistor **Rs** is used to attenuate the CMOS levels to PECL levels. The **Vpp** input (voltage requirement of PECL input) swing is given by the equation below with **Rout** (approximately 25 ohms) being the output impedance of the S/UNI-DUAL drivers. For **Vpp** = 800 mVolts of swing, **Rs** is approximately 240 ohms.

$$Vpp = (Zo/((Rs + Rout) + Zo)*Vcc$$

The **Vbb** voltage (3.7 volts for PECL) is generated by a voltage divider network which is set to the switching threshold of the optical transmitter:

$$Vbb = Vcc* R2/(R2 + R1)$$

3.5. What can be done to minimize power supply transient voltages?

High current draw during IC switching causes power supply transients ΔI due to the inductance of the power lines. Large voltages appear on the power rails due to the transient current flowing through these power line inductances. The magnitude of the noise voltage can be reduced by minimizing the inductance of the power lines and by decreasing the magnitude of the transient currents. The power line inductance can be minimized by using a power plane. The transient currents on the power rails can be minimized by supplying the power from an alternate source such as a decoupling capacitor near the circuit that is drawing the current.

The decoupling capacitance and the inductance of the wiring between the capacitor and the power pin determines the noise voltage at the power pin. Bulk decoupling capacitors are used to supply the bulk DC current, and the high frequency decoupling capacitors are used to supply all the transient current that is required when the circuit is switching.

3.6. What values should the decoupling capacitor be?

The bulk decoupling value should be 10 times the value of all the decoupling capacitance combined and should be located where the power comes in. Capacitors with low internal inductance should be used such as a tantalum electrolytic. Stay away from aluminum electrolytic as their inductances are an order of magnitude larger than the tantalum capacitor. A ferrite bead (or 1 to 10 µH inductor) can be used before the bulk capacitor to keep the power supply transient noise from entering the circuit. The power pin decoupling capacitor must be able to supply all the switching current. The minimum capacitance can be calculated by:

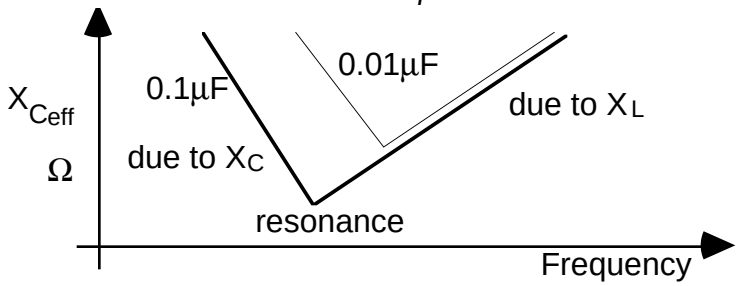
$$\mathbf{C = \Delta I * \Delta t/\Delta V}$$

The transient voltage drop $\Delta\mathbf{V}$ in the supply voltage is caused by the transient current $\Delta\mathbf{I}$ occurring over time $\Delta\mathbf{t}$. Using decoupling capacitors that are too large should be avoided. Since all capacitors have some inductance in series with the capacitance there will be a self-resonance at a certain frequency. Above this frequency, the inductor's impedance will increase, the effective impedance of the capacitor will increase and thus high frequency decoupling will suffer. The self-resonant frequency is given by the equation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

For decoupling a particular frequency, the lower the capacitor's impedance (Xc) at resonance, the better. Due to the capacitor's self inductance (X_L), the effective impedance of the capacitor (X_{Ceff}) is:

$$X_{Ceff} = X_C + X_L = \frac{1}{2\pi fC} + 2\pi fL$$



Note that the larger the capacitance (for the same inductance) the lower the resonant frequency. If the capacitor is too large, the self-resonance will be too low to be an effective bypass but if the capacitor is not large enough, there will be insufficient current to supply the transient current during switching. The smallest value capacitor to satisfy the above equations should be used. It is rarely necessary that a capacitor larger than 0.01 µF be used.

3.7. Where should the decoupling capacitors be placed?

The decoupling capacitor should be placed as close to the IC power pin as possible reduce the wiring inductance. IF there are two capacitors like 1.0uF and 0.01uF, place the 0.01uF closest to the pins. Ideal placement for an SMT device is on the component side at the pins, where trace length and even vias are eliminated. There are 5 sources of inductance: the inductance of the capacitor, the inductance of the wiring between the capacitor and the IC power pin, the power pin lead inductance inside the IC, the ground pin lead inductance inside the IC, and the ground inductance between the IC pin and ground. The capacitor inductance is negligible if the correct capacitor is used. There is no control over the lead frame inductance. To keep the inductance low, both the power lead and the ground lead should be keep as short as possible (less than 1.5 inches). The inductance for a trace is given by:

$$L = 0.005\ In(2\pi h/w)\ \mu H/inch$$

where **In** is the inverse log, **h** is the height between power or ground lead and the ground plane and **w** is the width of the power or ground lead. Note that doubling the width of the trace or reducing **h** will only decrease **L** approximately by 20 %, but decreasing the length by 50% will decrease the inductance by 50%. A typical board has about 15 nH of inductance per inch.

3.8. What can be done to minimize ground noise?

Return currents and power supply transients during high current consumption produce most of the ground noise. Since ground noise cannot be controlled by decoupling capacitors, the only way to minimizing the effect of ground noise is to minimize ground impedance and design circuits as to minimize currents. The best way to minimize ground impedance is to use a ground plane. It is not advisable to use ferrite beads in the ground path as this will inhibit the return currents from leaving and raise the ground noise level. This is a problem since TTL and CMOS logic are referenced to ground.

3.9. What to do with unused (CMOS) inputs?

All unused inputs should be connected to their inactive state to prevent unintentional switching which produces noise generation and power consumption. For the CMOS inputs the inactive low state can be connected to ground and the inactive high state can be connected to the power rail (Vcc) through a series resistor (4.7k).

3.10. Is it necessary to isolate the analog from the digital?

Yes. The digital CMOS circuits have high immunity to external noise (approximately 0.3 * Vcc) whereas a small amount of external noise coupled into the analog circuits can be devastating. The analog circuits operate on low voltage swings (600 mVolts for the S/UNI-DUAL PECL inputs) as compared to the large (5 Volt) of the CMOS inputs. The CMOS circuits can also generate a lot of switching noise, especially when a large number of circuits are running synchronously all timed to the same system clock. If the analog power and grounds are not isolated from each other it is unlikely that the device will be able to do clock and data recovery without any bit errors.

3.11. Should one isolate the transmit analog from the receive analog?

Yes. Any noise on the S/UNI-DUAL receive analog power and ground inputs or on the PECL inputs will impact the internal PLL's ability to recover the clock from the incoming data. Added noise will degrade jitter tolerance and add jitter to the recovered clock. It is also important to keep the analog optical receiver in common with the receiver portion of the S/UNI-DUAL, especially the grounds. The S/UNI-DUAL PECL inputs are differential and will reject common mode noise. However, they are internally self-biased between Vcc and ground (about 3.7 Vdc) and therefore must be AC-coupled. This 3.7V reference must be stable with reference to the incoming signal so that the switching threshold does not move and thus cause bit data jitter. It is especially important to keep the ground plane between the optical receiver in common with the RAVS1 & RAVS2 inputs of the S/UNI-DUAL. Ideally, any transmission trace should be routed directly over top of it's respective ground plane.

On the transmit side of the S/UNI-DUAL, a 155.52 MHz clock is synthesized from a 19.44 MHz reference clock. Any added noise on the power or ground inputs impacts the resulting 155.52 MHz clock. The added noise will increase the intrinsic jitter of the transmitter. The power and ground of the optical transmitter can be in common with the analog transmit power and ground of the S/UNI-DUAL.

3.12. How to isolate analog from digital and transmit from receive?

The DART board has three separate grounds, one for digital, one for analog 155.52 Mbit/s transmit , and one for the high speed analog receive. All three grounds are shorted together at the main connector. Digital +5 power is Vcc and is used directly with some local 0.1 uF decoupling. The other analog +5 power supplies are derived with series ferrites and local decoupling to the appropriate Transmit (TA)or Receive (RA) analog grounds. It is very important to keep the TX of the optics on the same ground as the DUAL. The same goes for the RX ground plane since the DUAL RXD± internal 3.7V reference is derived from power and ground.

One of our previous reference designs used cuts (channels) in the power/ground planes to isolate currents. This is more difficult to control and to predict the final results. Using this method, several PCB revisions may be required to achieve the optimum end result.

3.13. How does layout affect high speed return current?

At low speeds return current follows the path of least resistance back to the driver. At high speeds, however, the return current follows the path of least inductance which lies on the plane directly under the signal trace, as the total loop area between the outgoing and returning paths is minimized. In other words, the high-speed return current follows a path that is almost the "mirror image" of the signal trace on the plane underneath the trace. This tight coupling provides good flux cancellation so that common-mode current is reduced. Therefore, high speed traces should not cross cuts or heavily perforated areas (where tight spacing through-hole components reside) on the power and ground planes, as any cuts on these planes may interrupt the return currents, causing them to seek alternative paths back to the driver. The different routes taken by the outgoing and return currents will both induce common-mode noise on other nearby signal traces. In addition, by routing high speed signals over continuous power planes, the return current paths of these signals are known and other signals will not cross over these return currents, reducing the possibility of noise coupling. Detailed discussions on high-speed design are provided by the references.

3.14. When should ferrite beads be used?

Ferrite beads are mainly used on power rails to pass DC current but to attenuated the higher frequency noise that is riding on the DC rail. The impedance of ferrite beads increases with frequency. At DC the ferrite bead is like a short, but at higher frequencies, the impedance of a ferrite bead can increase to over 100 ohms (depending on the bead and frequency). Ferrite beads attenuate high frequency noise from the power supply from getting into a circuit, but they also stop high frequency noise from leaving the circuit. It is important, therefore, to use proper bypass decoupling when using ferrite beads.

Ferrite beads should be avoided on CMOS I/O power pins as the high current switching of the CMOS circuits causes a $\Delta \mathbf{I}/\Delta \mathbf{t}$ noise to be introduced into the power rail. Ferrite beads should also be avoided on the ground bus as this inhibits the return currents.

Ferrite beads can be used on the S/UNI-DUAL analog power pins as they draw very little current. The ferrite beads isolate all the receive inputs from each other. As the noise frequencies and levels are different in every design, it is hard to decide if beads are necessary and at what frequency should they be effective. However, it is harder to insert a ferrite bead after the board is built than it is to short out the bead if it is not needed.

The S/UNI-DUAL analog power pin RAVD2 generates a 311 MHz oscillation. If there is no ferrite bead on this input, the 311 MHz signal can get into the other analog power pins and performance can be affected.

Ferrite beads can be used on the optical receiver as the receiver portion draws very little current. Ferrite beads can also be used on the optical transmitter power rails as the transmitter drives a differential PECL pair which draws constant current. Most optical module vendors recommend using ferrite beads on both the receive and transmit power rails.

PECL (ECL) circuits draw constant current regardless of the frequency of operation as opposed to CMOS, which only draws current during switching. The DUAL does not have true PECL drivers, they are CMOS matched complimentary drivers. There will always be one of the two drivers turned on, and there will be a constant current drawn through the power pins.

3.15. Is it necessary to de-couple every power pin of the S/UNI-DUAL?

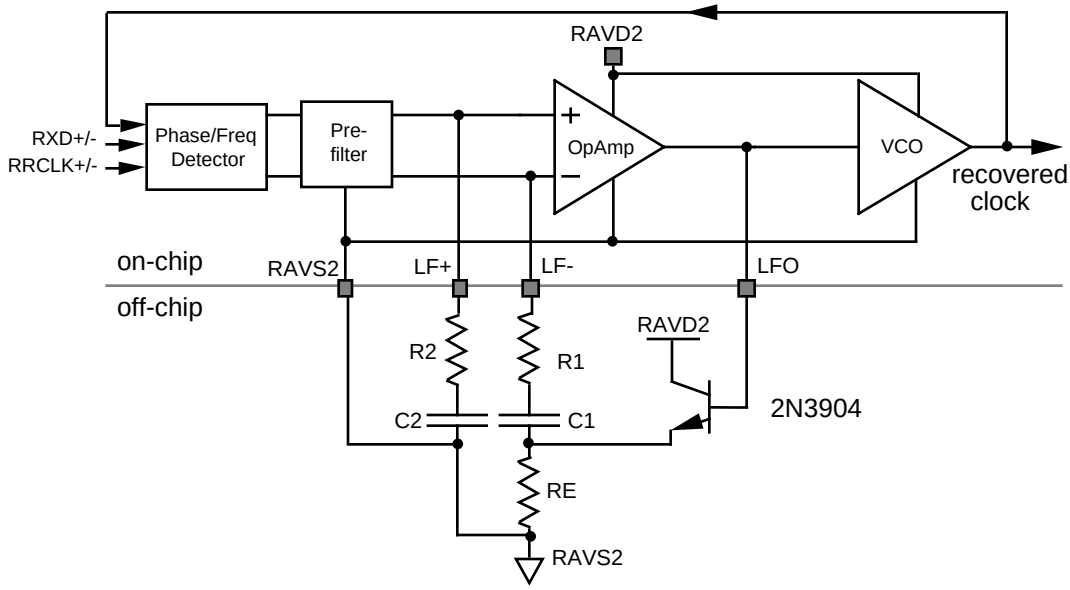
The S/UNI-DUAL can generate a lot of simultaneous synchronous and asynchronous switching noise. Especially if the drop side clock frequencies of the transmit and receive are synchronous and both logical devices are operational. It is important to decouple every power pin so as to reduce self generated noise and also prevent this noise from coupling onto the other planes and power pins.

3.16. Loop filter using ceramic capacitors

The internal op-amp in the S/UNI-DUAL's clock recovery unit (CRU) regenerates a 155.52 MHz clock from the incoming SONET data.

NOTE: the component values below are provisional. The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. The capacitor C1 should be non-polarized because when the S/UNI-DUAL is held in reset, it is reverse-biased at approximately 2.0 VDC. Also, for some process extremes, the capacitors may operate with a DC. reverse-bias of up to 1.0 VDC. In addition, under normal operating conditions, when the PLL is locked, the LF+ pin will be at about +1.0 VDC average. Since the S/UNI-DUAL is a terminating device, the loop filter values were chosen to achieve maximum jitter tolerance performance in the LAN application. C1 and C2 should be of a temperature stable Ceramic X7R or X5R (X=-55°C, 5=+85°C, 7=+125°C, and R = ±15% capacitance variation over this temperature). The X5R and X7R devices are available in initial tolerance of ±20%, ±15%, ±10% and are available in 6.3V, 10V, 16V, 25V or 50V. Y5V and Y5U should be avoided as these ceramics exhibit poor temperature tolerance for this application.

Fig. 23 Clock recovery loop filter using ceramic X5R capacitors



Line Rate (Mbit/s)	R1 (±1%)	R2 (±1%)	C1, C2 (X5R, ±20%)	RE (±1%)
155.52	68.1Ω	200Ω	4.7 µF	100Ω

Table 1: Recommended Component Values

Please see Appendix E for capacitor vendor details. A few suggested manufacturers of X5R and X7R ceramic capacitors are:

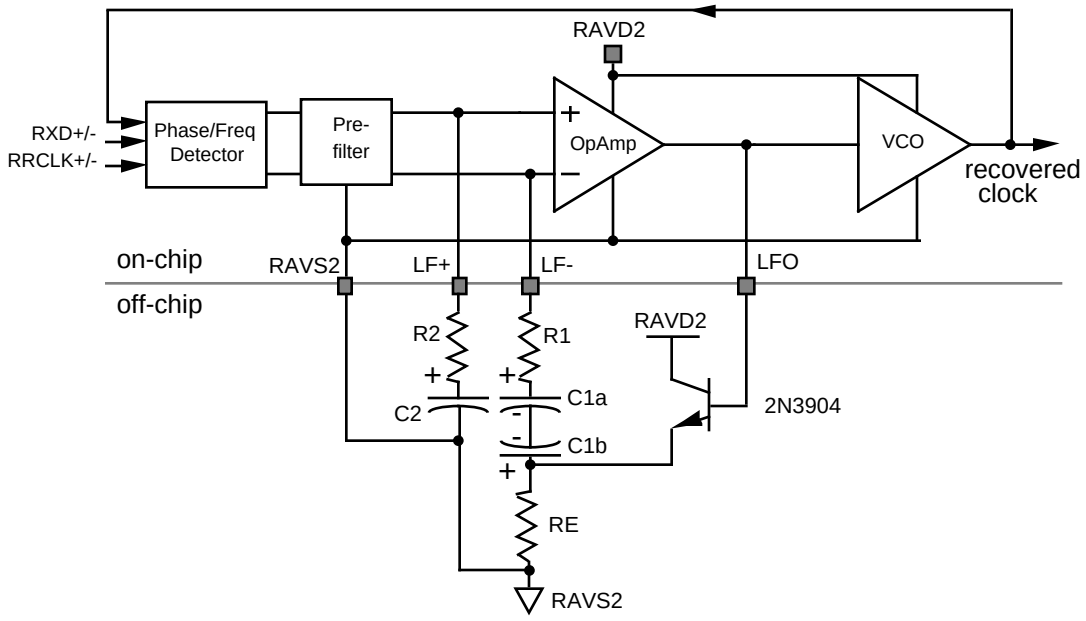
Manufacturer	PN#	µF	Type	VDC	Footprint
Taiyo Yuden	LMK316BJ475ML	4.7	X5R	10V	1206 (0.12" by .10")
Taiyo Yuden	EMK325BJ475MN	4.7	X5R	16V	1210 (0.12" by .10")
TDK	CC1206JX5R475K	4.7	X5R	6.3V	1206 (0.12" by .06")
PHILIPS	2220RR475K8AB0C	4.7	X7R	25V	2220 (0.22" by .20")
AVX	SM015C475KAJ240	4.7	X7R	50V	3230 (0.32" by .30")
Prestidio	3736X7R475K1NT91A	4.7	X7R	25V	3736 (0.37" by .36")
Vitramon	VJ2225Y475KXXAT	4.7	X7R	25V	2225 (0.22" by .25")

3.17. Loop filter using polarized tantalum capacitors

Due to footprint requirements, or sourcing constraints, two polarized Tantalum capacitors connected in series may be a more desirable option. Either back to back (-'ve to -'ve) or anode to anode (+'ve to +'ve) may be used to form one non-polar capacitor. Since the effective capacitance will be halved, two 33 µF capacitors must be used to form one 15 µF (actually 16.5 µF) non-polar capacitor. Since the LF+ pin will always have a positive DC bias (about +1 Vdc when in lock), C2 may be a single polarized capacitor with the positive terminal connected to the LF+ pin. However, C1 is made up of a series combination of C1a and C1b as shown in the schematic below. AVX corporation publishes several articles on back to back tantalums.

The capacitor C1 should be non-polarized because when the S/UNI-DUAL is held in reset, the capacitor C1 could be reverse-biased up to approximately 2.0V. Also, for some process extremes, this capacitor may operate with a dc reverse-bias of up to 1.0 Vdc.

Fig. 24 Clock recovery loop filter with tantalum polarized capacitors

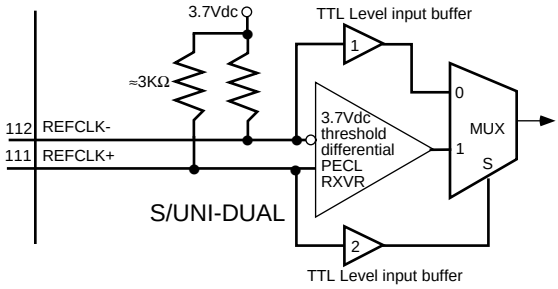


Line Rate (Mbit/s)	R1 (±1%)	R2 (±1%)	C2 (Tantalum, ±20%,)	C1a & C1b (Tantalum, ±20%, µF)	RE (±1%)
51.84	68.1 Ω	200 Ω	15 µF	33 µF	100 Ω

3.18. How to drive the REFCLK± inputs using one oscillator?

The REFCLK± , 19.44 MHz clock input block diagram is show below. These inputs can be driven with balanced AC coupled PECL source. Or if you ground REFCLK+, you can drive the REFCLK- with a single ended TTL gate. In this case the clock must be less than 0.4V for a low and 2V or more for a logic high.

Fig. 25 Block diagram of DUAL's REFCLK± inputs



In most applications it's more cost effective or technically desirable to supply a single ended 19.44 MHz reference clock. Generally, PECL clocks are very expensive and if you don't have to route the clock source a great distance a TTL/CMOS device is more than adequate, provided you design with care.

Fig. 26 Ideal reference clock

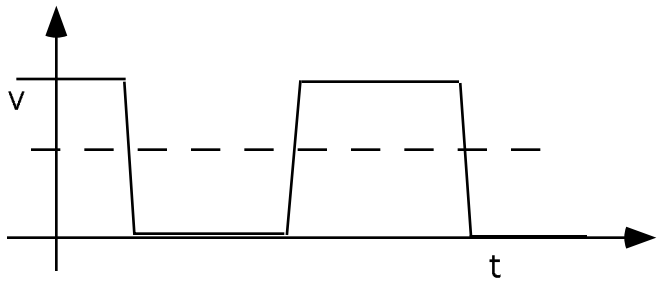
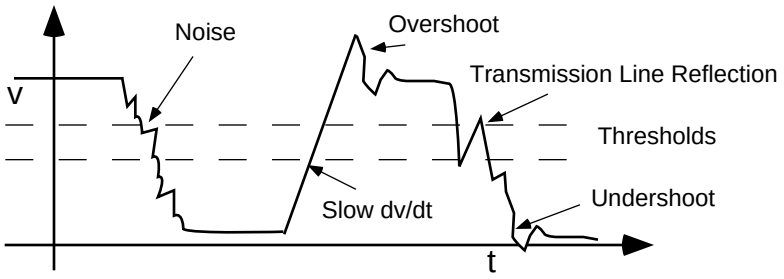


Fig. 27 Reference clock potential problems

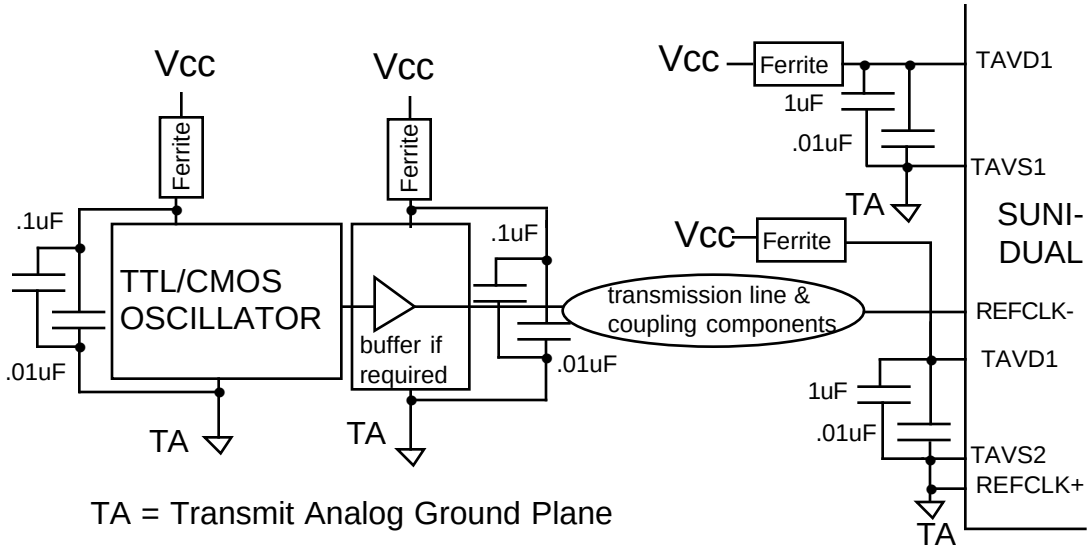


Ideal low intrinsic jitter is required if you use the 'non-loop time' mode TX clocking. However, even in loop-time mode, the fall-back is the reference clock if the RX clocking is lost due to a loss of RX clock. For non-loop time, whatever method you decide to use, please ensure that there is minimum jitter generated in the 155.52 MHz TX clock. As shown in the diagram above, ensure that you provide a low noise, free of jitter, properly terminated, minimum over/undershoot reference.

If it's a single ended clock, then attention must be paid to routing, termination, supply noise, and grounding. Since the PLL multiplies the reference clock by 8 to derive 155.52 it also multiplies any jitter at the input. So, jitter of 1.0 ns at the input is only 2% of the 19.44 MHz reference. However the output 155.52 MHz TX clock will have the same 1 ns jitter but now it's 1 ns/6.4 ns = 15% jitter.

As shown below, the system designer has several choices in clock generation and distribution. In all cases, to optimize intrinsic jitter, power supply decoupling is required. Note the larger 1.0 uF caps on TAVD1 and TAVD2. Please mount capacitors, especially the 0.01 uF, right at the pins.

Fig. 28 Decoupling REFCLK power pins



TA = Transmit Analog Ground Plane

a) Series source termination

The series termination may be the most desirable as it offers the lowest current consumption by the drivers, virtually zero current in the signal trace, and zero ground return currents. Therefore, the least amount of board noise to interfere with the analog circuitry. We chose trace Zo = 75 Ω because trace widths are easily manufacturable, and Rs is large enough and not swamped by the buffer source Z. The DART board incorporates the FCT541 circuit below. The FCT541 was chosen as it has faster rise time compared to 74ACT541 or 74F541.

Fig. 29 REFCLK using series termination with two loads

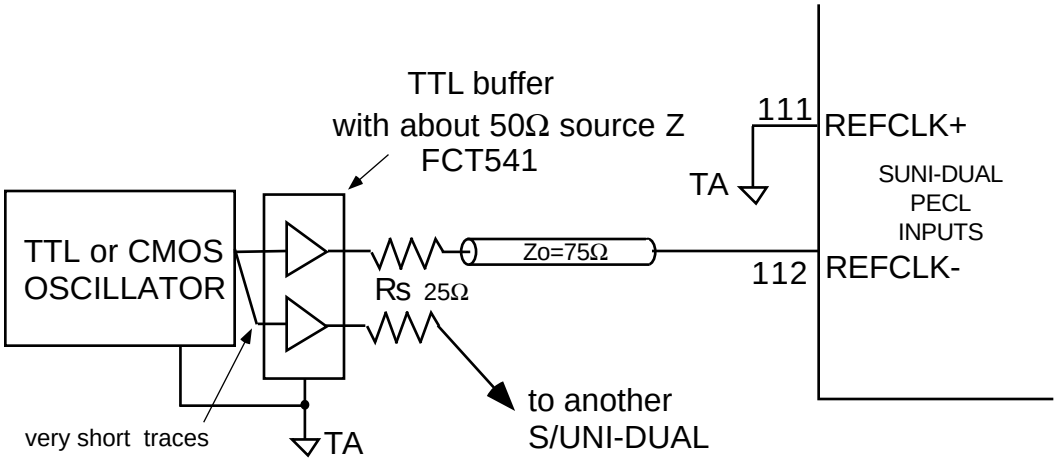
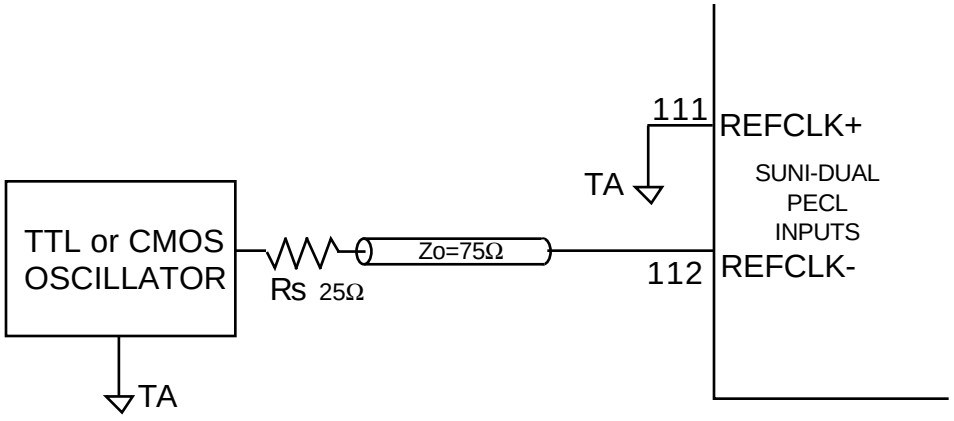


Fig. 30 REFCLK using series source termination and one load



The REFCLK+ signal must be connected to the TA (Transmit Analog Ground) and the signal source must be properly terminated. Also, very carefully decouple TAVD1 to TAVS1 and TAVD2 to TAVS2 as per schematic. Do not substitute/remove ferrites or capacitors.

Grounding the REFCLK+, internally turns off the PECL 3.7 Vdc threshold inputs, and enables the TTL level threshold (low = less than 0.8 V and high = more than 2.0V) gates.

The TTL oscillator should be placed as close to the buffer as possible as it is unterminated. The reason for using the TTL oscillator is to match the 74FCT541's TTL input level. A CMOS oscillator connected to these TTL inputs will cause duty cycle distortion on the output clock as TTL and CMOS signals switch at different thresholds. At the input thresholds, the edges must be sharp and free of noise, etc. When a different oscillator and buffer pair is used, it is important to match the output level of the oscillator to the input level of the buffer in order to avoid duty cycle distortion. Notice the FCT541 has TTL input thresholds (0.4V and 2V) and CMOS level outputs.

As on our DART board, series terminations may be the best choice since it offers the lowest power consumption, and the least amount of noise generated into the circuit. The buffer(s) is driving into a high impedance load hence the current will be almost zero except for current required due to stray capacitance (gate input capacitance). The source impedance must match the Zo of the trace. This source impedance is the sum of both the driver gate impedance and Rs, the external resistor. In our case we chose Rs = 25 Ω with trace Zo = 75 Ω. Careful check at the destination with a scope will assure the proper Rs selected. Make sure the inputs don't see any jitter or steps especially at the TTL input gate thresholds.

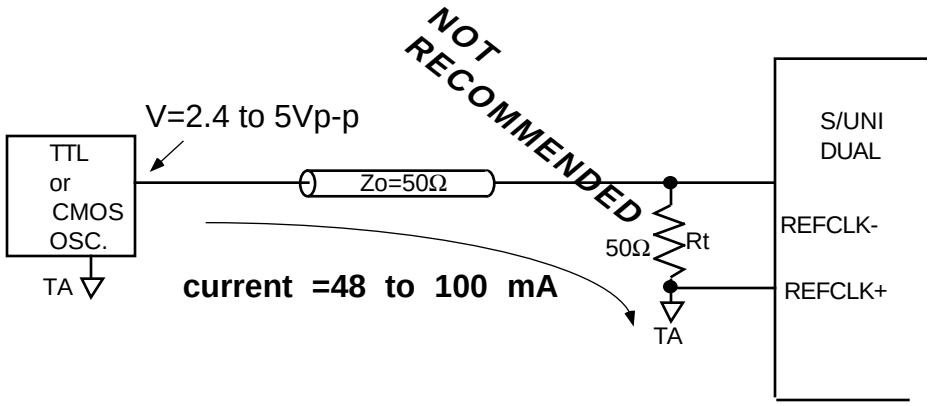
If you only have one DUAL on your PCB, then a buffer chip like the FCT541 is not required and you can use the oscillator to drive the Rs (source series resistor) directly. If you have multiple destinations it's a good idea to use multiple drivers with their own Rs. Multi drop is not recommended with the same driver as reflections will be a serious problem, depending on the trace length.

If you have only one Analog ground plane and multiple isolation cuts as in the SORD (S/UNI-LITE) reference design, then more careful attention must be placed to the routing and ground returns.

b) Parallel termination at the load using TTL thresholds

In the DUAL if you ground the REFCLK+ pin, the REFCLK- becomes a TTL threshold single ended input. Parallel termination may be used. However, the driver must be able to drive the necessary current into the far end Rt termination. At Zo = 50 Ω, Rt must be 50Ω and thus the current is 5V/50Ω= 100 mA. This will generate a lot of noise due to the driver switching, trace and ground return currents and is not recommended. To halve the drive current, you could use Rt with Zo traces =100Ω. But in practice, these are thin (0.008" wide) traces and may be difficult to manufacture reliably. Driving multiple loads is not recommended due to high current demands for this type design.

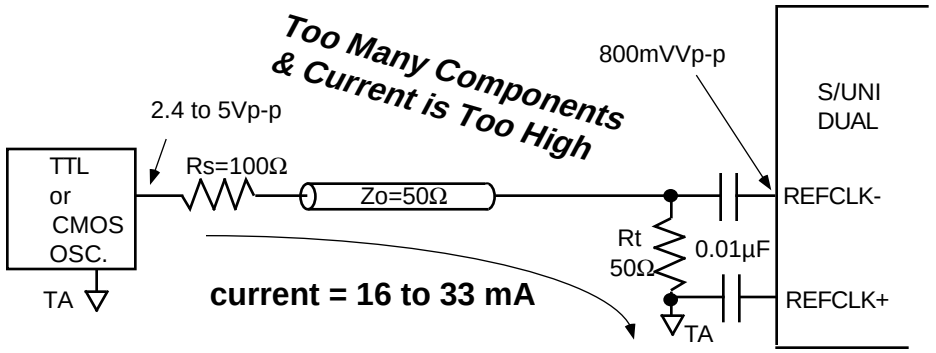
Fig. 31 Driving a 50 Ohm parallel termination load



c) Parallel termination with DUAL's PECL input thresholds

To reduce drive current, thus lower power and noise, it may be better to utilize the PECL thresholds of the REFCLK inputs. Care must be taken not to over load the DUAL inputs past the power rails. Simply decouple the REFCLK+ to TA (Transmit analog Ground) with a 0.01 uF cap and drive the REFCLK- with an AC coupled 800 mV clock. Here the current is 1/3 of method b) above.

Fig. 32 Parallel termination using DUAL's PECL inputs



$$Rs_{(min)} = \left(\frac{Rt[Vo_{(min)} - Vi_{(min)}]}{V_i} \right)$$

In this case, for a 50Ω transmission trace, Rt = 50 Ω, $Vi_{(min)}$, & $Vo_{(min)}$= 2.4V, Rs = 100 Ω. The maximum current , if Vo(max)=5V, would only be about 5V/150 Ω = 33 mA. The signal at the DUAL would be about 5V x 50Ω/150Ω = 1.67 Vp-p max. If the TTL output was only 2.4 Vp-p (as per worst case spec), then the current max = 16 mA and the input would be 800 mVp-p.

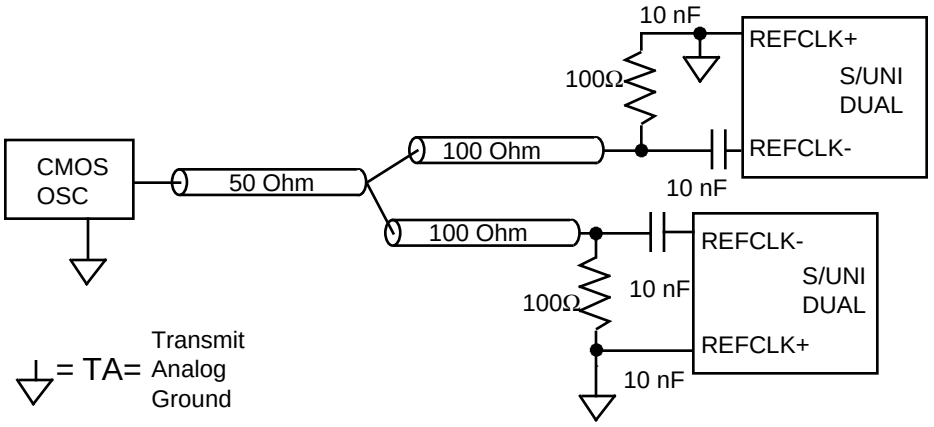
For Zo = 100 Ω, Rt = 100 Ω, then Rs = 200 Ω

d) Multidrop parallel termination with PECL load

One may be tempted to connect the one clock trace to two different devices and terminate at the far end. The concern is that the transmit and receive grounds could be isolated by channels cut into the ground plane. Potential difference between the grounds will affect one of the reference clock inputs. For example, if the reference clock is terminated to the ground of one device, the other device will get a less than ideal signal. A second problem may arise if the clock signal trace crosses the cuts in the ground plane (i.e. from transmit ground island to receive ground island). In that case, ground return current from the receive side cannot follow the signal trace back to the driver. Instead, it will seek an alternative path of least inductance. Consequently, this ground current will induce common-mode noise on signals nearby.

One solution may be to run a 50 ohm clock trace to the vicinity of the two inputs and then split into two 100 ohm traces. There will be no Zo discontinuity at the junction of the 50Ω and the two 100Ω traces. The two 100 Ω traces will look like a 50Ω trace since they are in parallel. The following diagram illustrates this solution:

Fig. 33 Multidrop parallel termination of the REFCLK

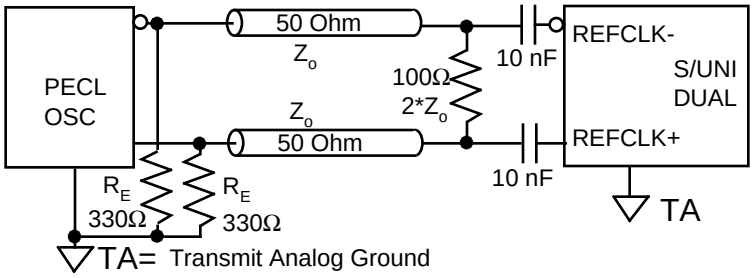


The drawback of the above solution is that, based on the layer setup described in Appendix F, the width of an 100 Ohm trace is less than 3 mil. This width may be difficult for board manufacturer to fabricate accurately. Inaccuracy in trace impedance will cause the signals to be improperly terminated.

e) PECL oscillator

This is the most expensive method but least risky in terms of layout and possible noise. As shown above, we've used single ended TTL in most of our reference designs with no adverse effects as long as careful attention is placed at design and layout stages. Use PECL drivers (or PECL Oscillator) if long traces are required, especially, if the clock is on a different board in your system.

Fig. 34 PECL oscillator driving long traces into REFCLK±



f) PECL oscillator driving two PECL single ended loads

Another alternative uses a single PECL source clock to drive two different PECL inputs. A PECL driver has two outputs , the +'ve and -'ve. Use the PECL oscillator 'out+' to drive one DUAL's REFCLK- , while the REFCLK+ is decoupled to ground with a 0.01µF capacitor. The PECL oscillator 'out-' is connected to the other DUAL's REFCLK-. Appropriate terminations are required in each case. PECL oscillators tend to be more expensive than the combined costs of a TTL oscillator and a buffer. is required. However, if the traces are long, or off-board, a good choice would be a PECL oscillator and PECL buffers if there are multiple loads.

3.19. How accurate should the on board reference clock be?

The on board reference clock is required to provide an alternative timing reference in the event that the primary timing reference becomes unavailable. For example, if the network equipment (NE) is configured for line timing mode in which the transmitted signals are timed from the clock derived from the received signal, the alternative timing reference allows the NE to provide the capability to switch to the secondary clock if the incoming signal becomes unsuitable to derive the clock from. For interfacing between WAN equipment, or between private and public ATM equipment, the Bellcore specification GR-CORE-253, Issue 2, Dec. 2,1995, Section 5.4.1 , requires the accuracy of the on board reference clock to be +/- 20 ppm or better. In an interface between private ATM user devices and private ATM network equipment, the ATM Forum specification "ATM PHYsical Medium Interface Specification for 155 Mbit/s over Twisted Pair Cable", version 1.0 Ballot Draft, 1994, requires the transmitter at the ATM user device to have a free-running transmit reference clock at 155.52 Mbit/s with an accuracy of +/- 100 ppm or better. In the DART board design, a TTL 19.44 MHz oscillator is used as a reference from which the 155.52 Mb/s is generated without loss of clock accuracy. Some of the vendors that provide these 19.44 MHz oscillators are listed below:

Vendor	+/-20ppm or better	+/-100ppm
Motron Industries 605-665-9321	Yes	Yes
Connor Winfield 708-851-4722	Yes	Yes
K&L Oscillatek	Yes	Yes
Champion 708-451-1000	Yes	Yes
Oak Frequency Control Group 717-486-3411	Yes	Yes
Ecliptek 714-433-1200	No	Yes

Table 3: 19.44 MHz Oscillator Vendors

3.20. CMOS vs. TTL terminology?

TTL vs. CMOS terminology may be a little confusing due to the evolution of the naming convention. Even though these refer to semiconductor family types, it's the voltage levels of the logic highs and lows that are important. Their speed in the application is also relevant.

The letter 'T' in the device prefix usually means that the IC's input thresholds are set at the traditional levels. That is a zero will be decoded if the voltage is lower than 0.4 volts. And a logic high will be decoded if the input detects 2.0 volts or more.

The letter 'C' in the prefix means that the device outputs will switch from Vss to Vcc power rails (typically zero to 5 volts depending on loading). TTL is not guaranteed to drive past 2.4V and a pull may be required if interfacing to other types of logic like PECL or CMOS.

DEVICE EXAMPLES

	Relative Speed & Slew Rate	CMOS Outputs High = 5V	CMOS Level Inputs 1/2 Vcc	TTL Level Outputs Hi>2.4V Low<0.8V	TTL Level Inputs Hi > 2.0V Low <0.4V
74C541	slowest	Yes	Yes	Yes	No
74LS541	slower	No	No	Yes	Yes
74S541	slow	No	No	Yes	Yes
74HC541	faster	Yes	Yes	Yes	No
74F541	fast	No	No	Yes	Yes
74FCT541	fastest	Yes	No	Yes	Yes

We chose to use the 74FCT541 since it has the fastest output slew rate, low power, TTL inputs and drives to the rails.

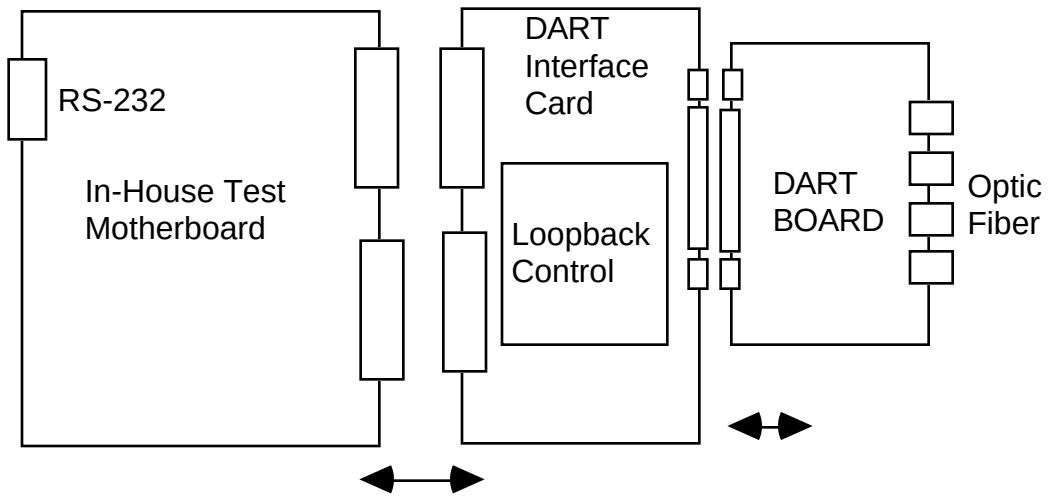
4. ACCESSING the DART board

4.1. DART board via DART Interface Card to SCI-PHY Mother Board

The arrangement below was used to test the functionality of the DART board. The SCI-PHY motherboard is a standard PMC-Sierra controller that allows access to the DART board's DUAL IC registers and. This motherboard also incorporates SAR functionality which provides a means of transmitting and receiving ATM cells via the SCI-PHY 16-bit bus. At 50 MHz FIFO clock, this motherboard is capable of servicing all four logical PHY devices running at 155.52 Mbits/s (OC-3) line rates.

The DART Interface Card was specially designed for the DART board to allow for connector pinout differences, power input, and to allow for simple drop side digital loop back, as outlined below in the next section.

Fig. 35 Testing the DART board



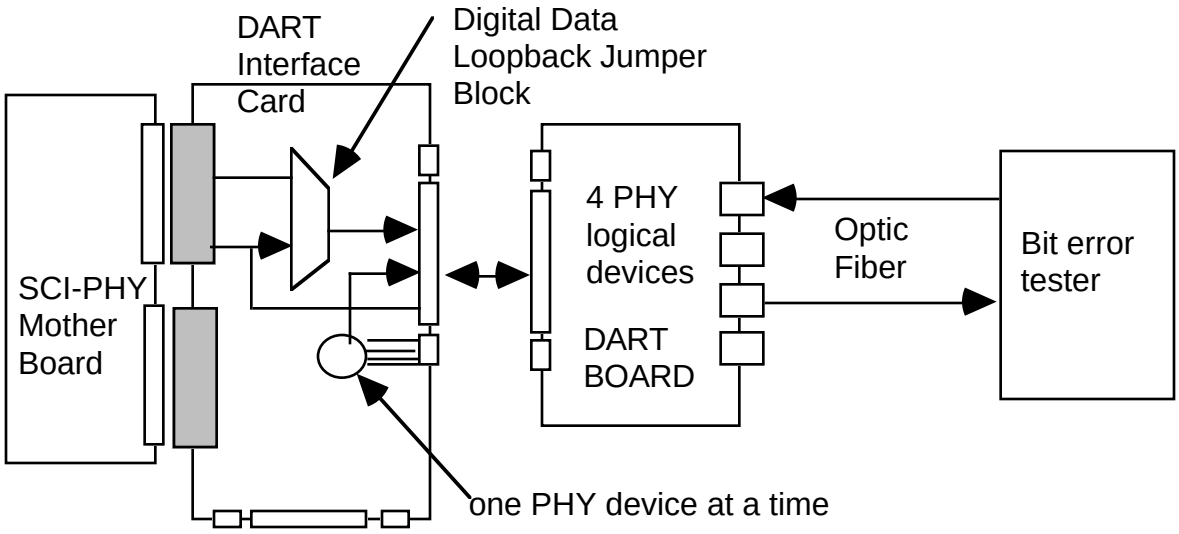
4.2. Drop side loop-back

The Interface Card provides capability for drop-side digital loop back of one PHY device at a time. Any one of the PHY RX FIFO stream can be routed to any one of the four TX FIFOs. Because we wanted to run the 16-bit bus at 50 MHz, we could not tolerate gate delays. A simple mechanical loop back jumper connector shorts out the RX 16 -bit PHY bus to the TX bus. A mechanical switch selects which PHY is the FIFO source, and another switch selects the destination PHY. Only one PHY is the source and one PHY is the destination at any one time.

The SCI-PHY motherboard can be connected to the Interface Card at all times in order to be able to configure and monitor the PHY Devices.

An external Line Bit Error tester generates SONET ATM cells and drives them into the optical Input. The RX FIFO cells are routed back to the TX FIFO through the jumper block. The PHY device then transmits the cells back to the Bit Error Tester via the optical transceiver.

Fig. 36 Drop side loop-back



5. PM5348 S/UNI-DUAL

For electrical, mechanical and register details, please refer to the S/UNI-DUAL PM5348 Data Sheet available either from your local PMC-Sierra Inc. Representative or from our Web Page at:

http://www.pmc-sierra.com

The PM5348 Dual User Network Interface (S/UNI-DUAL) is a monolithic integrated circuit that implements SONET/SDH processing and ATM mapping functions for two 155 Mbit/s or 51 Mbit/s ATM User Network Interfaces. It is fully compliant with SONET and SDH requirements and ATM Forum User Network Interface specifications. The S/UNI-DUAL is software configurable, allowing feature selection without changes to external wiring.

The S/UNI-DUAL receives two SONET/SDH channels via separate bit serial interfaces, recovers their corresponding clock and data, and processes section, line and path overhead for each channel. Each channel performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M0 or M1, G1) are also accumulated for each channel. Each channel of the S/UNI-DUAL interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

Each channel of the S/UNI-DUAL frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. Legitimate ATM cells are written to a four cell FIFO buffer.

The ATM cells are read from each channel's FIFO via a synchronous interface with cell-based handshake using either a split 8 bit wide datapath, a direct 8 bit wide datapath or a direct 16 bit wide datapath. Counts of received ATM cell headers that are errored and uncorrectable, those that are errored and correctable, and all passed cells are accumulated independently for each channel's performance monitoring purposes.

The S/UNI-DUAL transmits two SONET/SDH channels via separate bit serial interfaces and formats section, line, and path overhead for each channel. Each channel performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (M0 or M1, G1) are also inserted.

Each channel of the S/UNI-DUAL generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. It supports the insertion of a variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics.

ATM cells are written to each channel's internally programmable-length 4-cell FIFO via a synchronous interface using either a split 8 bit wide datapath, a direct 8 bit wide datapath, or a direct 16 bit wide datapath. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cellEach channel of the S/UNI-DUAL generates the header check sequence and scrambles the payload of the ATM cells. Payload scrambling can be disabled. No line rate clocks are required directly by the S/UNI-DUAL as it synthesizes the transmit clock and recovers the receive clocks using a single 19.44 MHz or 6.48 MHz reference clock.

The S/UNI-DUAL is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. It is implemented in low power, +5 Volt CMOS technology. It has TTL and PECL compatible inputs, has TTL/CMOS compatible outputs and is packaged in a 160 pin MQFP package.

5.1 S/UNI-DUAL register address map

For register details, please refer to the S/UNI-DUAL PM5348 Data sheet available either from your local PMC-Sierra Inc. Representative or from our Web Page at:

http://www.pmc-sierra.com

The microprocessor interface provides access to the S/UNI-DUAL device registers via the 140-pin SCI-PHY connector. The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-DUAL.

The S/UNI-DUAL address space extends from 0x000H to 0x1FFH. Of the 9 address bits, address bit 8 (A8) being the most significant bit and A0 being the least significant bit) is set low to access the S/UNI-DUAL normal mode register space .

APPENDIX A: PCB LAYOUT NOTES

A.1. Background

The DART board is a 6-layer board that has both through-hole and SMT (surface mount technology) components. The large IC are placed on the top side and most of the discrete devices are located on the solder side with power and ground planes buried internally. All routing traces are located on the two external sides for accessibility reasons.

Layer	Schematic Label	Description
1	Component side	signal traces and mainly components
2	TA	is the Transmit Ground (labeled 'TA')
3	D	is the ground and power respectively.
4	VCC	+5 volt power plane
5	RA	Receive Ground Plane
6	Solder Side	signal traces and discrete components

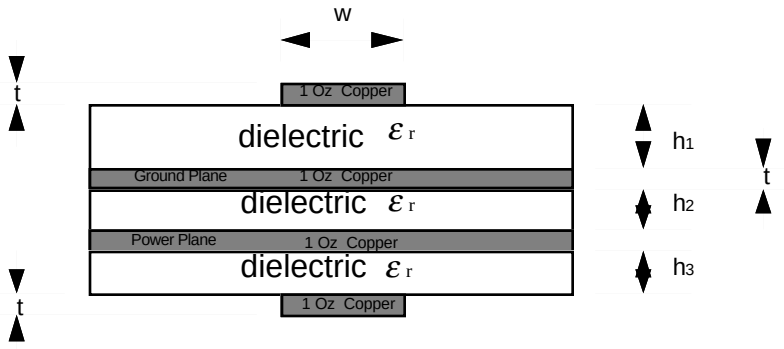
A.2. Trace Impedance Control

To reduce signal degradation due to reflection and radiation, the impedance of the traces that carry high speed signals such as transmitted and received data should be treated as microstrip transmission lines and terminated with matching impedance. The trace width is calculated using the formula

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

based on the following layer setup:

Fig. 37 Printed Circuit Board Stacking



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected.

For 1 oz copper, the thickness is 1.4 mil (2 oz = 2.88mil). This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The parameters h1, h2, and h3 can be specified. For example, if a 20 mil (including the copper thickness on both sides of the board) two layer core is selected, dielectric material that has the same relative dielectric constant can be added to both sides of the core to construct a 4 layer board.

Since all the controlled impedance traces are on the component side, only h1 is relevant in calculating the trace width. The calculation for the reference design is shown in the tables below:

Parameters	**Nominal**
Board Thickness (mil)	62 (including copper thickness)
Separation between layers 1 and 2 (mil)	10
Separation between layers 2 and 3 (mil)	30.5
Separation between layers 3 and 4 (mil)	10
Relative dielectric constant	4.2

Parameter	Data
ε_r	4.2
h (mil)	10
t (mil) for 1oz	1.4
Zo (Ohm)	50
W (mil)	17

Since h1 is proportional to the width of the traces, a small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

The low speed signals use 8 to 10 mil traces. Power and ground traces should be made as wide as possible to reduce the line inductance. All 50 Ohm traces are 17 mils wide.

A.3. Routing

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

- Turns and corners should be rounded to curves to avoid discontinuity in the signal path.
- Allow at least 10 mil clearance among vias, traces, and pads to prevent short and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements. For the traces that run between pads of the 140 pin edge connector, clearance of 6 mil and trace width of 8 mil can be used. However, the number and lengths such traces should be kept to a minimum.
- The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs.
- Even though single ended inputs should not run parallel to one another in close proximity, all of the single ended signals that run parallel to one another on the dropside interface are low speed signals and are sampled after they have all settled down; therefore, they should not cause any concern.
- All power and ground traces should be made as wide as possible to provide low impedance paths for the supply current as well as to allow quick noise dissipation.
- The oscillator used in a 14 pin DIP package. The connections to the oscillator are setup so that an oscillator with a smaller footprint (8 pin) can also be plugged in. An FCT541 buffer with series source terminations must be used.
- Since vias have an impedance, avoid them where possible, especially on critical traces such as TXD± and RXD±. Also where decoupling is critical, try to place capacitors at the pins (component side) and not have vias in series with the capacitors.

APPENDIX B: DART BOARD DROP SIDE CONNECTOR PINOUT

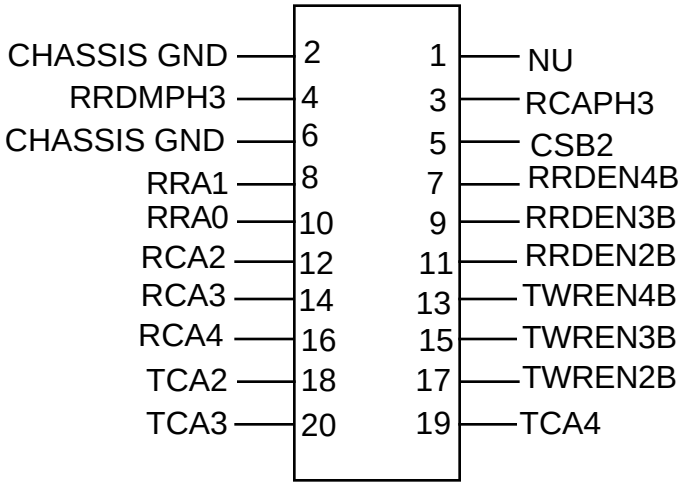
The system connector interfaces this DART board to the local ATM layer drop side controller. It has a total 140-pins to allow for the following functionality:

- 8 bit micro controller interface
- power, 5Vdc, ±10%
- ground
- control logic to four logical PHY devices
- 16 bit wide TX and RX parallel FIFO access and control via SCI-PHY bus

The DART SCI-PHY edge connector interface includes all the signals required to connect the DART board to a high layer protocol entity (i.e. AAL processor). Cells can be written to the S/UNI-DUAL/s transmit FIFO and read from the S/UNI-DUAL/s receive FIFO using this interface. The edge connector is made up of one 100 pin and two 20 pin dual line female connectors as shown in table below for a total of 140 pins. It consists of signals appropriate to read and write to the registers of the two DUAL devices on the daughter board, and it provides the necessary power and ground. TTL signal levels are used on this interface.

Since there are four logical PHY devices on the DART board, J1, J2 and J3 below have four sets of PHY control signals such as RCA, TCA, RRDENB, and TWRENB.

Fig. 38 DART board Expansion Connector



NU=Not Used on This board but defined

J1 20-PIN EXPANSION PHY CONTROL SIGNALS

Signal Name	Type	PIN	Function
NC	NC	1	Reserved
CHASSIS GND	Power	2 6	Safety ground used by Interface devices such as the Fiber Optic Transceiver or UTP-5 Electrical Line interface.
RCAMPH3	NC	3 4	Not used on DART board, no connect.
CSD2B	Input	5	Active low, PHY 8 bit microprocessor chip select used to select U3, S/UNI-DUAL #2 internal registers. Chip select for DUAL #1 is on pin 89 of J3, the 100 pin connector
RRDEN4B RRDEN3B RRDEN2B	Input	7 9 11	Active low Receive Read Enable used to enable reading the S/UNI receive FIFO of PHY device # 2,3 or 4. See J3 pin 47 for RRDEN1B. The active low receive read enable Input (RRDEN1B) is used to initiate reads from one logical PHY device on the SUNI-DUAL receive FIFO. When sampled low using the rising edge of RFCLK, a word is read from the SUNI-DUAL internal synchronous FIFO and output on the RDAT[15:0] bus. When sampled high using the rising edge of RFCLK, no read is performed. RRDENxB must operate in conjunction with RFCLK to access the SUNI-DUAL FIFO at a high enough instantaneous rate (≥ 19.44 MHz)as to avoid FIFO overflows. The ATM layer device may deassert RRDEN1B at anytime it is unable to accept another byte. When the RCA signal is configured to be de-asserted with zero octets (as opposed to four) in the SUNI-DUAL FIFO, it is not an error condition to hold the read enable (RRDEN1B) active. In this situation, the RCA signal identifies the valid octets.
RRA1 RRA0	Input	8 10	Not used on DART board, defined for RCMP Board. It's a UTOPIA Level 2 address bit 1 & 0.

RCA2 RCA3 RCA4	Output	12 14 16	Active high receive cell available (RCA) signal (polarity selectable in S/UNI-DUAL) indicates when a cell is available on the first logical PHY device. Used by S/UNI chip to notify the hardware on the drop side that there is at least one ATM cell ready to be read out of the receive FIFO. RCA can be configured to be de-asserted when either zero or four words remain in the S/UNI-DUAL FIFO. RCA is updated on the default rising edge of RFCLK but it's active edge is programmable.
TWREN4B TWREN3B TWREN2B	Input	13 15 17	The active low transmit write enable Input (TWRENB) is used to initiate writes to the SUNI-DUAL transmit FIFO. When sampled low using the rising edge of TFCLK, the word on TDAT[15:0] is written into the SUNI-DUAL transmit FIFO. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53 octet cell must be written to the SUNI-DUAL transmit FIFO before it is inserted into the SPE.
TCA2 TCA4 TCA3	Output	18 19 20	The transmit cell available (TCA) signal indicates when a cell is available in the S/UNI-DUAL transmit FIFO. When high, TCA indicates that the S/UNI-DUAL transmit FIFO is not full and a complete cell may be written in. When TCA goes low, it indicates either that the S/UNI-DUAL transmit FIFO is near full and can accept no more than four writes or that the transmit FIFO is full. Selection is made using a register bit in the S/UNI-DUAL TACP FIFO Control register. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the S/UNI-DUAL TACP FIFO Control register. If the programmed depth is less than four, additional cells may be written after TCA is asserted. TCA is updated on the rising edge of TFCLK. The active polarity of this signal is programmable in the S/UNI-DUAL and defaults to active high. TCA1 is on pin 18 of 100 pin connector

J2 20-PIN EXPANSION CONNECTOR

Signal Name	Type	PIN	Function
RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	1 2 3 4 5 6 7 8	RDAT[15:8] is the high order byte of the Received FIFO cell word RDAT[15:0]. Please refer to the S/UNI-DUAL data sheet for the 27 word cell data structure.
RXPRTY1	Output	9	Programmable function receive parity bit. In 16 bit mode, it's the receive parity bit for the Receive Data Bus RDAT[15:0] . In split bus mode, this is the parity bit for channel 2 of RDAT[15:8] . In 8-bit bus mode it is not used.
GND	Power	10 11	Ground (used as analog and digital ground)
TXPRTY1	Input	12	Programmable function transmit parity bit input for the transmit ATM cell Data Bus. In 16 bit mode, it's the parity bit of TDAT[15:0] . In 8-bit split bus mode, this is the parity for channel #2 of TDAT[15:8]. In 8-bit bus mode, this is not used.
TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	INPUT	14 13 16 15 18 17 20 19	TDAT[15:8] is the high order byte of the Transmit FIFO cell word RDAT[15:0]. Please refer to the S/UNI-DUAL data sheet for the 27 word cell data structure.

J3 100-PIN CONNECTOR

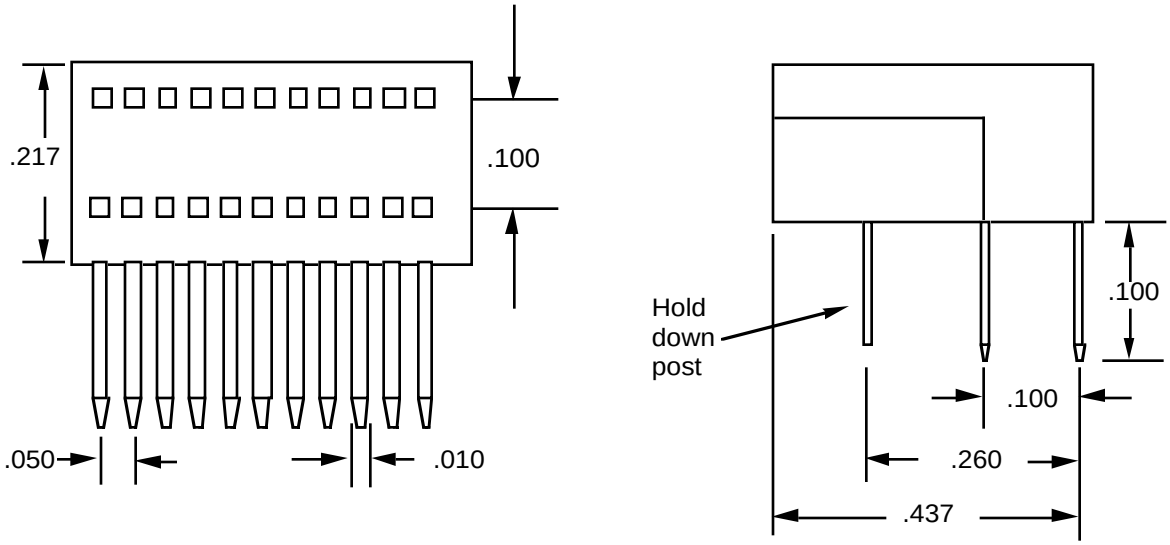
Signal Name	Type	PIN	Function
GND	Power	1,2,13 ,16,17 ,20,21 ,24,25 ,28,29 ,41,44 ,45,48 ,49,52 ,53,56 ,57,69 ,70,75 ,76,81 ,82,90 ,91,94 ,95,99 ,100	Ground, used on PCB as Digital Ground(D), Transmit Analog Ground (TA) and Receive Analog Ground (RA)
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7]	Input	3 5 9 11 4 6 10 12	TDAT[7:0] is the low order byte of the transmit FIFO cell word TDAT[15:0]. Please refer to the S/UNI-DUAL data sheet for the 27 word cell data structure.
TXPRTY0	Input	14	Programmable function transmit parity input bit for the transmit ATM cell Data Bus. This input is ignored in 16 bit mode. In 8-bit split bus mode, this is the parity for channel #1 of TDAT[7:0]. In 8-bit bus mode, the parity of TDAT[7:0] and input TXPRTY[0] is checked.
VCC	Power	7,8,35 36,63, 64,85, 86	+5 Volts DC Power
TSOC	Input	15	The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[15:0] bus. When TSOC is high, the first octet of the cell is present on the TDAT[15:0] stream. It is not necessary for TSOC to be present at each cell. An interrupt may be generated on the INTB signal if TSOC is high during any byte other than the first byte. TSOC is sampled on the rising edge of TFCLK

TCA1	Output	18	See pin 18,19,20 of J1 for TCA description
NC		19 23 26 42 51 54 55 62 83 87	No Connect
TFCLK	Input	22	The transmit write clock (TFCLK) is used to write ATM cells to the SUNI-DUAL four cell transmit FIFO. TFCLK cycles at a 50MHz or lower instantaneous rate. A complete 53 octet cell must be written to the SUNI-DUAL FIFO before being inserted in the synchronous payload envelope (SPE). TDAT[15:0], TXPRTY, TWRENB and TSOC are sampled on the rising edge of TFCLK. TCA is updated on the rising edge of TFCLK.
TWREN1B	Input	27	See description of J1 pin 13, 15,17
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7]	Output	31 33 37 39 30 32 38 40	RDAT[7:0] is the low order byte of the Received FIFO cell word RDAT[15:0]. Please refer to the S/UNI-DUAL data sheet for the 27 word cell data structure.
RXPRTY0	Output	34	Programmable function receive parity bit. In 16 bit mode, this pin is held low. In split bus mode, this is the parity bit for for channel #1 on RDAT[7:0] . In 8-bit bus mode, this is the parity bit for both channels.
RSOC	Output	43	The receive start of cell (RSOC) signal marks the start of cell on the RDAT[15:0] bus. When RSOC is high, the first octet of the cell is present on the RDAT[15:0] stream. RSOC is updated on the rising edge of RFCLK.
RCA1	Output	46	See J1 pin 12,14, & 16 for full description.
RRDEN1B	Input	47	See connector J1 pins 7,9 & 11 for details on the other three RRDENxB signals

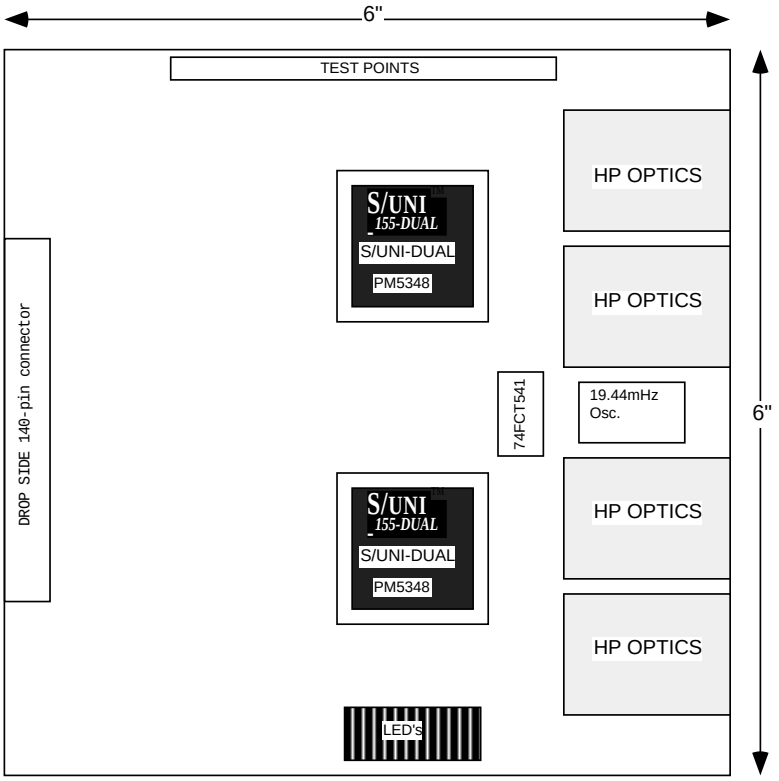
RFCLK	Input	50	The receive read clock (RFCLK) is used to read ATM cells from the SUNI-DUAL receive FIFO. RFCLK must cycle at a 50 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow (≥ 19.44 MHz @ 155.52 MHz line rate). RRDENB is sampled using the rising edge of RFCLK. RSOC, RDAT[15:0], RXPRTY and RCA are updated on the rising edge of RFCLK.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	59 61 65 67 58 60 66 68	The address bus A[7:0] selects specific registers during S/UNI-DUAL register accesses.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	Input & Output	71 73 77 79 74 78 80 84	The bi-directional data bus D[7:0] is used during by the local microprocessor to read and write to the S/UNI-DUAL control and status registers.
A[8]	Input	72	Address bit 8 used by S/UNI-DUAL. When low, the user accessible registers (0x000 to 0x0FF) are available to the local microcontroller. When high, the test mode registers (0x100 to 0x1FF) can be accessed. In normal operation only the lower 256 locations are defined and used.
INTB	Open Drain Output	88	The active low interrupt (INTB) signal goes low when a S/UNI-DUAL interrupt source is active, and that source is unmasked. The S/UNI-DUAL may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (RDI), loss of pointer (LOP), path AIS, path RDI and many others. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output. and must be pulled high with a resistor.
CSB1	Input	89	The active low chip select from the local uP must be low to access U2, S/UNI-DUAL #1 registers.
RSTB	Input	92	The active low reset (RSTB) signal provides an asynchronous S/UNI-DUAL reset.

RDB	Input	93	The active low read enable (RDB) signal is low during S/UNI-DUAL register read accesses. The S/UNI-DUAL drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
RDY		96	Not Used
WRB	Input	97	The active low write strobe (WRB) signal is low during a S/UNI-DUAL register write accesses. The D[7:0] bus contents are latched into the addressed register on the rising WRB edge while the selected CSB1 or CSB2 is low.
ALE	Input	98	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal S/UNI-DUAL address latches are transparent. It allows the S/UNI-DUAL to interface to a multiplexed address/data bus. The S/UNI-DUAL ALE has an integral pull up resistor. Not Used.

APPENDIX C: MECHANICAL DRAWINGS



AMP 101911-8 Edge Connector



PCB Board Dimensions

APPENDIX D: DART BOARD PARTS LIST

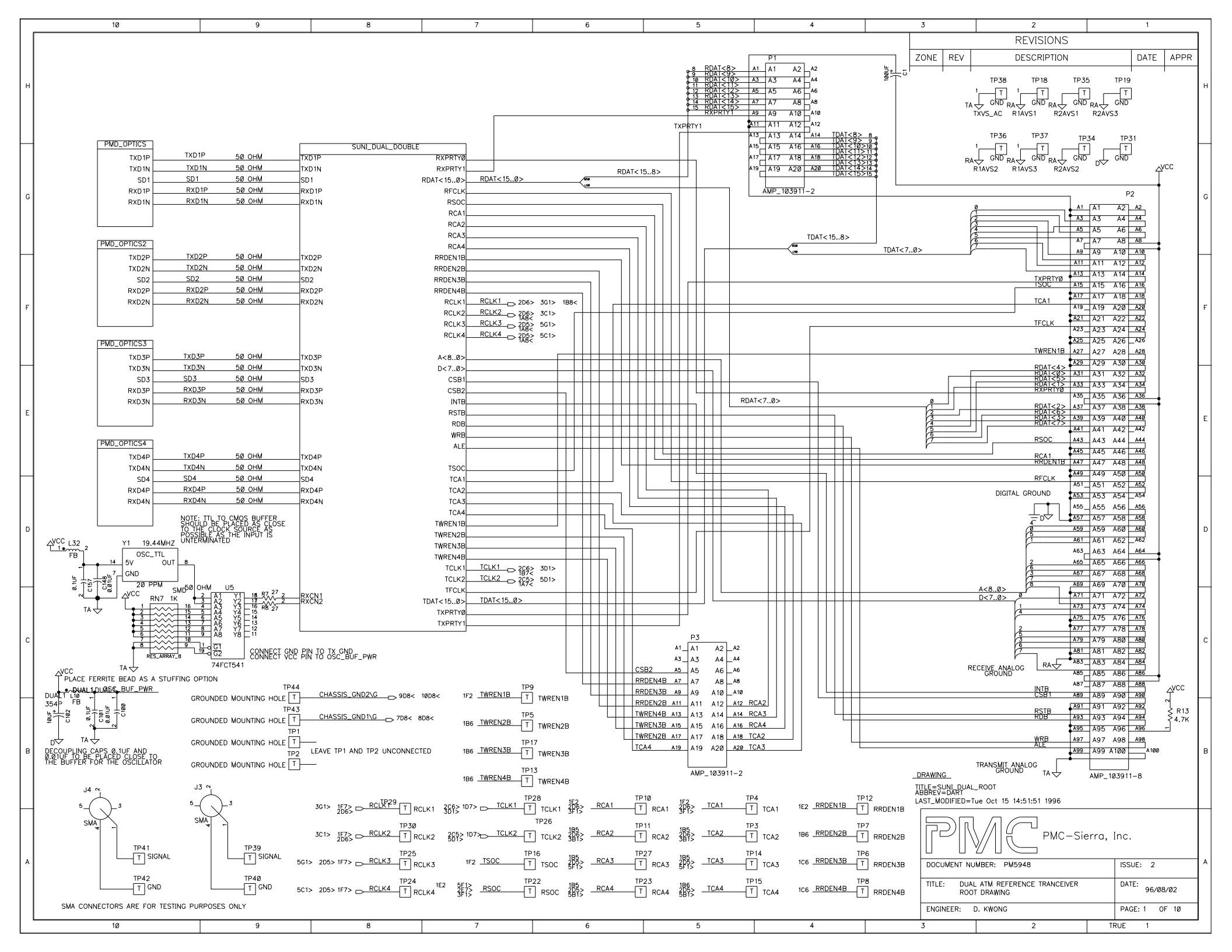
NO.	Part Name - Value	Part Number Description	Jedec Type	Ref Des	Qty
1	2N3904	SOT23-BASE	SOT23	Q1-Q4	4
2	74FCT541	74FCT541DW, FCT octal buffer	SOIC20W	U4, U5	2
3	1.0 µF CAP TANTALUM	Decoupling, 10 or 16V	CAP200	C89,C91,C117,C119	4
4	0.1µF CAP, CERAMIC	Ceramic, decoupling, high frequency	SMDCAP1206	C3,C7,C21,C25, C76,C80,C81,C83,	28
		Low ESR and low ESL		C85,C93-C96,C101,C107,C108,C110,	
				C112,C120-C123,C141,C142,C145	
				C146,C150,C151,C154,C155,C157	
5	0.01µF CAP, CERAMIC	Ceramic, decoupling, high frequency	SMDCAP805	C2,C5,C8-C12,C15-C19,C22,	84
		Low ESR and low ESL		C23,C27-C59,C64-C68,C73-C75,	
				C82,C84,C86-C88,C90,	
				C92,C103,C109-C111,C114-C116,	
				C118,C124,C128-C139,C148	
6	47PF CAP	NPO_805	SMDCAP805	C4,C20,C26,C113	4
7	100µF CAPACITOR,16V	ELECTROLYTIC	CAP320	C1	1
8	10 µF CAPACITOR,16V	TANT TEH	SMDTANCAP_C	C6,C13,C14,C24,C78,C98,C102	17
				C105,C126,C140,C143,C144,C147	
				C149,C152,C153, C156	
9	4.7µF X5R Ceramic SMT Cap.	Taiyo Yuden inc.		C60,C63,C69,C72,C79,C97,C106,C125	8
	NON-POLARIZED	PN# LMK316BJ475ML-B, 4.7¨F, 10V, X5R, 20%, 1206 size			
		see app note inside this document section 3.16 and 3.17 and Appendix E next for capacitor vendor sources			
10	CONN100-AMP_103911-8	AMP -- 103911-8	AMP_103911-8	P2	1
11	CONN20-AMP_103911-2	AMP_103911-2	AMP_103911-2	P1,P3	2
12	HEADER2-BASE	DIGI-KEY S1011-36-ND	JUMPER2	J1,J2	2
13	INDUCTOR-FB,50,	**FAIR-RITE PN# 2743019447**	INDUCTOR_FB	L3-L32	30
		DO NOT SUBSTITUTE	.18" by .12" by .12" high		
14	LCD_PMD-HPBR-5205	HP -- HPBR-5205	PMD-SOCKET	U6-U9	4
15	LED10-RED,25MA,2.1V		DIP20_LED	U1	1
16	19.44MHZ OSC, TTL, DIP	20 PPM, see app note	CRYS14	Y1	1
17	RESISTOR-100Ω,1%	SMD	SMDRES805	R3,R6,R11,R17,R51,R54,R58,R61	8
18	RESISTOR-200Ω,1%	SMD	SMDRES805	R40,R43,R45,R48	4
19	RESISTOR-237Ω,1%	SMD	SMDRES805	R1,R2,R4,R5,R9,R10,R12,R16,R87-R90	12
20	RESISTOR-27Ω,5%	SMD	SMDRES805	R7,R8	2
21	RESISTOR-330Ω,5%	SMD	SMDRES805	R66-R68,R72-R74,R78-R80,R84-R86	12
22	RESISTOR-4.7KΩ,5%	SMD	SMDRES805	R13-R15,R26, R29-R39,R44,R49	17
23	RESISTOR-49.9Ω,1%	SMD	SMDRES805	R64,R65,R70,R71,R76,R77,R82,R83	8
24	RESISTOR-68.1Ω,1%	SMD	SMDRES805	R52,R53,R59,R60	4
25	RESISTOR-681Ω,1%	SMD	SMDRES805	R63,R69,R75,R81	4
26	4.7KΩ RES_ARRAY_15pos	SMD	SOIC16	RN1-RN3,RN5	4
27	1KΩ RES_ARRAY_8_pos	SMD	SOIC16	RN4,RN6,RN7	3
28	SMA-BASE	Test Points only	SMA	J3,J4	2
29	SUNIDUAL PM5348	PMC-Sierra Inc.	PQFP160	U2,U3	2
30	TEST POINT HEADER	DIGI-KEY S1011-36-ND	TST_PT_1	TP3-TP17,TP19-TP35,TP39-TP42	1
	TOTAL COMPONENT COUNT				276

APPENDIX E: 4.7µF Ceramic Multilayer X5R and X7R Capacitor Sources

- ±20 % and ± 10% basic tolerance
- Stable X5R and X7R ±15% tolerance over temperature:
  (X7R rated from -55 to +125°C and X5R from -55°C to +85°C)
- small size Surface Mount, some may only be reflow qualified
- unpolarized
- Part #'s below are for bulk, check Data Sheet for other packaging

Manufacturer	Distributor's PN#	µF	%	Type	DCV	Footprint	Thick
Taiyo Yuden Inc.	EMK325BJ475MN-B	4.7	20%	X5R	16V	1210 (0.12" by .10")	1.9mm
	LMK316BJ475ML-B	4.7	20%	X5R	10V	1206 (0.12" by .06")	1.6mm
		special factory order for 10%					
	LMK316BJ475KL-B	4.7	10%	X5R	10V	1206 (0.12" by .06")	1.6mm
	EMK325BJ475KN-B	4.7	10%	X5R	16V	1210 (0.12" by .10")	1.9mm
	Manufacturer: Taiyo Yuden Inc. , 16-20 Ueno 6-chome, Taito-ku, Tokyo, Japan Phone: 03-3833-5441, FAX: 03-3835-4754						
	Rep.: Ty Bowman, Chicago, USA, 847-925-0888						
	Distributor : Canada; Electro Source, 6875 Royal Oak Rd., Burnaby BC, 604-435-2533 UK; Taiyo Yuden Westfield. London Road, High Wy. Combe Buckingham Shire HP11,1MA Phone:(44) 1494-464642 FAX: (44) 1494-474743						
TDK	CC1206JX5R475K	4.7	10%	X5R	6.3V	1206 (0.12" by .06")	
	(internal Manufacturer's PN # C3216X5R0J475K)						
	TDK Corp. of America: 1600 Feehanville Drive, Mount Prospect, Ill. USA 60056 1996 Edition Electronic Components Distributor Catalog page 15-20 Phone: (847) 803-6100 FAX: (847) 803-6296						
	Distributor: Enerlec Sales, Brenda, Richmond BC, Canada, 604-273-0882						
PHILIPS	2220RR475J8AB0C	4.7	5%	X7R	25V	2220 (0.22" by .20")	
	2220RR475K8AB0C	4.7	10%	X7R	25V	2220 (0.22" by .20")	
	2220RR475M8AB0C	4.7	20%	X7R	25V	2220 (0.22" by .20")	
	Philips Electronics Ltd., 601 Milner Avenue, Scarborough, Ontario, Canada Compact X7R Series Catalog Phone (416) 292-5161 FAX: (416) 292-4477						
AVX	SM015C475KAJ240	4.7	10%	X7R	50V	3230 (0.32" by .30")	
	SM015C475MAJ240	4.7	20%	X7R	50V	3230 (0.32" by .30")	
	AVX Corporation, Myrtle Beach, SC USA, SMPS Series Capacitors Catalog Phone: (803) 448-9411 FAX: (803) 448-1943						
	AVX Limited, Aldershot England Phone: (252-336868 FAX: 252-346643						
Prestidio	3736X7R475K1NT91A	4.7	many	X7R	25V	3736 (0.37" by .36")	
	Prestidio Components Inc., 7169 Construction Court, San Diego, CA USA 92121 EEM 1997 Catalog; page A1122-1123 Phone: (619) 578-9390 FAX: 1-800-538-3880						
Vitramon	VJ2225Y475JXXAT	4.7	5%	X7R	25V	2225 (0.22" by .25")	
	VJ2225Y475KXXAT	4.7	10%	X7R	25V	2225 (0.22" by .25")	
	VJ2225Y475MXXAT	4.7	20%	X7R	25V	2225 (0.22" by .25")	
	Manufacturer: Vitramon, #10 Route 25, Monroe, CT 06468, Mail: PO Box 544, CT 06601 Phone (203) 268-6261 FAX: (203) 452-5670						

APPENDIX F: SCHEMATICS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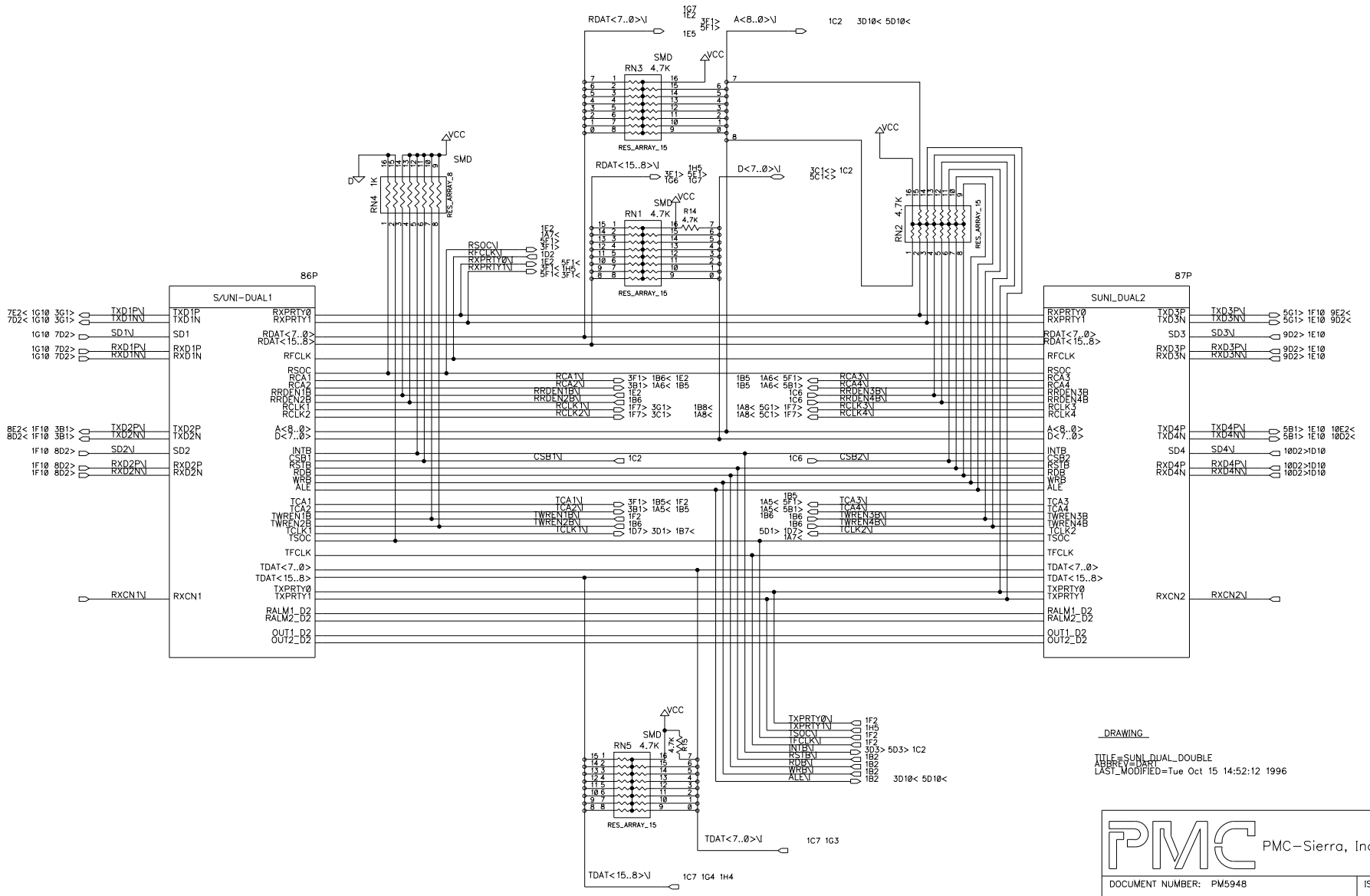
PMD_OPTICS2
PMD_OPTICS3
PMD_OPTICS4
SUNI_DUAL_DOUBLE
P1
P2
P3
AMP_103911-2
AMP_103911-8
NOTE: TTL TO CMOS BUFFER SHOULD BE PLACED AS CLOSE TO THE CLOCK SOURCE AS POSSIBLE AS THE INPUT IS UNTERMINATED
CONNECT GND PIN TO TX GND
CONNECT VCC PIN TO OSC_BUF_PWR
74FCT541
PLACE FERRITE BEAD AS A STUFFING OPTION
DUAL1.0UF5C_BUF_PWR
DECOUPLING CAPS 0.1UF AND 0.01UF TO BE PLACED CLOSE TO THE BUFFER FOR THE OSCILLATOR
GROUNDED MOUNTING HOLE
LEAVE TP1 AND TP2 UNCONNECTED
SMA CONNECTORS ARE FOR TESTING PURPOSES ONLY
DIGITAL GROUND
RECEIVE ANALOG GROUND
TRANSMIT ANALOG GROUND
DRAWING
TITLE=SUNI_DUAL_ROOT
ABBREV=DART
LAST_MODIFIED=Tue Oct 15 14:51:51 1996
PMC-Sierra, Inc.
DOCUMENT NUMBER: PM5948
ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER ROOT DRAWING
DATE: 96/08/02
ENGINEER: D. KWONG
PAGE: 1 OF 10

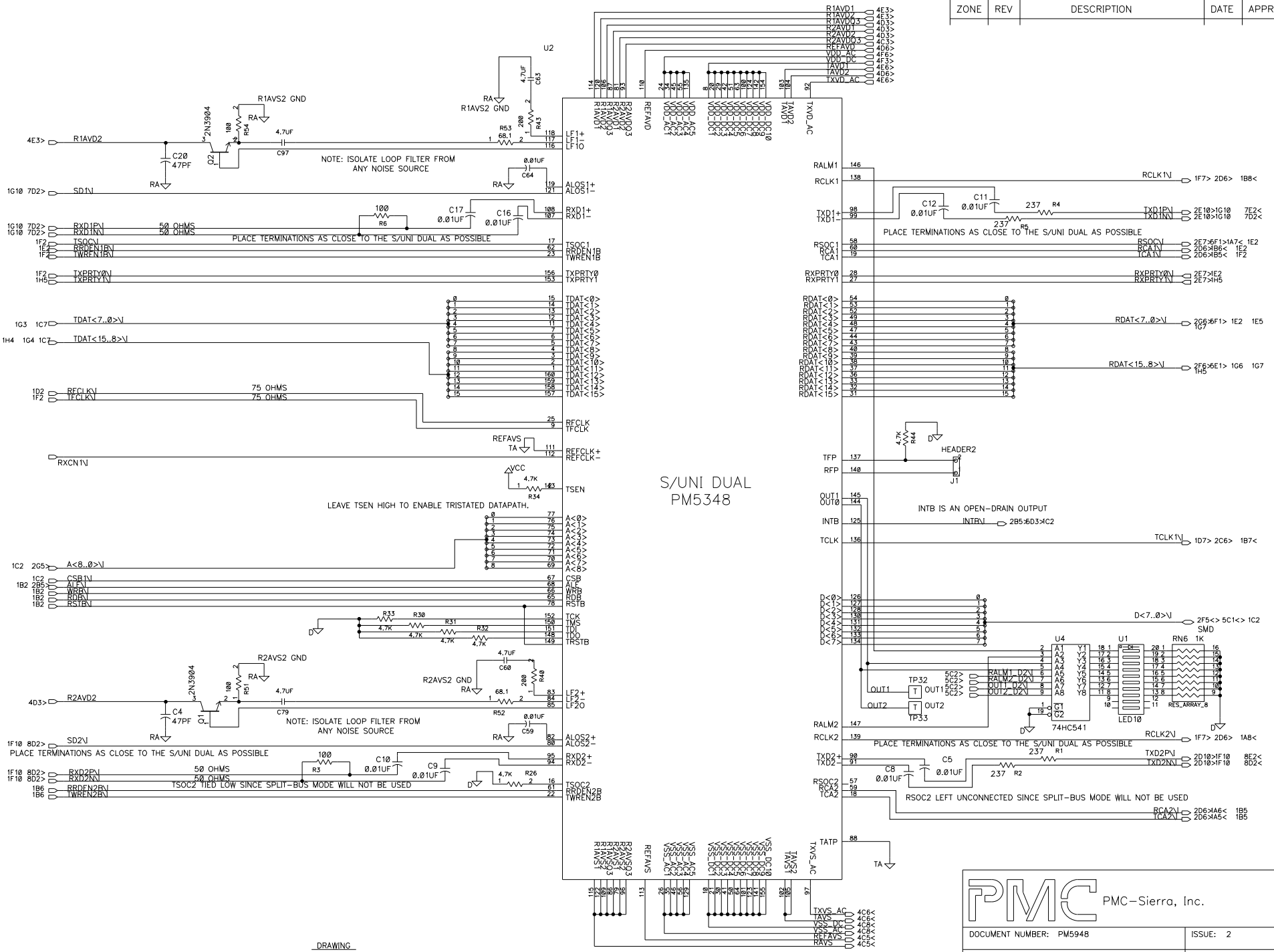
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

THIS PAGE PROVIDES PULL-UPS AND PULL-DOWNS FOR BOTH S/UNI-DUALS



PMC-Sierra, Inc.	
DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER S/UNI-DUAL PULL-UPS AND PULL-DOWNS	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 2 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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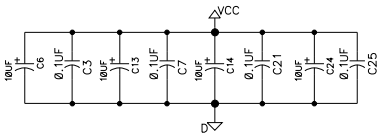
PMC-Sierra, Inc.

DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER S/UNI-DUAL #1	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 3 OF 10

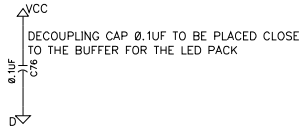
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

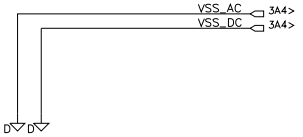
DART BOARD POWER FOR S/UNI-DUAL CHIP #1

POWER FOR CONNECTORS AND EXTERNAL CIRCUITRY

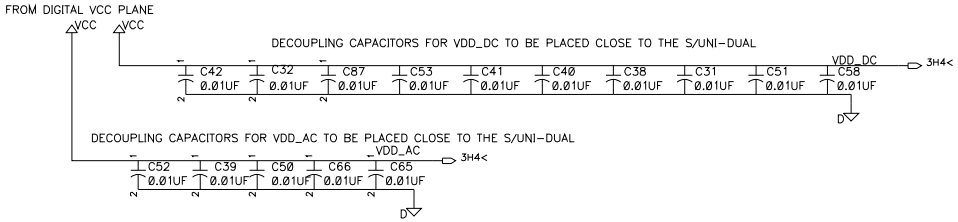


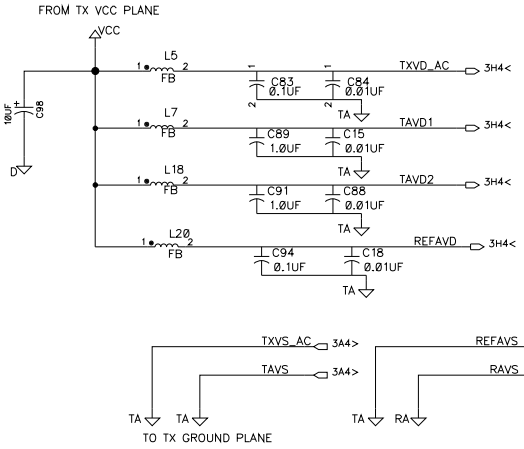
NOTE: DECOUPLING CAPACITORS FOR CONNECTOR P1

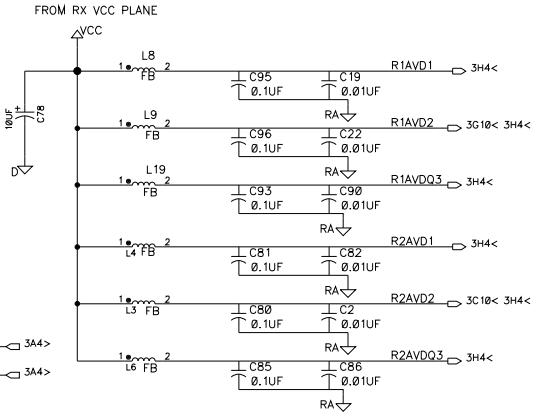




NOTE: VSS_AC AND VSS_DC ARE DIGITAL GROUND







BOARD CONSISTS OF ONE VCC PLANE AND THREE SEPARATE GROUND PLANES CONSISTING OF ONE DIGITAL GROUND PLANE DENOTED BY 'D', ONE TRANSMIT ANALOG GROUND PLANE DENOTED BY 'TA', AND ONE RECEIVE ANALOG GROUND PLANE DENOTED BY 'RA'

NOTE: ALL DECOUPLING CAPS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE SUNI_DUAL PINS.
THE BULK CAPS SHOULD BE PLACED AWAY FROM THE SUNI_DUAL PINS AND CLOSE TO THE FERRITE BEADS

DRAWING
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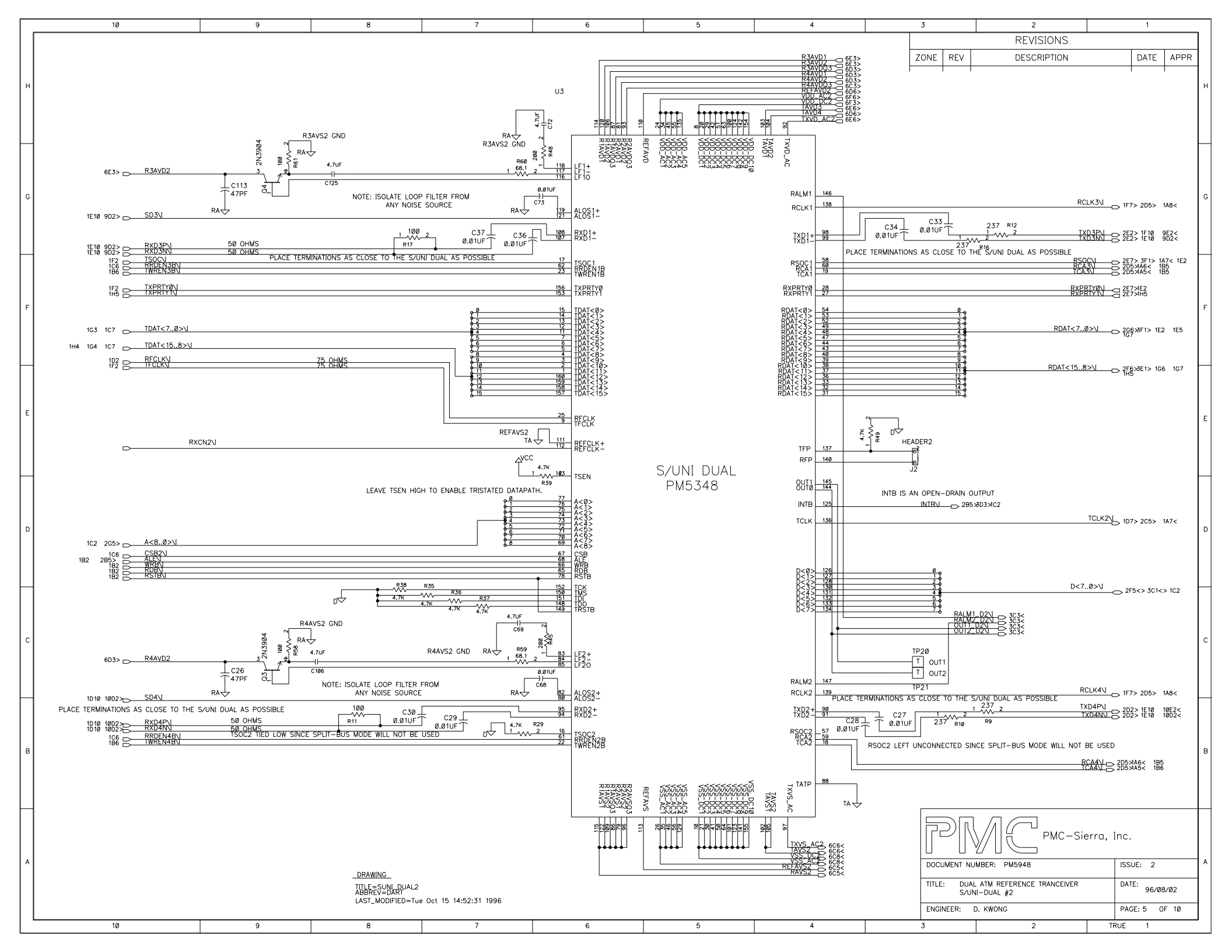
LAST_MODIFIED=Tue Oct 15 14:52:25 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER S/UNI-DUAL #1 + CONNECTOR POWER SUPPLY	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 4 OF 10


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
U3
S/UNI DUAL
PM5348
NOTE: ISOLATE LOOP FILTER FROM ANY NOISE SOURCE
PLACE TERMINATIONS AS CLOSE TO THE S/UNI DUAL AS POSSIBLE
LEAVE TSEN HIGH TO ENABLE TRISTATED DATAPATH.
INTB IS AN OPEN-DRAIN OUTPUT
RSOC2 LEFT UNCONNECTED SINCE SPLIT-BUS MODE WILL NOT BE USED
TSOC2 TIED LOW SINCE SPLIT-BUS MODE WILL NOT BE USED
R3AVS2 GND
R4AVS2 GND
VCC
HEADER2
TP20
TP21
PMC-Sierra, Inc.
DOCUMENT NUMBER: PM5948
ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER S/UNI-DUAL #2
DATE: 96/08/02
ENGINEER: D. KWONG
PAGE: 5 OF 10
DRAWING
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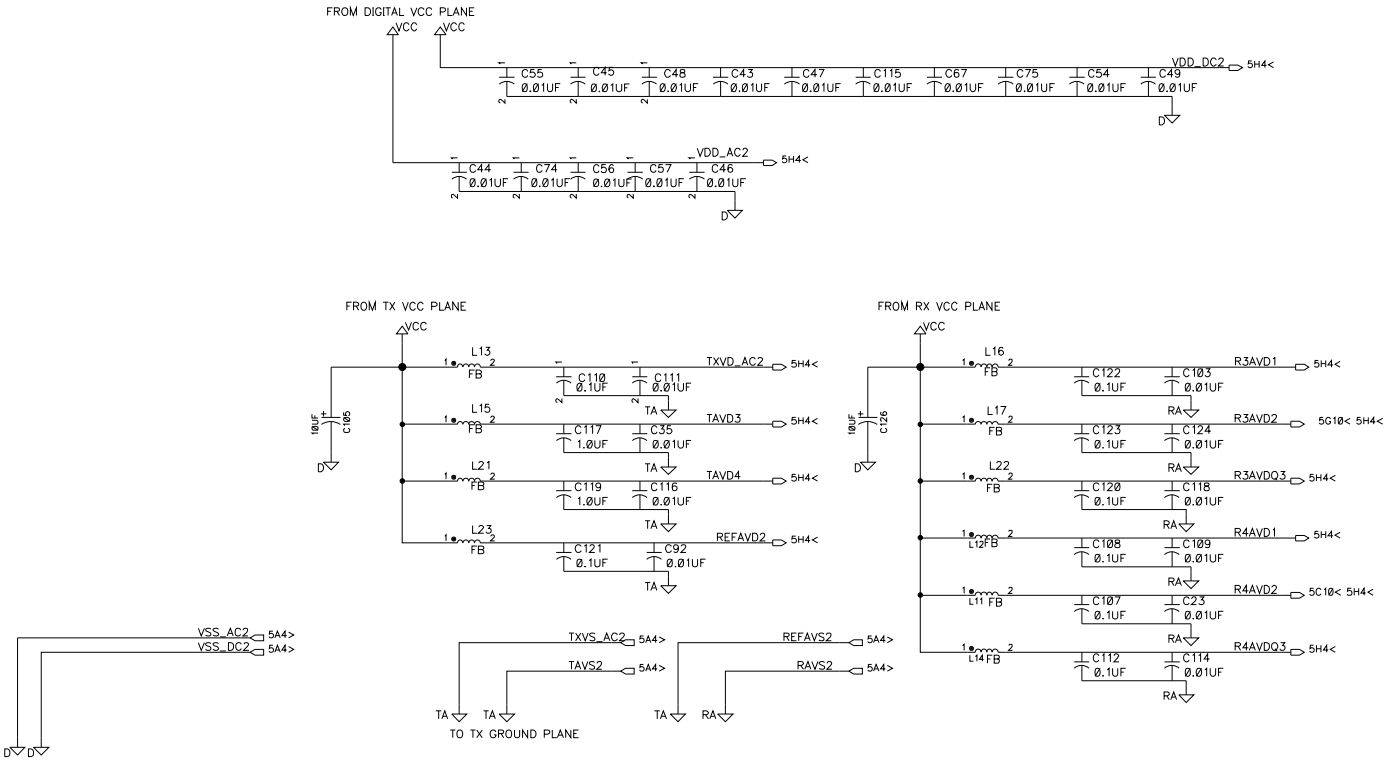
ABBREV=DART
LAST_MODIFIED=Tue Oct 15 14:52:31 1996

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DART BOARD POWER FOR S/UNI-DUAL CHIP #2



NOTE: VSS_AC AND VSS_DC ARE DIGITAL GROUND

BOARD CONSISTS OF ONE VCC PLANE AND THREE SEPARATE GROUND PLANES CONSISTING OF ONE DIGITAL GROUND PLANE DENOTED BY 'D', ONE TRANSMIT ANALOG GROUND PLANE DENOTED BY 'TA', AND ONE RECEIVE ANALOG GROUND PLANE DENOTED BY 'RA'

NOTE: ALL DECOUPLING CAPS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE SUNI_DUAL PINS.
THE BULK CAPS SHOULD BE PLACED AWAY FROM THE SUNI_DUAL PINS AND CLOSE TO THE FERRITE BEADS

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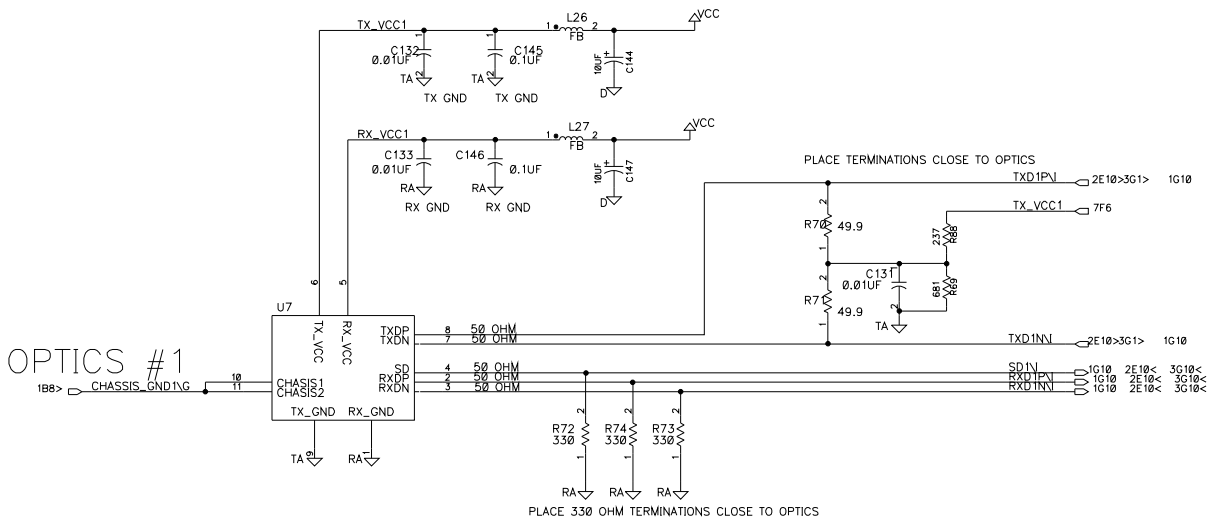
PMC-Sierra, Inc.

DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER S/UNI-DUAL CHIP #2 POWER SUPPLY	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 6 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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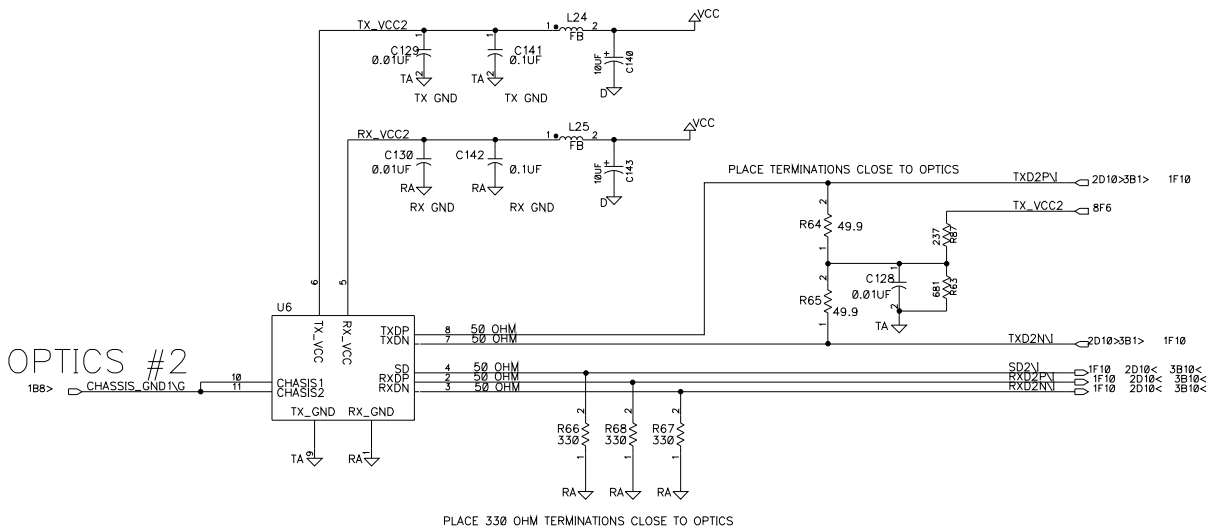
PMC-Sierra, Inc.

DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER OPTICS MODULE #1	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 7 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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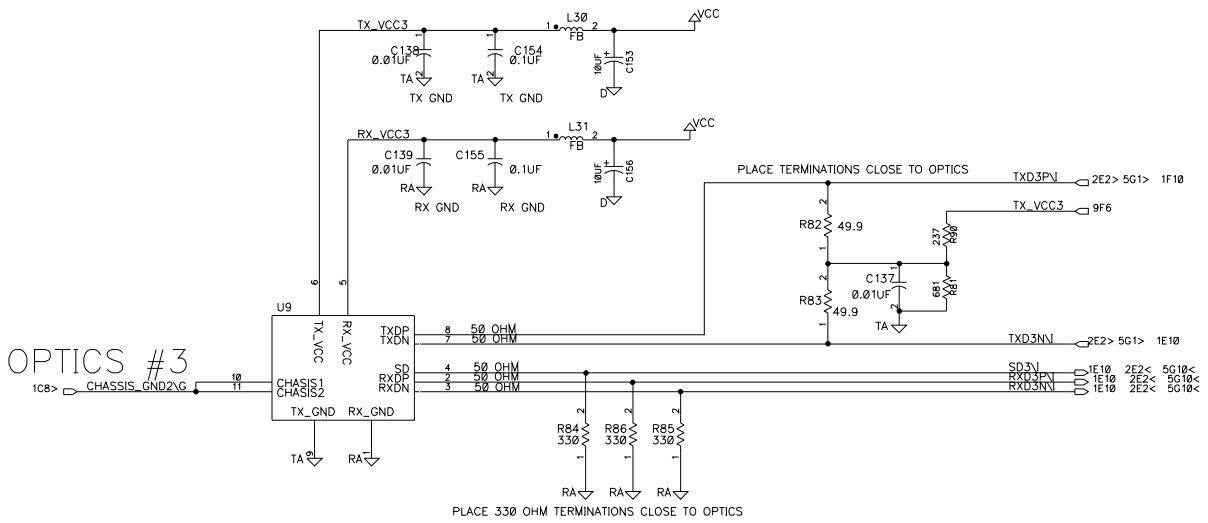
DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER OPTICS MODULE #2	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 8 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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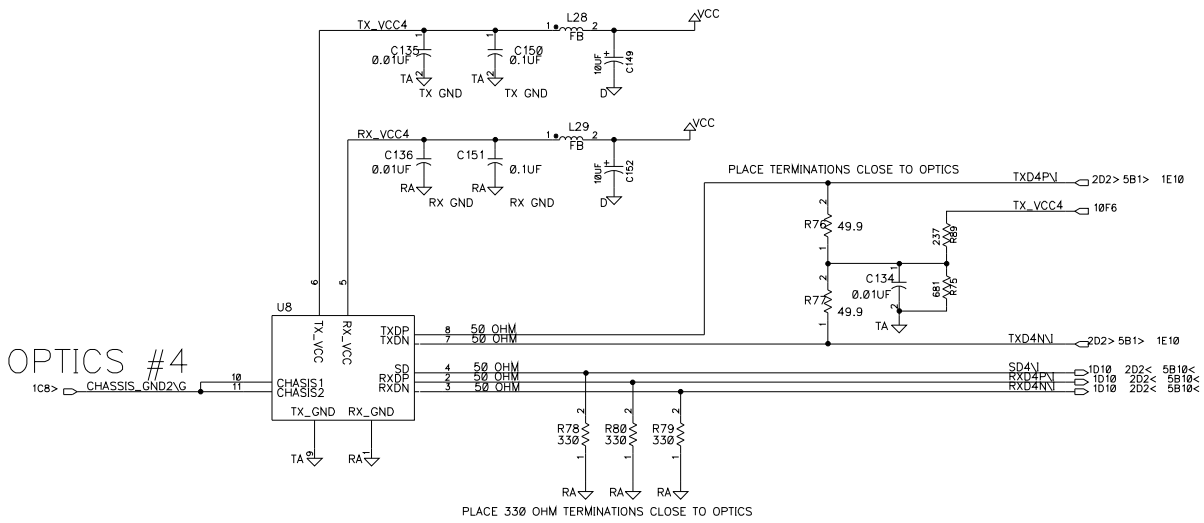
DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER OPTICS MODULE #3	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 9 OF 10

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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DOCUMENT NUMBER: PM5948	ISSUE: 2
TITLE: DUAL ATM REFERENCE TRANCEIVER OPTICS MODULE #4	DATE: 96/08/02
ENGINEER: D. KWONG	PAGE: 10 OF 10

APPENDIX G: SCHEMATIC COMPONENT CROSS REFERENCE

*** Unit Cross-Reference ***
--- for the entire design --

C1 CAPACITOR 1H3
C2 CAP 4D4
C3 CAP 4F10
C4 CAP 3C9
C5 CAP 3B3
C6 CAPACITOR 4F10
C7 CAP 4F10
C8 CAP 3B4
C9 CAP 3B7
C10 CAP 3B8
C11 CAP 3G3
C12 CAP 3G3
C13 CAPACITOR 4F10
C14 CAPACITOR 4F9
C15 CAP 4E6
C16 CAP 3G7
C17 CAP 3G7
C18 CAP 4D6
C19 CAP 4E4
C20 CAP 3G9
C21 CAP 4F9
C22 CAP 4E4
C23 CAP 6D4
C24 CAPACITOR 4F9
C25 CAP 4F9
C26 CAP 5C9
C27 CAP 5B3
C28 CAP 5B4
C29 CAP 5B7
C30 CAP 5B8
C31 CAP 4F4
C32 CAP 4F7
C33 CAP 5G3
C34 CAP 5G3
C35 CAP 6E6
C36 CAP 5G7
C37 CAP 5G7
C38 CAP 4F5
C39 CAP 4F7
C40 CAP 4F5
C41 CAP 4F6
C42 CAP 4F7
C43 CAP 6F6
C44 CAP 6F7
C45 CAP 6F7
C46 CAP 6F6
C47 CAP 6F6
C48 CAP 6F6
C49 CAP 6F4
C50 CAP 4F7
C51 CAP 4F4
C52 CAP 4F7
C53 CAP 4F6
C54 CAP 6F4
C55 CAP 6F7
C56 CAP 6F7
C57 CAP 6F6
C58 CAP 4F4
C59 CAPACITOR 3C6
C60 CAPACITOR 3C7
C63 CAPACITOR 3H6
C64 CAPACITOR 3G6
C65 CAP 4F6
C66 CAP 4F6
C67 CAP 6F5
C68 CAPACITOR 5C6
C69 CAPACITOR 5C7
C72 CAPACITOR 5H6
C73 CAPACITOR 5G6
C74 CAP 6F7
C75 CAP 6F4
C76 CAPACITOR 4E10
C78 CAPACITOR 4E5
C79 CAPACITOR 3C8
C80 CAP 4D4
C81 CAP 4D4
C82 CAP 4D4
C83 CAP 4E7
C84 CAP 4E6
C85 CAP 4C4
C86 CAP 4C4
C87 CAP 4F6
C88 CAP 4D6
C89 CAP 4E7
C90 CAP 4D4
C91 CAP 4D7
C92 CAP 6D6
C93 CAP 4D4
C94 CAP 4D7
C95 CAP 4E4
C96 CAP 4E4
C97 CAPACITOR 3G8
C98 CAPACITOR 4E8
C100 CAPACITOR 1B10
C101 CAPACITOR 1B10
C102 CAPACITOR 1B10
C103 CAP 6E4
C105 CAPACITOR 6E8
C106 CAPACITOR 5C8
C107 CAP 6D4
C108 CAP 6D4
C109 CAP 6D4
C110 CAP 6E7
C111 CAP 6E6
C112 CAP 6C4
C113 CAP 5G9
C114 CAP 6C4
C115 CAP 6F5
C116 CAP 6D6
C117 CAP 6E7
C118 CAP 6D4
C119 CAP 6D7
C120 CAP 6D4
C121 CAP 6D7
C122 CAP 6E4
C123 CAP 6E4
C124 CAP 6E4
C125 CAPACITOR 5G8
C126 CAPACITOR 6E5
C128 CAP 8D4
C129 CAP 8F6
C130 CAP 8E6
C131 CAP 7D4
C132 CAP 7F6
C133 CAP 7E6
C134 CAP 10D4
C135 CAP 10F6
C136 CAP 10E6
C137 CAP 9D4
C138 CAP 9F6
C139 CAP 9E6
C140 CAPACITOR 8F5
C141 CAP 8F5
C142 CAP 8E6
C143 CAPACITOR 8E5
C144 CAPACITOR 7F5
C145 CAP 7F5
C146 CAP 7E6
C147 CAPACITOR 7E5
C148 CAP 1C10
C149 CAPACITOR 10F5
C150 CAP 10F5
C151 CAP 10E6
C152 CAPACITOR 10E5
C153 CAPACITOR 9F5
C154 CAP 9F5
C155 CAP 9E6
C156 CAPACITOR 9E5
C157 CAPACITOR 1C10
J1 HEADER2 3E3
J2 HEADER2 5E3
J3 SMA 1B10
J4 SMA 1B10
L3 INDUCTOR 4D5
L4 INDUCTOR 4D5
L5 INDUCTOR 4E7
L6 INDUCTOR 4C5
L7 INDUCTOR 4E7
L8 INDUCTOR 4E5
L9 INDUCTOR 4E5
L10 INDUCTOR 1C10
L11 INDUCTOR 6D5
L12 INDUCTOR 6D5
L13 INDUCTOR 6E7
L14 INDUCTOR 6C5
L15 INDUCTOR 6E7
L16 INDUCTOR 6E5
L17 INDUCTOR 6E5
L18 INDUCTOR 4D7
L19 INDUCTOR 4D5
L20 INDUCTOR 4D7
L21 INDUCTOR 6D7
L22 INDUCTOR 6D5
L23 INDUCTOR 6D7
L24 INDUCTOR 8F5
L25 INDUCTOR 8E5
L26 INDUCTOR 7F5
L27 INDUCTOR 7E5
L28 INDUCTOR 10F5
L29 INDUCTOR 10E5
L30 INDUCTOR 9F5
L31 INDUCTOR 9E5
L32 INDUCTOR 1D10
P1 CONN20 1H4
P2 CONN100 1G1
P3 CONN20 1C5
Q1 2N3904_ 3C9
Q2 2N3904_ 3G9
Q3 2N3904_ 5C9
Q4 2N3904_ 5G9
R1 RESISTOR 3B2
R2 RESISTOR 3B3
R3 RESISTOR 3B8
R4 RESISTOR 3G2
R5 RESISTOR 3G3
R6 RESISTOR 3G8
R7 RESISTOR 1C9
R8 RESISTOR 1C9
R9 RESISTOR 5B2
R10 RESISTOR 5B3
R11 RESISTOR 5B8
R12 RESISTOR 5G2
R13 RESISTOR 1B1
R14 RESISTOR 2F6
R15 RESISTOR 2B6
R16 RESISTOR 5G2
R17 RESISTOR 5G8
R26 RESISTOR 3B6
R29 RESISTOR 5B6
R30 RESISTOR 3C7
R31 RESISTOR 3C7
R32 RESISTOR 3C7
R33 RESISTOR 3D8
R34 RESISTOR 3D6
R35 RESISTOR 5C7
R36 RESISTOR 5C7
R37 RESISTOR 5C7
R38 RESISTOR 5D8
R39 RESISTOR 5D6
R40 RESISTOR 3C6
R43 RESISTOR 3G6
R44 RESISTOR 3E3
R45 RESISTOR 5C6
R48 RESISTOR 5G6
R49 RESISTOR 5E3
R51 RESISTOR 3C9
R52 RESISTOR 3C7
R53 RESISTOR 3G7
R54 RESISTOR 3G9
R58 RESISTOR 5C9
R59 RESISTOR 5C7
R60 RESISTOR 5G7
R61 RESISTOR 5G9
R63 RESISTOR 8D3
R64 RESISTOR 8E4
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R66 RESISTOR 8D5
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R68 RESISTOR 8D5
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R71 RESISTOR 7D4
R72 RESISTOR 7D5
R73 RESISTOR 7D5
R74 RESISTOR 7D5
R75 RESISTOR 10D3
R76 RESISTOR 10E4
R77 RESISTOR 10D4
R78 RESISTOR 10D5
R79 RESISTOR 10D5
R80 RESISTOR 10D5
R81 RESISTOR 9D3
R82 RESISTOR 9E4
R83 RESISTOR 9D4
R84 RESISTOR 9D5
R85 RESISTOR 9D5
R86 RESISTOR 9D5
R87 RESISTOR 8E3
R88 RESISTOR 7E3
R89 RESISTOR 10E3
R90 RESISTOR 9E3
RN1 RES_ARRAY_15 2F6
RN2 RES_ARRAY_15 2E4
RN3 RES_ARRAY_15 2G6
RN4 RES_ARRAY_8 2F8
RN5 RES_ARRAY_15 2B6
RN6 RES_ARRAY_8 3C1
RN7 RES_ARRAY_8 1C10
TP1 TST_PT_BIG 1B9
TP2 TST_PT_BIG 1B9
TP3 TST_PT 1A5
TP4 TST_PT 1B5
TP5 TST_PT 1B7
TP6 TST_PT 1A4
TP7 TST_PT 1A4
TP8 TST_PT 1A4
TP9 TST_PT 1C7
TP10 TST_PT 1B6
TP11 TST_PT 1A6
TP12 TST_PT 1B4
TP13 TST_PT 1B7
TP14 TST_PT 1A5
TP15 TST_PT 1A5
TP16 TST_PT 1A7
TP17 TST_PT 1B7
TP18 TST_PT_SMALL 1H2
TP19 TST_PT 1H1
TP20 TST_PT 5C3
TP21 TST_PT 5C3
TP22 TST_PT 1A7
TP23 TST_PT 1A6
TP24 TST_PT 1A8
TP25 TST_PT 1A8
TP26 TST_PT 1A6
TP27 TST_PT 1A6
TP28 TST_PT 1B7
TP29 TST_PT 1B8
TP30 TST_PT 1A8
TP31 TST_PT 1H1
TP32 TST_PT 3C3
TP33 TST_PT 3C3
TP34 TST_PT 1H2
TP35 TST_PT 1H2
TP36 TST_PT_SMALL 1H2
TP37 TST_PT_SMALL 1H2
TP38 TST_PT_SMALL 1H2
TP39 TST_PT 1A9
TP40 TST_PT 1A9
TP41 TST_PT 1A10
TP42 TST_PT 1A10
TP43 TST_PT_BIG 1B9
TP44 TST_PT_BIG 1C9
U1 LED10 3C2
U2 SUNIDUAL 3H6
U3 SUNIDUAL 5H6
U4 74XXX541 3C2
U5 74XXX541 1C9
U6 LCD_PMD 8D7
U7 LCD_PMD 7D7
U8 LCD_PMD 10D7
U9 LCD_PMD 9D7

Y1 OSC_TTL 1D10

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPR

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TITLE: ?T ?T2	DATE: YY/MM/DD
ENGINEER: ?E	PAGE: ?P OF ?T

APPENDIX H: SCHEMATIC SIGNAL CROSS REFERENCE

*** Signal Cross-Reference ***
--- for the entire design --

```
A <8..0>        2G5> 1C2 3D10< 5D10<
ALE             2B5> 1B2 3D10< 5D10<
CHASSIS_GND1     1B8> 7D8< 8D8<
CHASSIS_GND2     1C8> 9D8< 10D8<
CSB1            1C2 2D6< 3D10<
CSB2            1C6 2D5< 5D10<
D <7..0>        2F5<> 3C1<> 5C1<> 1C2
INTB            2B5> 3D3> 5D3> 1C2
OSC_BUF_PWR      1C10>
OUT1            3C4
OUT1_D2          5C2> 3C3<
OUT2            3C4
OUT2_D2          5C2> 3C3<
R1AVD1          4E3> 3H4<
R1AVD2          4E3> 3G10< 3H4<
R1AVDQ3          4D3> 3H4<
R2AVD1          4D3> 3H4<
R2AVD2          4D3> 3C10< 3H4<
R2AVDQ3          4C3> 3H4<
R3AVD1          6E3> 5H4<
R3AVD2          6E3> 5G10< 5H4<
R3AVDQ3          6D3> 5H4<
R4AVD1          6D3> 5H4<
R4AVD2          6D3> 5C10< 5H4<
R4AVDQ3          6C3> 5H4<
RALM1_D2         5C2> 3C3<
RALM2_D2         5C2> 3C3<
RAVS            3A4> 4C5<
RAVS2           5A4> 6C5<
RCA1            2D6> 3F1> 1B6< 1E2
RCA2            2D6> 3B1> 1A6< 1B5
RCA3            2D5> 5F1> 1A6< 1B5
RCA4            2D5> 5B1> 1A6< 1B5
RCLK1           1F7> 2D6> 3G1> 1B8<
RCLK2           1F7> 2D6> 3C1> 1A8<
RCLK3           1F7> 2D5> 5G1> 1A8<
RCLK4           1F7> 2D5> 5C1> 1A8<
RDAT <15..0>    2F6> 2G6> 3E1> 3F1> 5E1> 5F1> 1E2
                  1E5 1G6 1G7 1H5
RDB             1B2 2B5< 3D10< 5D10<
REFAVD          4D6> 3H4<
REFAVD2         6D6> 5H4<
REFAVS          3A4> 4C5<
REFAVS2         5A4> 6C5<
RFCLK           1D2 2E7< 3E10< 5F10<
RRDEN1B          1B4< 1E2 2D6< 3F10<
RRDEN2B          1A4< 1B6 2D6< 3B10<
RRDEN3B          1A4< 1C6 2D5< 5F10<
RRDEN4B          1A4< 1C6 2D5< 5B10<
RSOC            2E7> 3F1> 5F1> 1A7< 1E2
RSTB            1B2 2B5< 3D10< 5D10<
RXCN1           2C10< 3E10<
RXCN2           2C2< 5E10<
RXD1N           7D2> 1G10 2E10< 3G10<
RXD1P           7D2> 1G10 2E10< 3G10<
RXD2N           8D2> 1F10 2D10< 3B10<
RXD2P           8D2> 1F10 2D10< 3B10<
RXD3N           9D2> 1E10 2E2< 5G10<
RXD3P           9D2> 1E10 2E2< 5G10<
RXD4N           10D2> 1D10 2D2< 5B10<
RXD4P           10D2> 1D10 2D2< 5B10<
RXPRTY0         2E7> 1E2 3F1< 5F1<
RXPRTY1         2E7> 1H5 3F1< 5F1<
RX_VCC1          7E6
RX_VCC2          8E6
RX_VCC3          9E6
RX_VCC4          10E6
SD1             7D2> 1G10 2E10< 3G10<
SD2             8D2> 1F10 2D10< 3B10<
SD3             9D2> 1E10 2E2< 5G10<
SD4             10D2> 1D10 2D2< 5B10<
TAVD1           4E6> 3H4<
TAVD2           4D6> 3H4<
TAVD3           6E6> 5H4<
TAVD4           6D6> 5H4<
TAVS            3A4> 4C6<
TAVS2           5A4> 6C6<
TCA1            2D6> 3F1> 1B5< 1F2
TCA2            2D6> 3B1> 1A5< 1B5
TCA3            2D5> 5F1> 1A5< 1B5
TCA4            2D5> 5B1> 1A5< 1B6
TCLK1           1D7> 2C6> 3D1> 1B7<
TCLK2           1D7> 2C5> 5D1> 1A7<
TDAT <15..0>    1C7 1G3 1G4 1H4 2A5< 2A6< 3F10<
                  5F10<
TFCLK           1F2 2B5< 3E10< 5E10<
TSOC            1A7< 1F2 2B5< 3F10< 5F10<
TWREN1B          1C7< 1F2 2D6< 3F10<
TWREN2B          1B6 1B7< 2C6< 3B10<
TWREN3B          1B6 1B7< 2D5< 5F10<
TWREN4B          1B6 1B7< 2C5< 5B10<
TXD1N           2E10> 3G1> 1G10 7D2<
TXD1P           2E10> 3G1> 1G10 7E2<
TXD2N           2D10> 3B1> 1F10 8D2<
TXD2P           2D10> 3B1> 1F10 8E2<
TXD3N           2E2> 5G1> 1E10 9D2<
TXD3P           2E2> 5G1> 1F10 9E2<
TXD4N           2D2> 5B1> 1E10 10D2<
TXD4P           2D2> 5B1> 1E10 10E2<
TXPRTY0         1F2 2B5< 3F10< 5F10<
TXPRTY1         1H5 2B5< 3F10< 5F10<
TXVD_AC         4E6> 3H4<
TXVD_AC2        6E6> 5H4<
TXVS_AC         3A4> 4C6<
TXVS_AC2        5A4> 6C6<
```

```
TX_VCC1         7E2< 7F6
TX_VCC2         8E2< 8F6
TX_VCC3         9E2< 9F6
TX_VCC4         10E2< 10F6
VDD_AC          4F6> 3H4<
VDD_AC2         6F6> 5H4<
VDD_DC          4F3> 3H4<
VDD_DC2         6F3> 5H4<
VSS_AC          3A4> 4C8<
VSS_AC2         5A4> 6C8<
VSS_DC          3A4> 4C8<
VSS_DC2         5A4> 6C8<
WRB             1B2 2B5< 3D10< 5D10<
```

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

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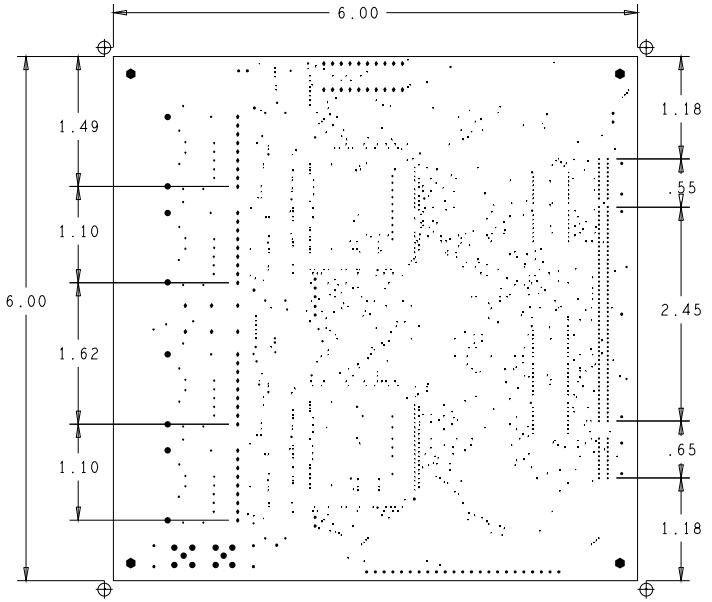
ENGINEER: ?E	PAGE: ?P OF ?T

APPENDIX I: PCB ARTWORK

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



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ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
MECH DRAWING
GND_TA PLANE
GND_RA PLANE
SOLDER PASTE TOP
SOLDER PASTE BOTTOM

	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	GND_TA	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	2.88 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	2.88 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
	COPPER	CONDUCTOR	GND_RA	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	10.0 mil	4.2
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	1.44 mil	-------

Note: 50 ohm controlled impedance traces with trace width of 17 mil are on Top and Bottom layers.

Notes:

1. Copper thickness is 2 oz on VCC_PLANE & GND_PLANE and 1 oz on other layers
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recognized by UL to the 94V-0 rating.

NCDRILL_LEGEND

/ FIGURE / HOLESIZE / QTY /

▲	13.000-P	648
■	22.000-P	140
●	25.000-P	115
■	36.000-P	49
◆	42.000-P	62
●	79.000-P	16
⬢	125.000-P	4

UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN S. SIU	96	07	28
TOLERANCES ON:	CHECKED			
2 PL DECIMALS ±	ENGRG			
3 PL DECIMALS ±	ISSUED			
ANGLES ±				
FRACTIONS ±				

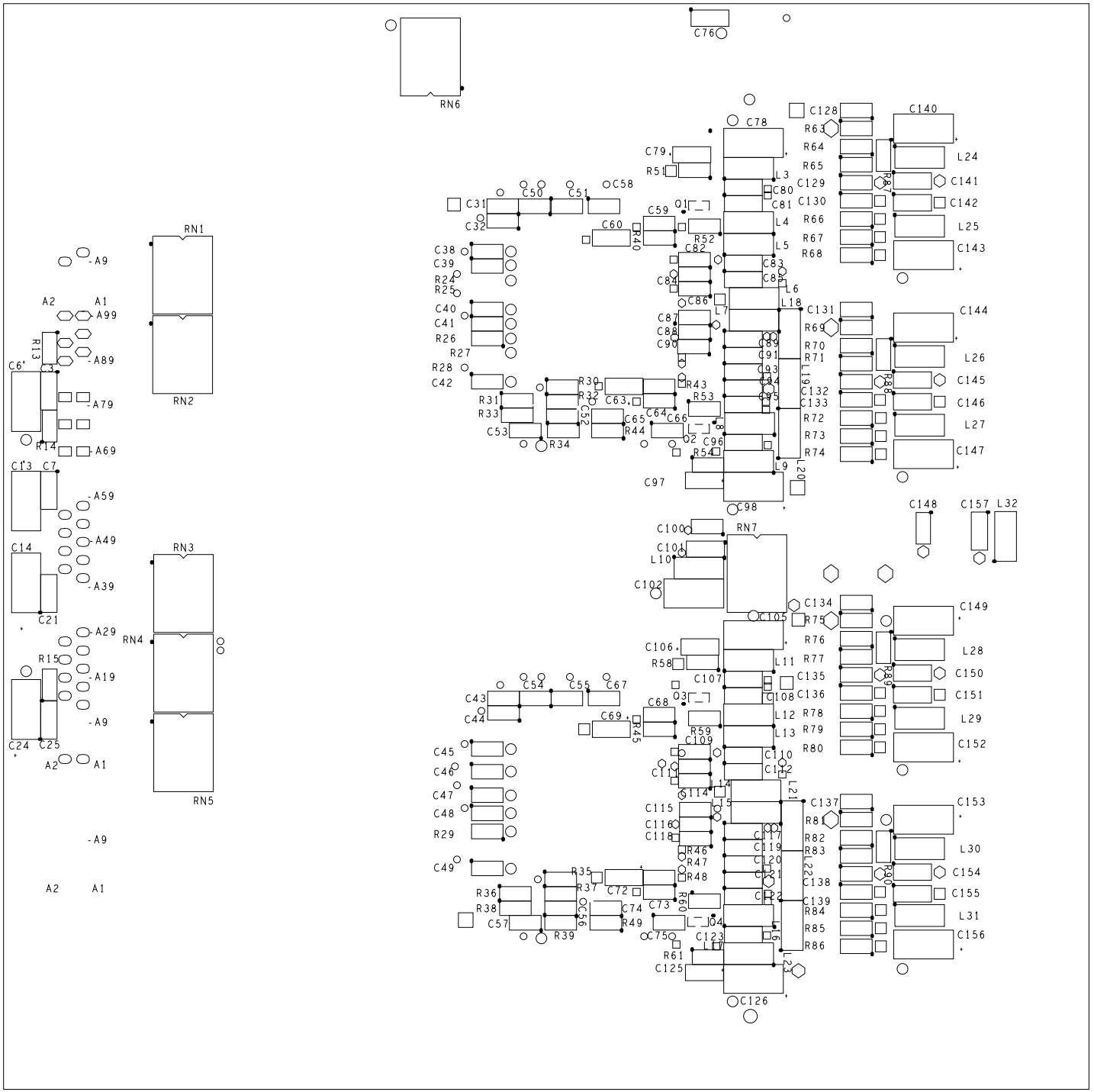
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		

SCALE	NTS	SHEET OF


RN1
RN2
RN3
RN4
RN5
RN6
RN7
A9
A99
A89
A79
A69
A59
A49
A39
A29
A19
A2
A1
C1
C3
C6
C7
C13
C14
C21
C24
C25
R13
R14
R15
C76
C78
C79
C80
C81
C82
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C84
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C156
C157
R24
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L30
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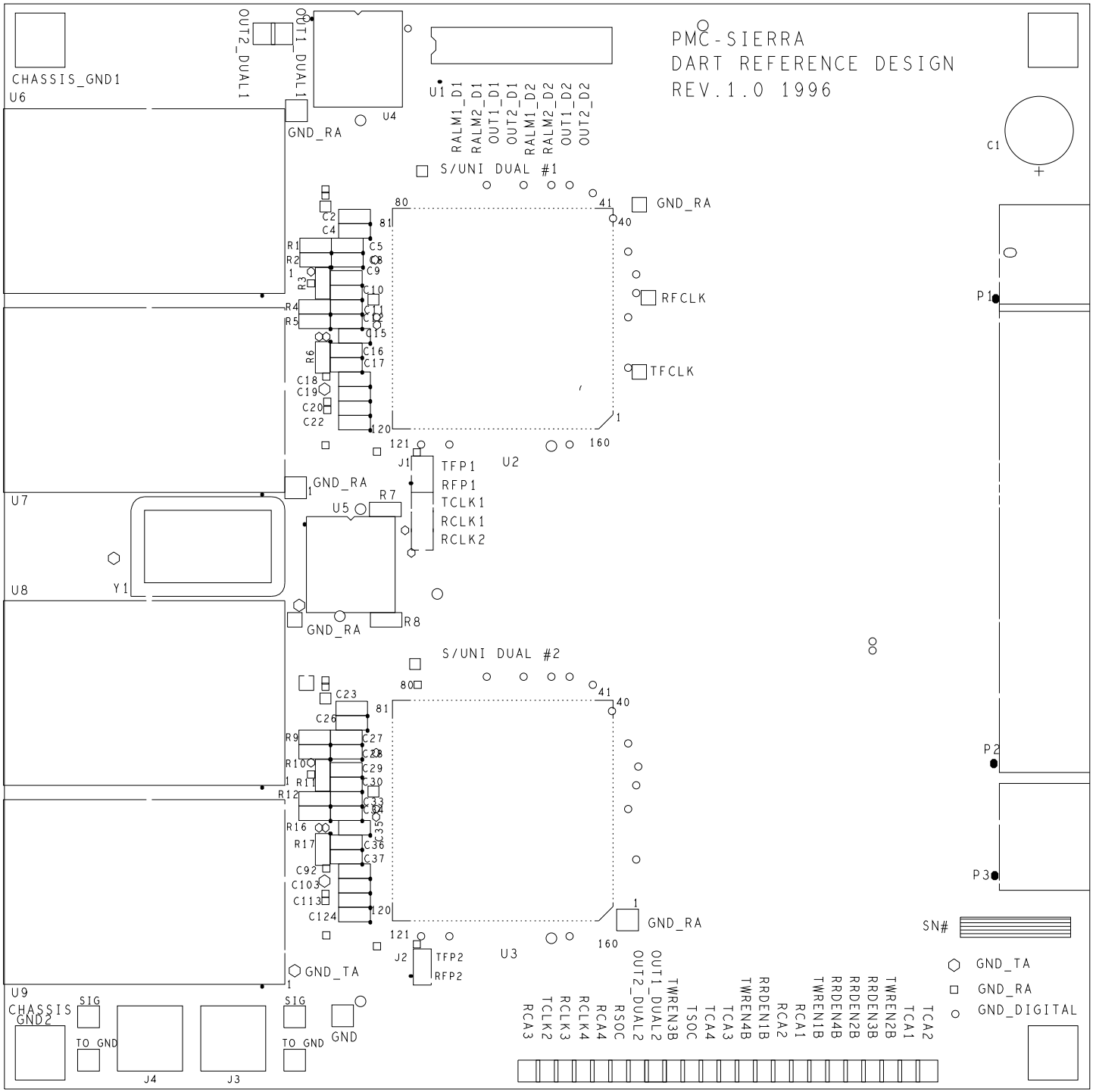
L32
Q1
Q2
Q3
Q4

SILK SCREEN TOP



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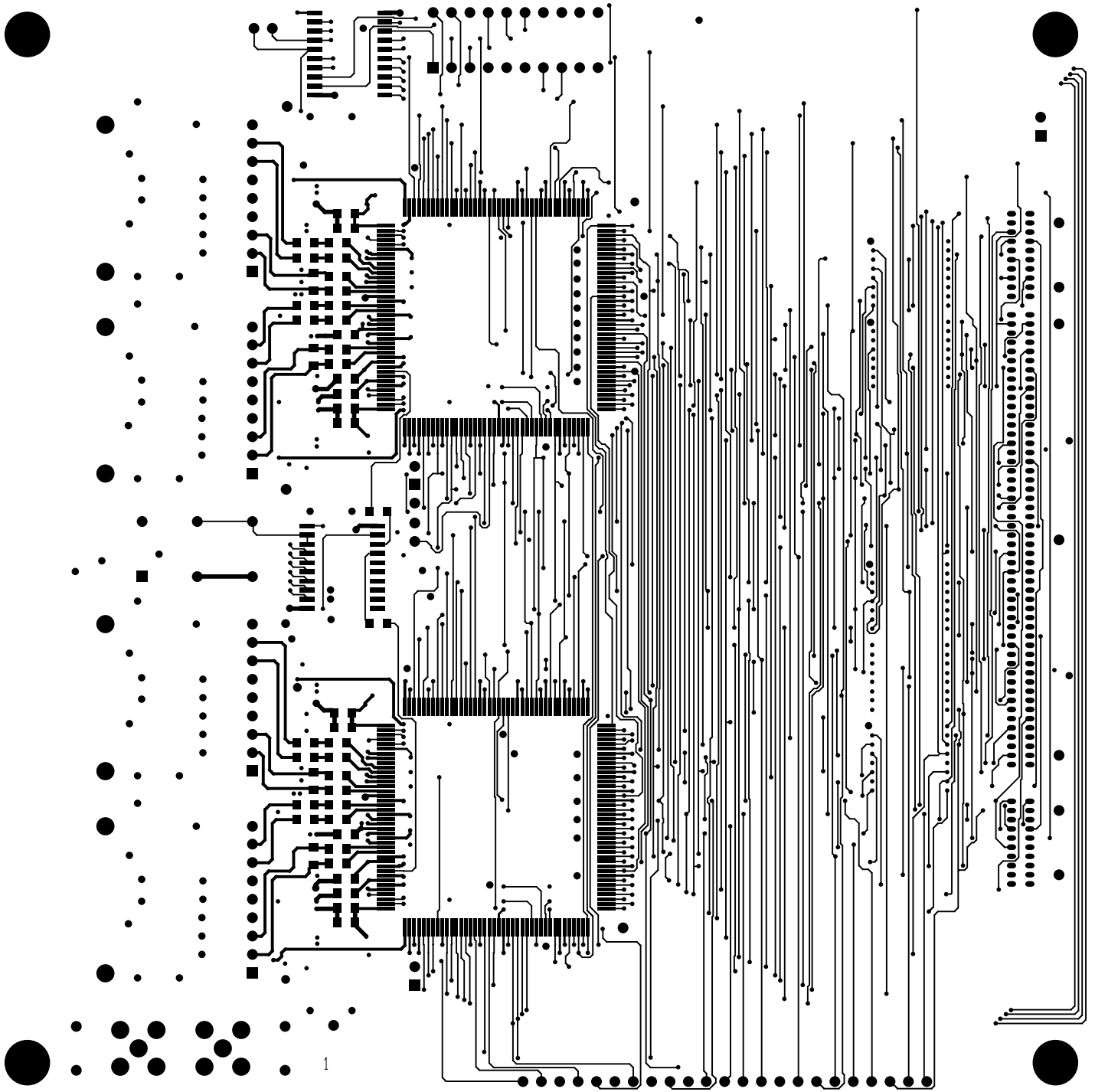
TOP LAYER



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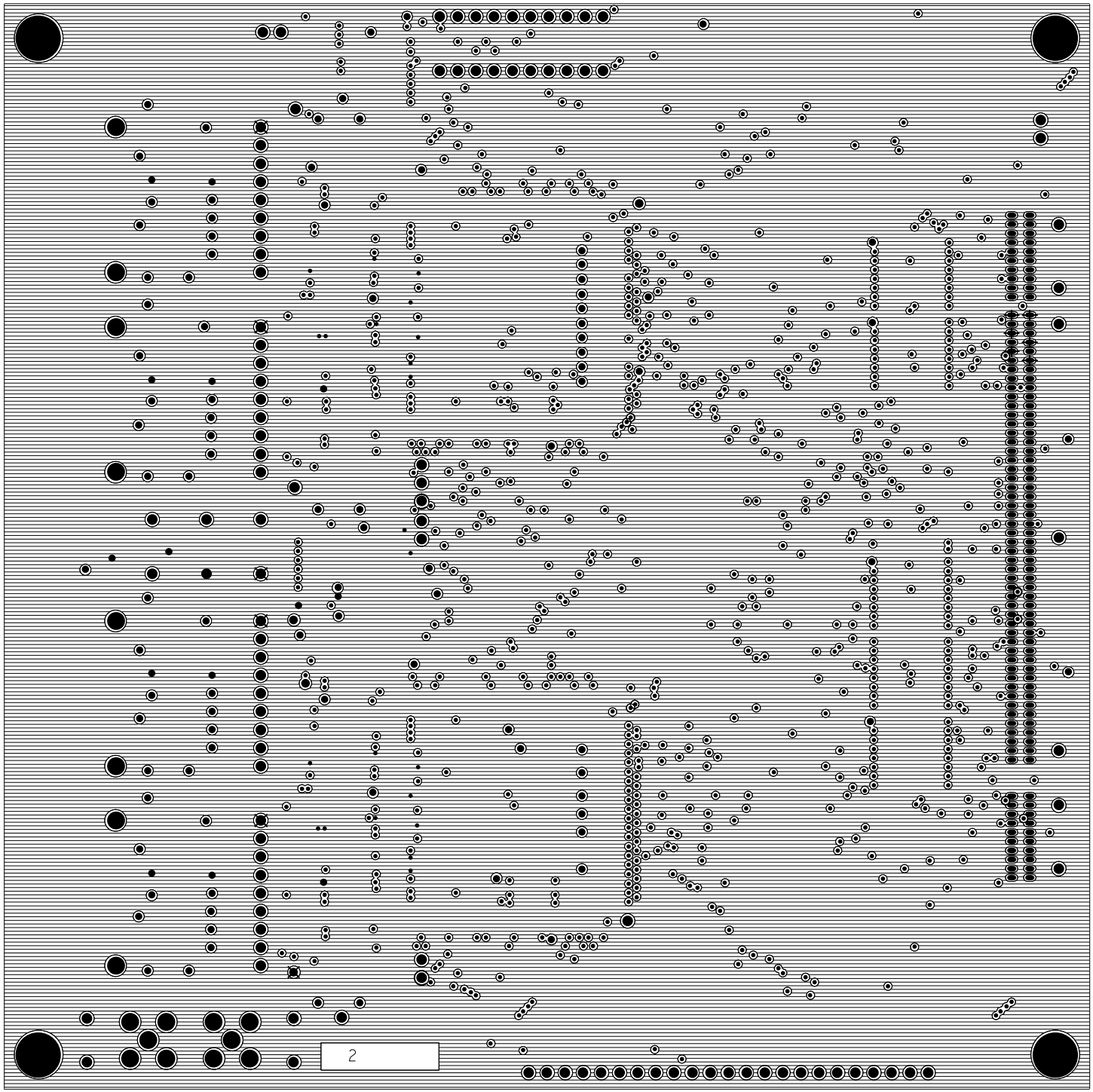
GND_TA PLANE



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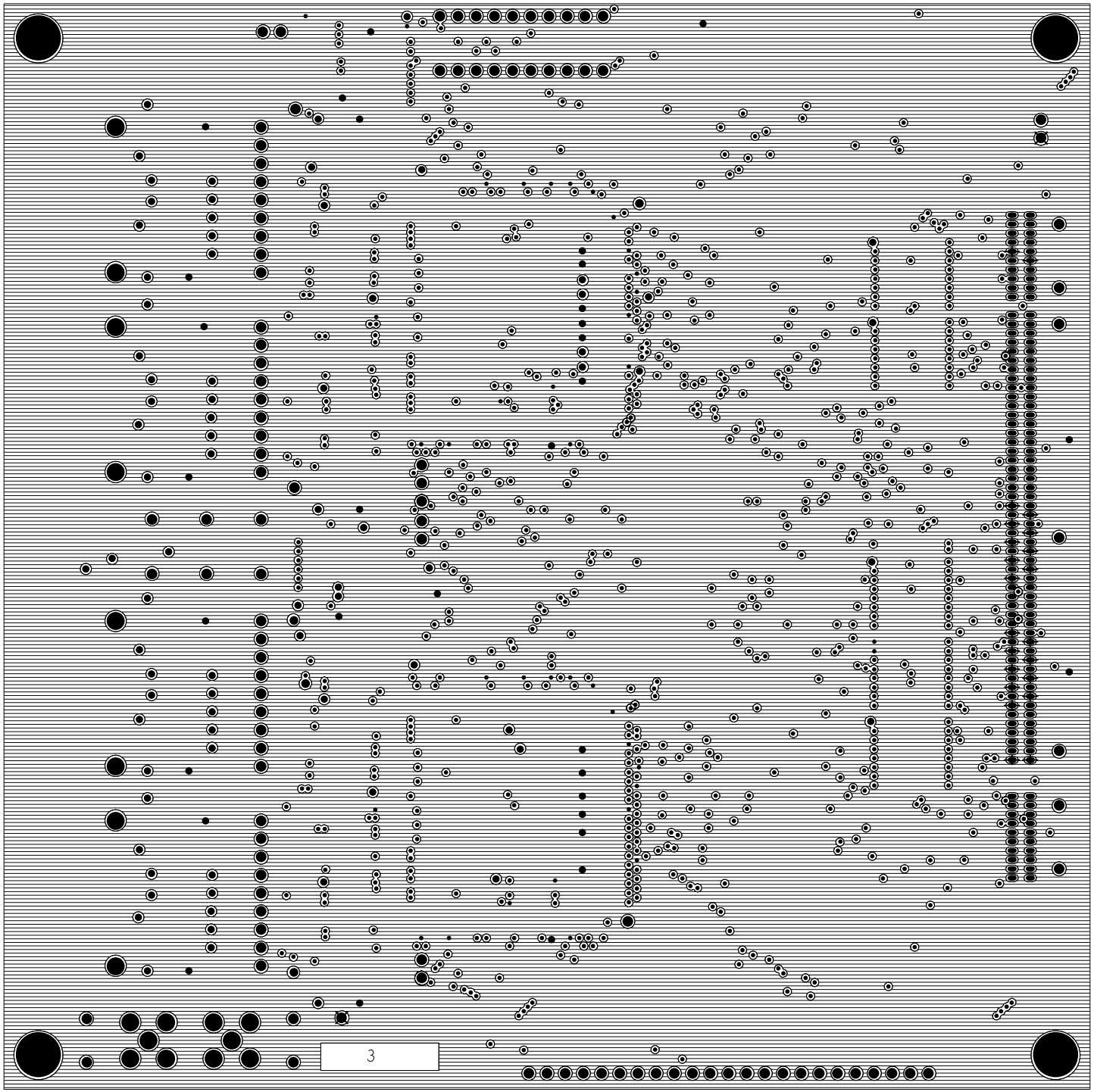
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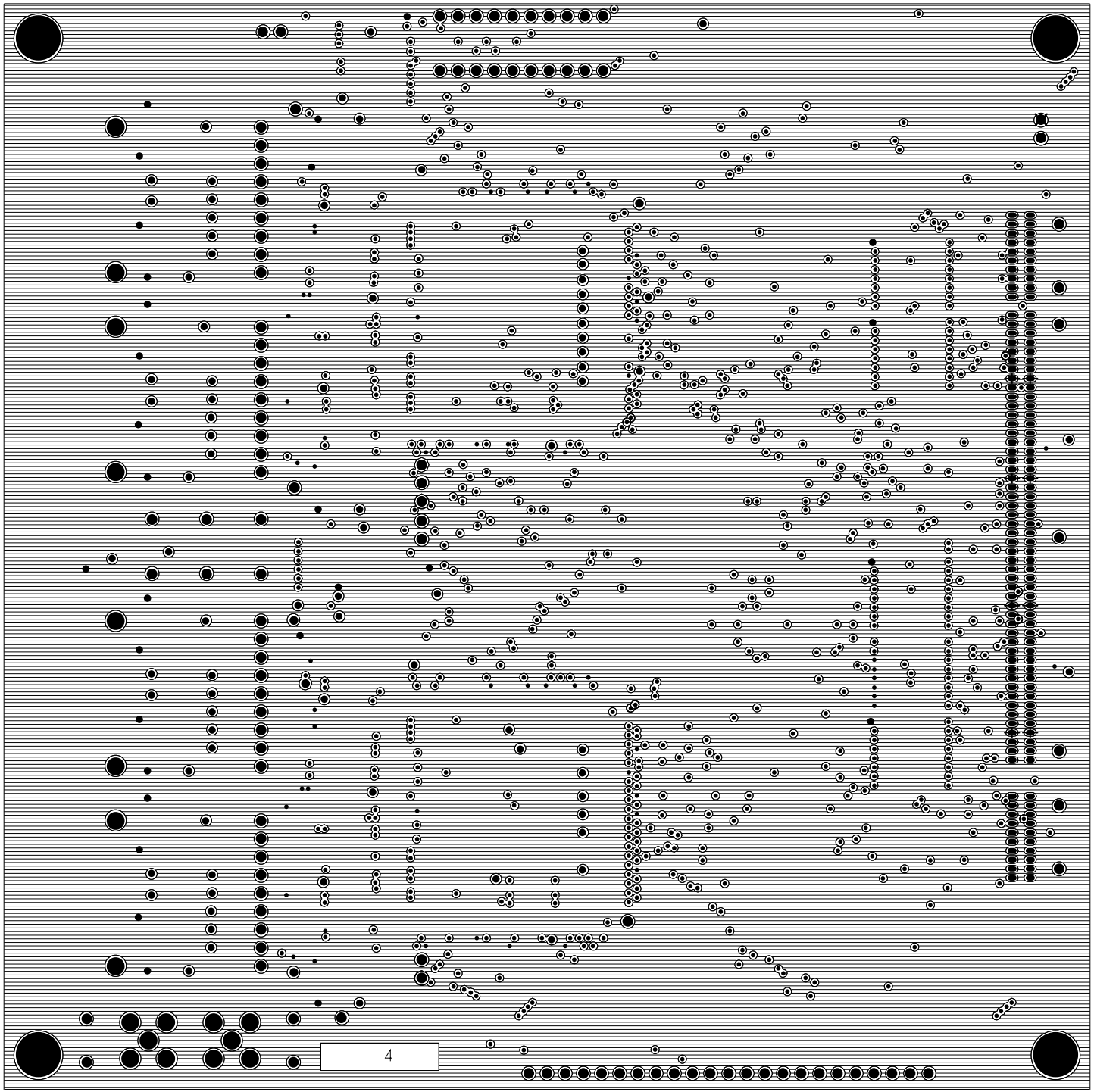
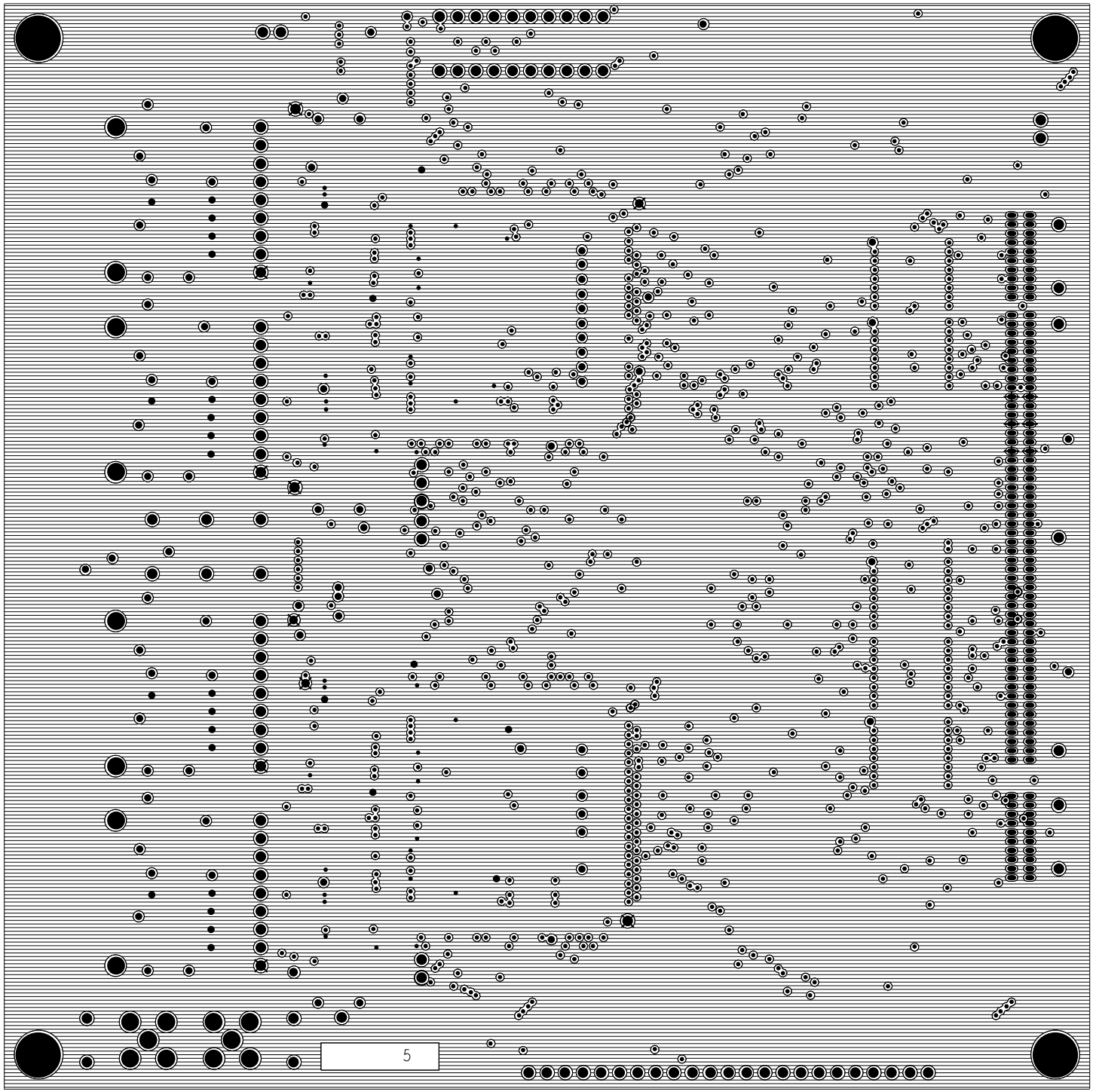
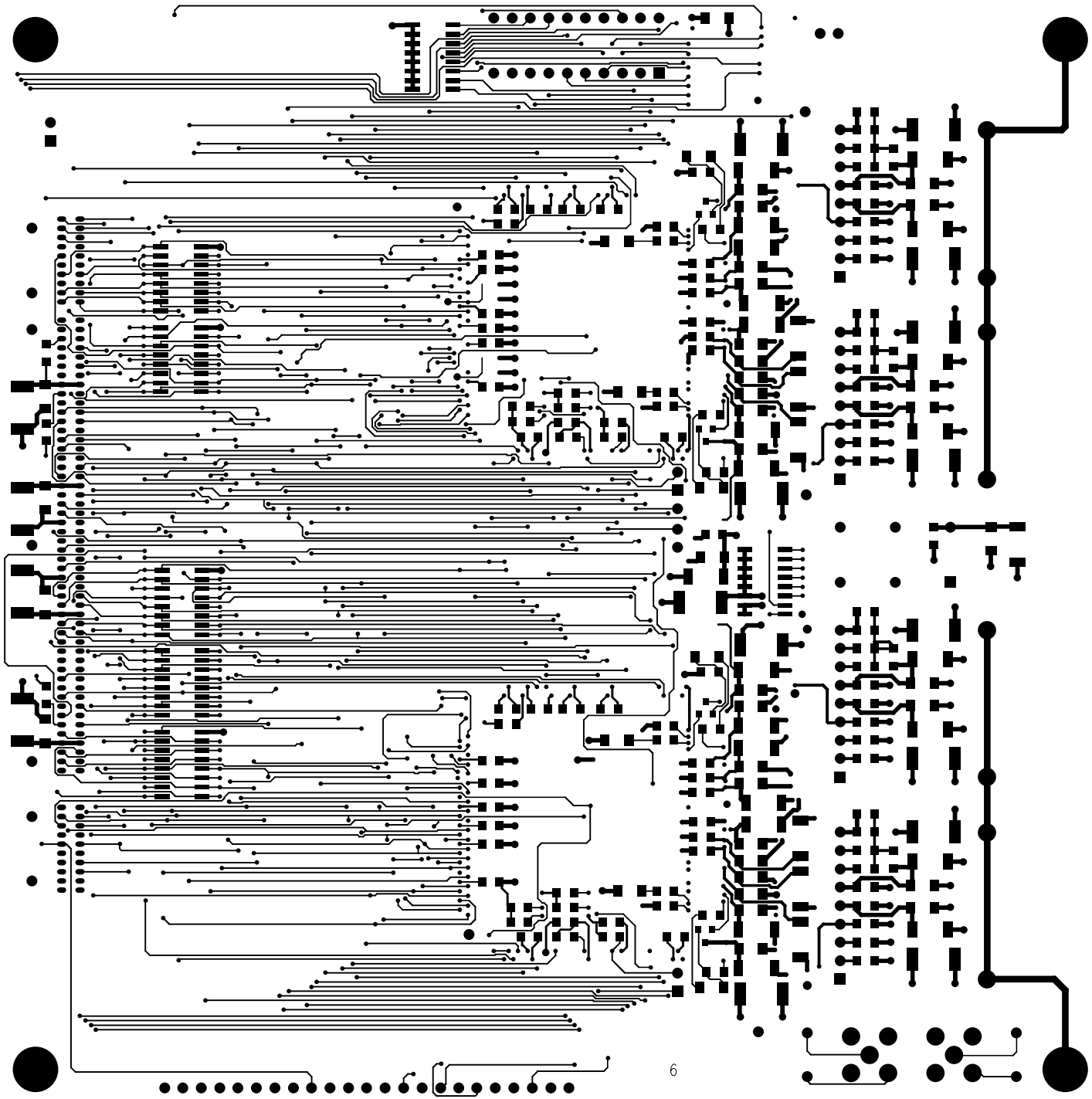
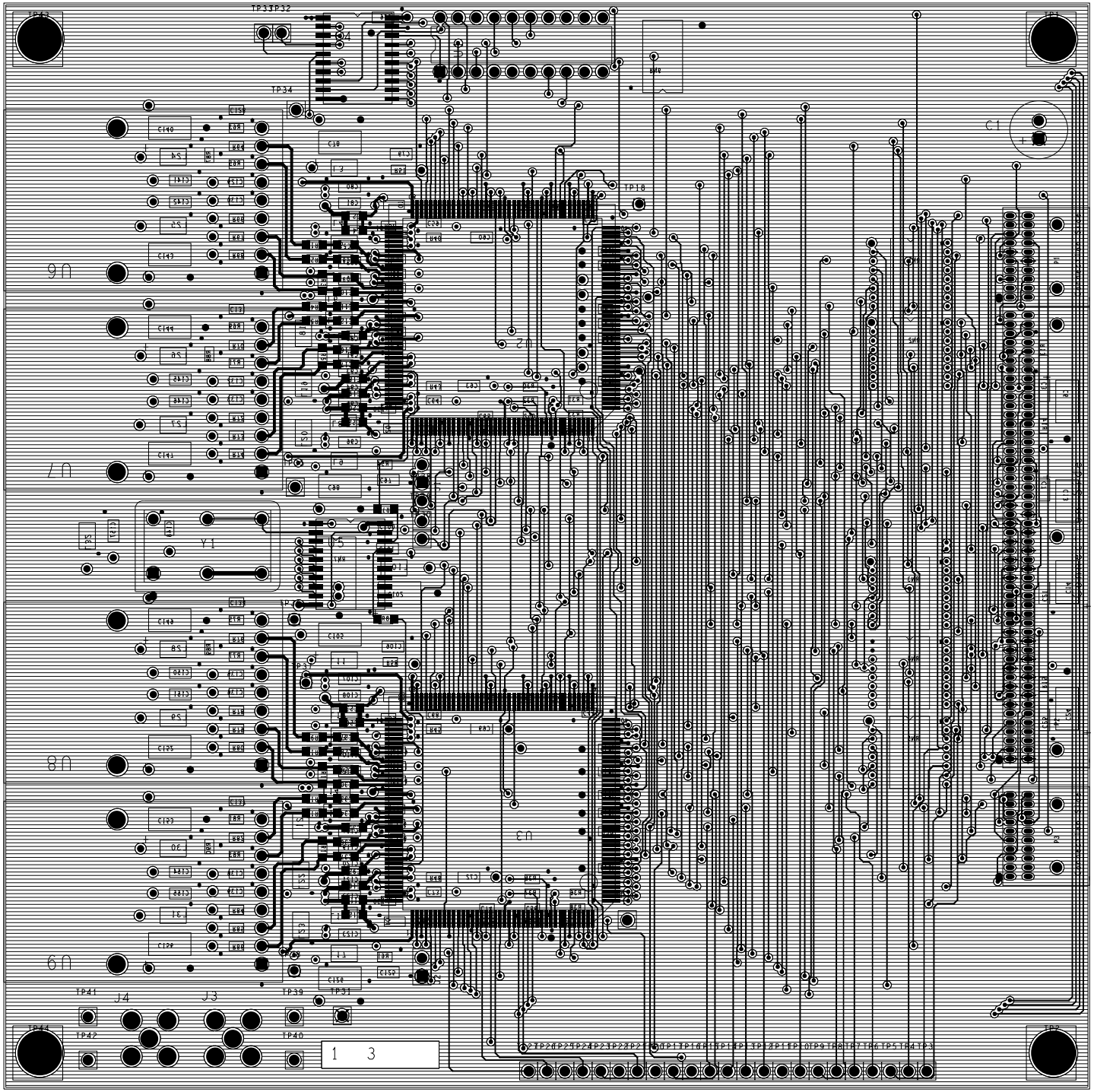

4

GND_RA PLANE





TOP LAYER GND PLANE



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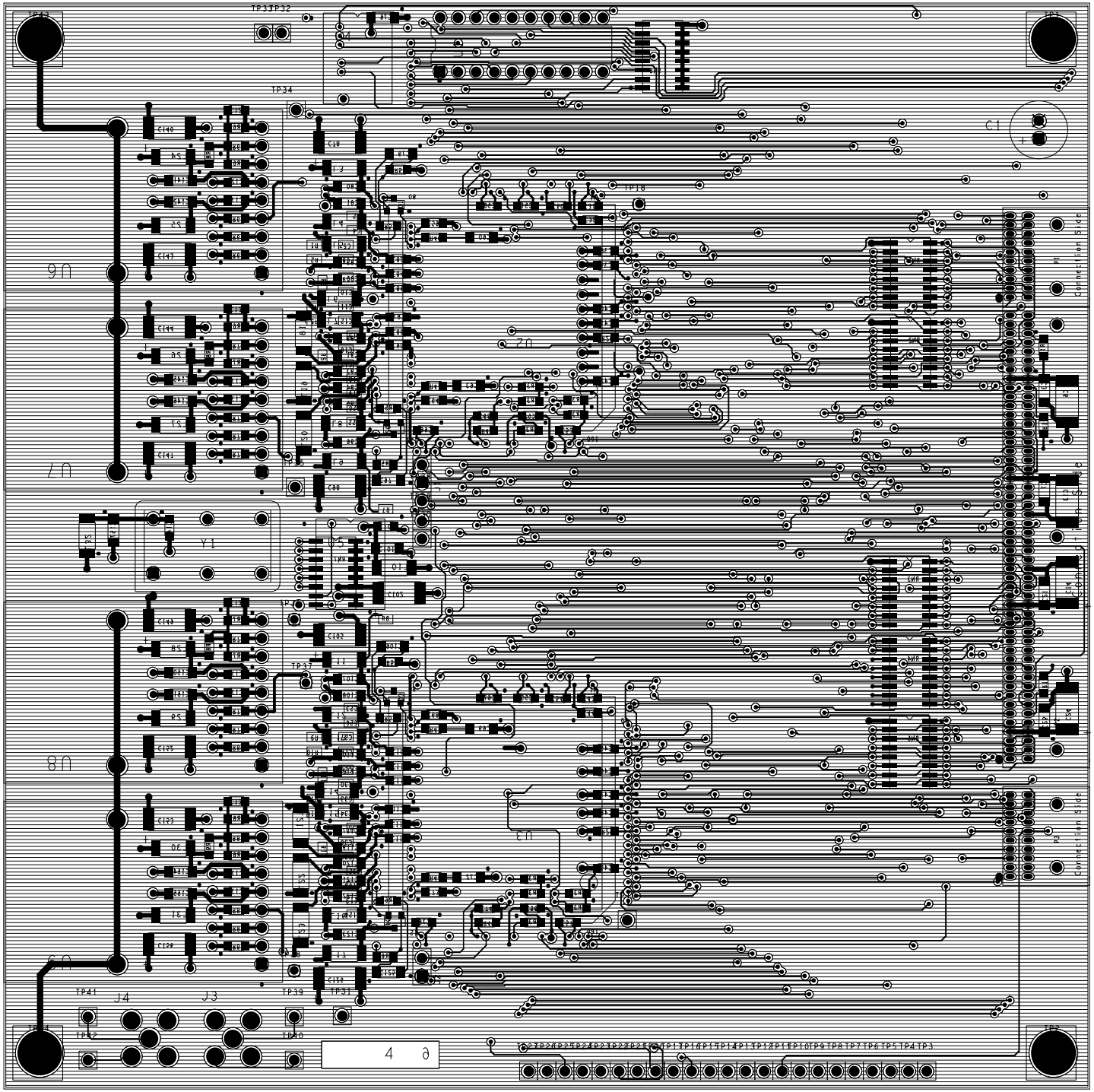
J4
J3
Y1
U2
U3
U5
U6
U7
U8
Connection Side
Connection Side

APPENDIX J: REFERENCES

- American National Standards for Telecommunications, ANSI T1.105.03 - 1994
- Bell Communications Research, Bellcore GR-253-CORE, Issue 2, Dec. 2, 1995
- International Telecommunications Union, ITU-T Recommendation G.958 - "Digital Line Systems Based on the Synchronous Digital Hierarchy for use on Optical Fibre Cables"
- PMC-Sierra, PMC5348 databook, Issue 5, January 1997, PMC-950919, "S/UNI-155-DUAL, Saturn User Network Interface 155.52 & 51.84 Mbit/s"
- PMC-Sierra, S/UNI-LITE (PM5347) and the Optical Reference Design (SORD board), PM5946, PMC-950112
- Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", Second Edition, John Wiley & Sons.
- Montrose, Mark I., "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press, 1995.
- Graham, Martin and Johnson, Howard W., "High-Speed Digital Design: A Handbook of Black Magic", PRT Prentice-Hall Inc, 1993.
- Tokin catalog EC-110E and User's manual EC-111E, 1996, USA 1-408-432-8020

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