PM3350
ELAN 8x10

24-Port Ethernet Switch Reference Design

PROPRIETARY AND CONFIDENTIAL

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[1] Refer to the System Configuration to determine the number of MAC addresses supported by the firmware programmed into the EPROM. The system can be configured to support up to 32k MAC addresses. See the PM3350 datasheet.

REFERENCES

- PMC-Sierra PM3350 Datasheet, Issue 1 (1997)
- ISO/IEEE 8802.3 CSMA/CD Local Area Networking Specification (1993)
- Level One Communications, Data Book (1996), "Ethernet PHY Products"

OVERVIEW

This document describes an implementation of a 24-port Ethernet Switch design based on PMC-Sierra's PM3350 Elan 8x10. This design, called the 24-port Elan 8x10 Reference Design, embodies PMC-Sierra's guidelines and suggestions for designing an Ethernet switch.

This reference design is intended to operate in two modes: 1) Stand-alone mode, where this board provides the complete functionality of a 24-port Ethernet Switch, and 2) This board can interface with other boards, such as the 2-port Fast Ethernet Switch reference design, through the PCI expansion backplane.

In addition to the three PM3350 Elan 8x10 devices (each supporting 8 ports), the PM3350 Reference Design incorporates on-board DRAM, EPROM, oscillators, 10BaseT PHY chips (Level One LXT944), 10BaseT magnetics, RJ-45 jacks, status LEDs and other miscellaneous devices to complete the switch design. A complete list of components can be found in the Bill of Materials.

The Functional Description gives a list of key features of this reference design. The Implementation Description provides a detailed description of all the major components which are found in the schematics (included as Attachment I). The Interface Description lists the RJ45 and the PCI expansion bus pin definitions. For readers who are interested more additional in-depth considerations for this reference design, the Design Consideration section provides many tips and guidelines on high-speed circuit board design and component selection. Finally, a Bill of Materials and the schematics are included at the end.

FUNCTIONAL DESCRIPTION

The block diagram of this reference design is shown in Figure 1. The following is a summary of the features offered in this switch.

Feature List

- Complete 24-port 10BASE-T non-blocking switching
- Operates i) as a completely stand-alone switch, or ii) in conjunction with other switch cards using the PCI expansion bus, such as the 2-port Fast Ethernet Switch reference design, to create larger switch systems
- Supports a peak system bandwidth of 1 Gbit per sec (600 Mbit/s sustained) using the PCI expansion bus
- Filters and switches packets using a locally-maintained database
- Performs packet switching, IEEE 802.1d compliant transparent bridging, or both
- Store-and-forward mode with full CRC check.

Fig. 1 Reference Design System Block Diagram

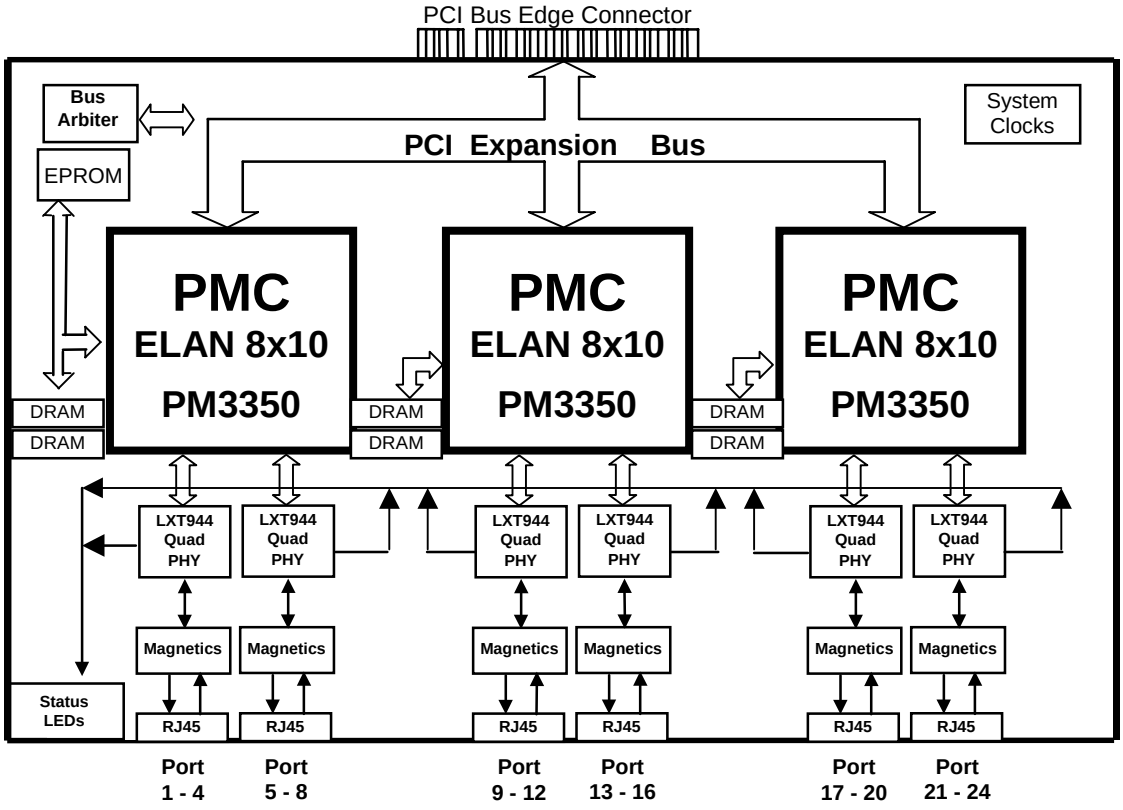
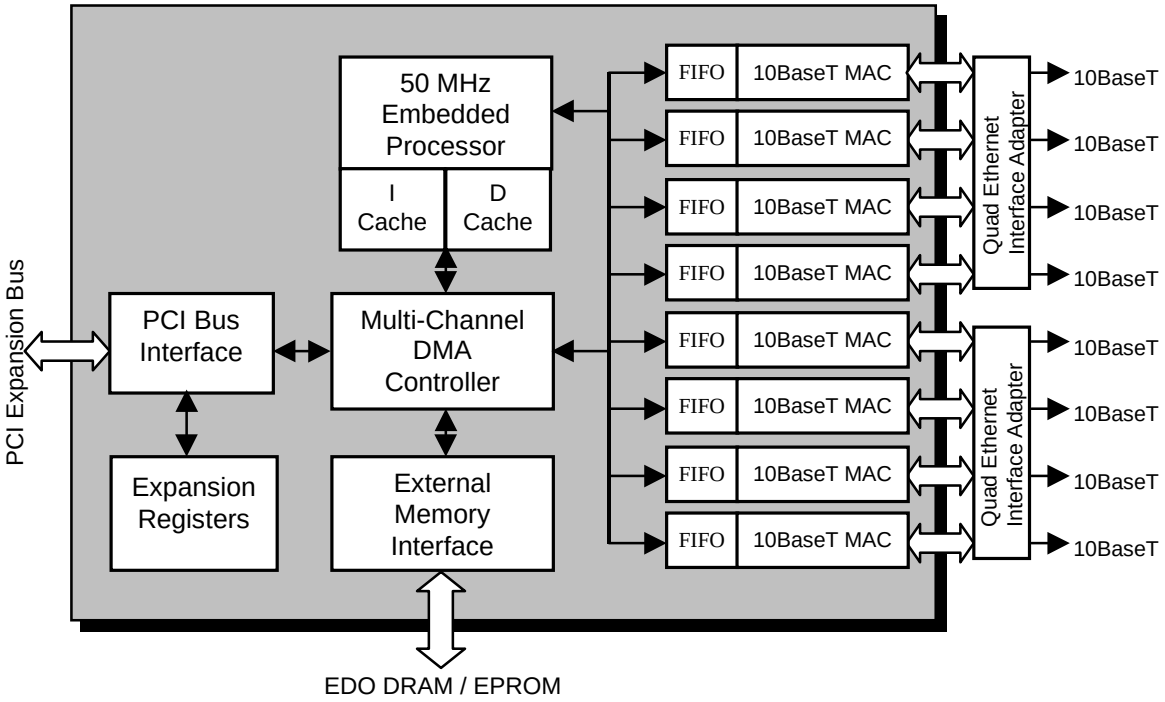


Fig. 2 Block Diagram



PM3350 Elan 8x10

The PM3350 is a highly integrated stand-alone single-chip switching device for Ethernet/IEEE 802.3 switching and bridging applications. The device supports all processing required for switching Ethernet/IEEE 802.3 packets between eight independent half-duplex 10 Mbit/s ports. In addition, a switch built around the Elan 8x10 can be expanded by connecting up to 7 additional devices to the on-chip 1 Gbit/s expansion port, a system clock oscillator for the bus and a simple PAL for bus arbitration. Switch configuration and management can be performed either remotely (in-band), via the on-chip SNMP MIB, agent and integrated TCP/UDP/IP stack.

The Elan 8x10 chip contains all the required elements of a high-performance Ethernet switch: MAC-layer interfaces, buffer FIFOs, a high-speed DMA engine for fast packet transfers, a local memory interface for up to 16 MB of external buffer memory, a PCI compatible bus master and slave unit for modular expansion, and a powerful switch processing unit that implements the switching and bridging functions. The only additional components required to create a complete 8-port switch are two quad Ethernet Medium Access Unit (MAU) devices, line transformers and a bank of external memory.

The Elan 8x10 device is implemented in high-density CMOS technology for low cost and high performance. It is available in a 256 ball grid array (BGA) package, and is ideally suited for compact, low-cost desktop, workgroup and departmental Ethernet switching applications.

IMPLEMENTATION DESCRIPTION

The schematic diagram of the 24-Port Elan 8x10 Reference Design is contained in Attachment I.

Page 1 of the schematics shows the main functional blocks. The core functionality consists of three identical[2] "ports" or "slices" of 10M Ethernet circuitry, each using a PM3350, DRAM memory, and physical interface components (PHY, transceiver, magnetics, etc.) Additionally, the board contains an EPROM for code download, PCI Arbiter, connectors, timing sources and miscellaneous "glue" circuitry.

Functional blocks are described below. All of the major components are described for one slice of the 10M Ethernet circuitry. The same description apply to all two slices:

- Slice (Port) 1- 8: Sheets 3 - 6
- Slice (Port) 9 - 16: Sheets 7 - 10
- Slice (Port) 17 - 24: Sheets 11 - 14

The components ID's are listed in parenthesis after each component name.

[2]Identical except for the EPROM which only PM3350 #0 is connected to.

10M Ethernet Switch Circuitry

PM3350

(U23, U24, U28) [Sheet 3,7,11]

Three PM3350 8-port Ethernet switch chips form the core of the 24-port Reference Design.

EEPROM

(U15) [Sheet 4]

One 256K by 8-bit, 150ns[3] EPROM is included. A smaller EPROM (128K x 8-bit) can be used if an unmanaged version of the firmware is used. The board is designed to accommodate a larger EPROM (512K x 8-bit) should it be needed for more software features.

The EPROM is used for the PM3350 boot code, switching code, SNMP code (when available), and any special function code (e.g., custom LED display, aging, backpressure, VLAN, etc.). Code is downloaded into the first PM3350 device (U23), which in turn will download the code to the other PM3350 devices in a daisy-chain fashion through the PCI bus.

This device has a socket for ease of replacement.

DRAM

(U14/U17&U13/U16, U21/U22, U27/U29) [Sheet 4,8,12]

Two, 256K by 16-bit, 60ns EDO DRAM chips (one MByte total) are used to provide RAM storage for each PM3350. The DRAM is used for MAC address tables, packet buffer storage, and for data structures required during operation.

An additional bank of memory is installed in locations U13 and U16 to support managed versions of the switch.

Physical Layer Interfaces

(U4&U2, U8&U6, U12&U10) [Sheet 5&6, 9&10, 13&14]

[3] 150ns is the closest to the 180ns specified in the ED datasheet.

Six Level One LXT944 devices are used to provide the physical interface for 10BASE-T Ethernet systems. Please refer to a current issue of the Level One Communications Databook for information describing this quad Ethernet physical layer interface device.

Line Interface Circuitry

(Transformers: U3&U1, U7&U5, U11&U9) [Sheet 5&6, 9&10, 13&14]

The line interface circuitry consists of the transformers (four quad magnetics/filter components), and passive networks necessary to interface the LXT944 device to the RJ-45 connectors, and onto UTP5 cables carrying Ethernet 10 BaseT signals. This circuitry reflects recommendations in the Level One data book.

Common Components

Timing Distribution

[Sheet 2]

(Y2) - The high-speed timing to the PM3350 devices is sourced from a 50MHz crystal oscillator.

(Y1) - The high-speed timing to the PCI bus is sourced from a 40MHz crystal oscillator.

PCI Bus Connector

(P1) [Sheet 2]

There is one edge connector on the board that is connected to the onboard PCI bus expansion port backplane. It is used to interface this board to other reference designs such as the 2-port Fast Ethernet Switch using PM3351. When this reference design is operating in the stand-alone mode, this edge connector is not used. Please refer to the Interface Description section for the pin definitions.

Note that this PCI connection is not compliant to the PCI specification, v2.1. This is because of 1) the pin redefinition required for PCI arbitration (see the PCI Arbiter description), and 2) the fact that there are more than one "PCI device load" on a single board attached to the bus.

PCI Arbiter

(U18) [Sheet 2]

The 24-port Reference Design board has one Arbiter CPLD that implements a simple arbiter required by the PCI bus expansion port.

The PCI Arbiter implements a simple round-robin algorithm to control bus access by the PM3350 devices onto the PCI expansion bus. This arbiter is implemented in a 44-PLCC CPLD (e.g. Xilinx XC9572-7-PC44). Please contact PMC-Sierra, Ethernet Division, for information on the implementation of the arbiter.

This arbiter assumes sole control on the PCI expansion bus when this reference design board is interfaced to the 2-port Fast Ethernet Switch reference design. Because of this, bus request/grant signals of the PM3351 devices have to be routed through the PCI bus backplane onto this reference design, which is accomplished by re-defining some of the unused pins on the PCI connector.

This device has a socket for ease of replacement. When two ELAN Reference Design boards are interfaced the 2-port Fast Ethernet Switch reference design board should have its U43 removed.

Reset Debounce

(U31) [Sheet 3]

The Dallas DS1233 "EconoReset" device is used to provide power-up reset and the reset debounce function. It monitors the status of the power supply (Vcc) and will automatically assert the reset when a threshold is crossed. Reset is maintained active for a minimum time of 350ms.

Resistors and Jumpers

Three configurations of resistors and jumpers are provided below.

Master 24x10 stand alone
Open JP3
Open JP6
Open JP9
Open JP12
Install JP8
Open JP1
Install JP2
Install JP5

Install JP10

Slave 24x10 with master 24x10

Install Jumper JP3-1 to JP3-2

Install Jumper JP3-3 to JP3-4

Install Jumper JP3-5 to JP3-6

Install Jumper JP6-1 to JP6-2

Install Jumper JP6-3 to JP6-4

Install Jumper JP6-5 to JP6-6

Install Jumper JP9

Install JP12

Install JP8

Install JP1

Install JP2

Install JP5

Install JP10

Remove resistor R83 and replace at R326

Remove resistor R92 and replace at R333

Remove resistor R107 and replace at R378

Remove resistor R272 at top and replace R272 at bottom

Remove R307 at top and replace R307 at bottom

Remove R317 at bottom and replace R317 at top

Remove R314 at bottom and replace R314 at top

Remove R370 at top and replace R370 at bottom

Remove R366 at bottom and replace R366 at top

Remove R99 at bottom and replace R99 at top

Remove R98 at top and replace R98 at bottom

Master 24x100 with slave 2x100 or slave 24x10
Open JP3
Open JP6
Install JP9
Install JP12
Install JP8
Open JP1
Install JP2
Install JP5
Install JP10

(JP3) [Sheet 2]: This header designates the PCI signals for REQ that will come from the three PMC3350 devices in route to the arbiter (U1). All jumper positions are normally open and can only be used after the arbiter has been removed. In a 48-port switch Reference Design (or with the 2x100 Reference Design) this secondary board must have jumpers across positions 1-2, 3-4, and 5-6.

(JP6) [Sheet 2]: This header designates the PCI signals for GNT that will go to the three PMC3350 devices from the arbiter (U1). All jumper positions are normally open and can only be used after the arbiter has been removed. In a 48-port switch reference design (or with the 2x100 Reference Design) this secondary board must have jumpers across positions 1-2, 3-4, and 5-6

(JP9) [Sheet 2]: This header with the use of a jumper determines the source of the PCI clock. The clock may be sourced from the on-board oscillator (U2) or it may be provided from the PCI bus edge connector. In normal operation it is provided by the on-board clock with the jumper installed

(JP4/7/11) [Sheet 3]: These headers are reserved for future use and should not be used.

(JP8) [Sheet 3]: This header with the use of a jumper determines the source of the system Reset signal. The Reset is sourced from the on-board switch (S1) only or it may be provided from the PM3350. In normal operation it is provided by the PM3350 with the jumper installed.

(JP12) [Sheet 2]: This header with the use of a jumper determines that the reset signal goes out to the PCI bus when installed.

(S1) [Sheet 2]: This switch is a master reset for the Reference Design board.

Other Board Components

RJ-45 Connectors

(J1, J2, J3) [Sheet 6,10,14]

There are 24 RJ-45 connectors (3 blocks of eight) for connection of Ethernet 10 BaseT segments to the switch. They are configured as a "hub" connection.

LEDs

(D3, D2, D5, D4, D7, D6)

[Sheet 5,6,9,10,13,14]

There is 1 LED per port, arranged vertically in groups of four. Each LED is a link light corresponding to a port.

Power Supply Connections

This Reference Design board requires a 5.0V +/- 5% power supply capable of providing a minimum of 4.0 Amps. The regulator U30 provides 3.3V to an island within the 5V power plane.

Configuration Resistors

Each "slice" of 10M port circuitry uses a bank of resistors to configure the PM3350 after reset. Resistors, not dip switches, are used to lower the cost. The resistor functions and default values are given below.

Function	PM3350 0	Value	PM3350 1	Value	PM3350 2	Value
PCIRUN	R264	1	R304	1	R361	1
RISCRUN	JP1	open	R305	0	R364	0
Reserved	R270	0	R306	0	R368	0
IMDIS	R273	0	R308	0	R369	0
PCI3V	R274	0	R309	0	R371	0
Reserved	JP2	Installed	JP5	Installed	JP10	Installed
CHIPID [3]	R260	0	R307	0	R370	1
CHIPID [2]	R259	1	R317	1	R366	0
CHIPID [1]	R60	1	R319	1	R99	0
CHIPID [0]	R272	0	R314	1	R98	0
RTCDIV [5]	R64	1	R312	1	R346	1
RTCDIV [4]	R239	1	R311	1	R344	1
RTCDIV [3]	R232	0	R310	0	R96	0
RTCDIV [2]	R63	0	R73	0	R97	0
RTCDIV [1]	R236	0	R282	0	R345	0
RTCDIV [0]	R62	1	R285	1	R95	1
MXSEL[1]	R231	0	R276	0	R381	0
MXSEL[0]	R235	1	R279	1	R380	1
MSLO	R241	0	R277	0	R382	0
MDCAS	R234	1	R280	1	R383	1
MTYPE3 [2]	R237	1	R74	1	R384	1
MTYPE3 [1]	R243	0	R313	1	R387	1
MTYPE3 [0]	R65	1	R75	0	R385	0
MTYPE2 [2]	R240	1	R283	1	R386	1
MTYPE2 [1]	R261	0	R288	0	R367	0
MTYPE2 [0]	R263	1	R286	1	R112	1
MTYPE1 [2]	R266	1	R289	1	R365	1
MTYPE1 [1]	R269	1	R278	0	R111	0
MTYPE1 [0]	R271	0	R281	1	R363	1
MTYPE0 [2]	R268	1	R284	1	R110	1
MTYPE0 [1]	R265	1	R287	1	R360	1
MTYPE0 [0]	R262	0	R290	0	R109	0

Notes

1) The top row (PCIRUN) correspond to D31, the MSB of the memory data bus

2) RISCRUN of Bank 0 is set to 1, since the EPROM is connected to the ED in this bank.

Note: Looking at the top side (component side) of the board, if the board is placed such that the PM3350 devices is at the bottom and with the RJ45 connectors on the top, then the resistor placement is defined as:

Top = Pull-up (High)

Bottom = Pull-down (Low)

Configuration Resistor Functions

The Configuration Resistors provide the default pull-up/down values on the memory databus, which are read by the PM3350 after reset. 4.7K resistors are used for them. The CHIPID have a custom 3-pin 0805 footprint (one pin for pull-up, one for the signal, one for the pull-down).

WARNING: Modifying these resistors may prevent the reference design board from working. Please refer to the PM3350 datasheet for detailed description of these functions.

PCIRUN Configuration

PCIRUN: This line determines whether the PM3350 runs in master or slave mode.

RISCRUN Configuration

RISCRUN: This line controls whether the chip runs or halts after reset.

IMDIS Configuration

IMDIS: Internal memory disable, which controls the bootcode fetch location. High = boot strapped from the external local memory, Low = boot strapped from on-chip ROM.

PCI3V Configuration

PCI3V: This selects the PCI interface signaling environment. High = 3.3V, Low = 5V.

CHIPID Configuration

CHIPID: These 4-bits determine the chip's PCI address. This is used to set the second nibble (bits 24 - 27) of the PM3350's address space on the PCI bus. The top nibble (bits 28 - 31) are initialized to zero (0), but can be set by software control if required.

The CHIPID's of the 4 banks are set to 6, 7, 8 by default respectively, so as to distinguish them from the CHIPID's of the 4 FED devices on the 4-port Fast Ethernet Switch reference design. 0 and 1 are reserved for other PCI devices that may be connected to the PCI expansion bus.

RTCDIV Configuration

RTCDIV: These 6-bits determine the setting for the Real-Time Clock Divisor.

MXSEL Configuration

MXSEL: These resistors set the DRAM Row / Column multiplexing

MXSEL	Column Address Bits	DRAM Configurations Supported
00	8	64k x N & 128k x N
01	9	256k x N & 512k x N
10	10	1 Meg x N & 2 Meg x N
11	11	4 Meg x N & 8 Meg x N

(Note: at the time of this design suitable 64xN and 128xN are difficult to purchase in the market.)

MSLO Configuration

MSLO: This resistor selects the expected access time of the DRAM. If MSLO is high, 80ns DRAM is expected. If MSLO is low, 60ns DRAM is expected.

MDCAS Configuration

MDCAS: This resistor selects the type of DRAM used. If MDCAS is high, the memory interface will generate control signals for 2-CAS DRAM's.. If MDCAS is low, it generates signals for single CAS DRAM's. This reference design uses two CAS DRAM’s.

MTYPE Configuration

These twelve resistors per PM3350 are divided into four groups of three bits each. Each bit combination selects one of eight different memory types. These bits are read off the data bus during start-up, and tell the RISC how to access memory. Each group corresponds to one of the four banks of memory. On the Reference Design Board:

- Bank 0 is set up to be EDO DRAM,
- Bank 1 is available on U23. Other PM3350 this bank is unused.
- Bank 2 is set up as EPROM,
- Bank 3 is only used on the PM3350 for status LEDS during debug.

MTYPE	Memory Type	Speed
000	Reserved	N/A
001	Reserved	N/A
010	Reserved	N/A
011	Reserved	N/A
100	Reserved	N/A
101	EPROM	180 nsec
110	EDO DRAM	60/80 nsec
111	Reserved	N/A

Two 256K x 16-bit 60ns EDO DRAM's are used for each PM3350 device in this reference design.

An additional two 256K x 16-bit 60ns EDO DRAMs are used by the master PM3350 device to support managed versions of the operating firmware.

INTERFACE DESCRIPTION

This section is a detailed description the physical interfaces in this reference design, which include 1) the RJ45 connectors, and 2) the PCI Expansion Bus connector.

RJ45 Pin Definition

Each of the 24 RJ45 connectors on the reference design have the following pin definition.

Signal Name	Pin	Type	Description
TX+ TX -	3 6	O	Transmit Pair on UTP5 Cable.
RX + RX -	2 1	I	Receive Pair on UTP5 Cable.

The pins are defined such that the port looks like a hub port. This allows a direct cable connection from the switch port to a computer. A crossover cable is needed to connect the switch port to another switch port.

PCI Expansion Bus Interface

Signal Name	Pin	Type	Description
AD[31:0]	B20 A20 B21 A22 B23 A23 B24 A25 B27 A28 B29 A29 B30 A31 B32 A32 A44 B45 A46 B47 A47 B48 A49 B52 B53 A54 B55 A55 B56 A57 A59 B58	I/O	Multiplexed PCI address/data bus, used by the PCI host or the PM3350 to transfer addresses or data.
CBE[3:0]	B26 B33 B44 A52	I/O	Command/Byte-Enable lines. These lines supply a command (during PCI address phases) or byte enables (during data phases) for each bus transaction.
PAR	A43	I/O	Address/data/command parity, supplies the even parity computed over the AD[31:0] and CBE[3:0] lines during valid data phases; it is sampled (when the PM3350 is acting as a target) or driven (when the PM3350 acts as an initiator) one clock edge after the respective data phase.
FRAME*	A34	I/O	Bus transaction delimiter (framing signal); a HIGH-to-LOW transition on this signal indicates that a new transaction is beginning (with an address phase); a LOW-to-HIGH transition indicates that the next valid data phase will end the currently ongoing transaction.

IRDY*	B35	I/O	Transaction Initiator (master) ready, used by the transaction initiator or bus master to indicate that it is ready for a data transfer. A valid data phase ends with data transfer when both IRDY* and TRDY* are sampled asserted on the same clock edge.
TRDY*	A36	I/O	Transaction Target ready, used by the transaction target or bus slave to indicate that it is ready for a data transfer. A valid data phase ends with data transfer when both IRDY* and TRDY* are sampled asserted on the same clock edge.
STOP*	A38	I/O	Transaction termination request, driven by the current target or slave to abort, disconnect or retry the current transfer.
DEVSEL*	B37	I/O	Device acknowledge: driven by a target to indicate to the initiator that the address placed on the AD[31:0] lines (together with the command on the CBE[3:0] lines) has been decoded and accepted as a valid reference to the target's address space. Once asserted, it is held asserted until FRAME* is de-asserted; otherwise, it indicates (in conjunction with STOP* and TRDY*) a target-abort.
IDSEL	A26	I	Device identification (slot) select. Assertion of IDSEL signals the PM3350 that it is being selected for a configuration space access.
REQ* REQ7* REQ6* REQ5* REQ4* REQ3*	B18 B1 A1 A3 A2 B2	I	Bus requests (to bus arbiter). They are used only when external ED/FED devices are connected on the PCI bus. They are asserted by the external devices to request control of the PCI bus. It is intended that a PCI arbiter the PM3350 board have control of bus arbitration. PCI 2.1 specification defines only one Bus Request signal. In this case, these extra Bus Request signals occupy the following unused pins on the PCI connector: B1: -12V (REQ7*), A1: TRST* (REQ6*), A3: TMS (REQ5), A2: +12V (REQ4*), B2: TCK (REQ3*)
GNT* GNT7* GNT6* GNT5* GNT4* GNT3*	A17 B7 A7 B8 B10 A9	O	Bus grant (from bus arbiter). They are used only when external ED/FED devices are connected on the PCI bus. This indicates to the external device that it has been granted control of the PCI bus. It is intended that a PCI arbiter on the PM3350 board have control of bus arbitration. PCI 2.1 specification defines only one Bus Grant signal. In this case, these extra Bus Grant signals occupy the following unused pins on the PCI connector: B7: INTB* (GNT7*), A7: INTC* (GNT6*), B8: INTD* (GNT5*), B10: Reserved(GNT4), A9: Reserved (GNT3*)
INTA*	A6	O	Interrupt request. This pin signals an interrupt request to the PCI host.
PERR*	B40	I/O	Bus parity error signal, asserted by the PM3350 as a bus slave, or sampled by the PM3350 as a bus master, to indicate a parity error on the AD[31:0] and CBE[3:0] lines.
SERR*	B42	OD	System error, used by the PM3350 to indicate to the PCI central resource that there was a parity error on the AD[31:0] and CBE[3:0] lines during an address phase.
PCICLK	B16	I	PCI bus clock; supplies the PCI bus clock signal to the PM3350.
RST*	A15	I	PCI bus reset (system reset). Performs a hardware reset of the PM3350 and associated peripherals when asserted.

Notes: 1) The '*' indicates active-low signals, which corresponds to '#' used in the PCI specification.

2) Pin numbers are listed MSB first

APPENDIX A: DESIGN CONSIDERATIONS

For those who are interested more additional in-depth considerations for this reference design, this Design Consideration section provides many tips and guidelines on high-speed circuit board design and component selection.

Power Supply Decoupling

A 0.01uF or 0.1uF decoupling capacitor is also placed as close to each power pin as possible. If noise attenuation is required, a small surface mount series resistor (1 to 10 Ohms) can be added in series with the power pin.

Unused CMOS Inputs

"Floating" CMOS inputs (those that are left unconnected) may switch unpredictably, causing unwanted noise and power consumption. Therefore, all unused inputs should be connected to their inactive state: to ground or to the power rail (Vcc). Unused bi-directionals should be "pulled" through a series resistor (4.7k or greater) to avoid short-circuits occurring if the bi-directionals are erroneously configured as outputs.

EMI Considerations

EMI can be reduced via proper routing, decoupling, power and ground distribution, shielding, and filtering. Most of the items listed below for EMI improvement also lend themselves towards improving system level performance.

Routing Guidelines

Proper decoupling and termination are effective ways of reducing EMI. The following are some routing guidelines which will help reduce EMI:

- Data lines should be kept away from the clock signals to avoid noise coupling.
- No high speed signals should be routed near the vicinity of the RJ45 modular jack and the transformer in order to prevent common-mode noise coupling onto the cable.
- Footprints of capacitors can be placed along signals with fast rise and fall times. In the event that fast edges causes excessive EMI, they can be slowed down (if timing and system level performance are not compromised) using these capacitors.

Power and Ground Planes

- The power plane should be kept away from the RJ45 modular jack and the transformer to prevent noise coupling.
- Ensure that power and ground planes of different sections do not overlap in order to prevent noise coupling.
- Provide a chassis ground plane under the RJ45 modular jack.

PCI Considerations

The following are PCI specification guidelines for trace lengths. These are not absolute constraints, but good to work toward for proper signal integrity and bus throughput.

- Use 0.25 inches for power traces (assuming 20 mil power traces).
- The maximum trace lengths for all 32-bit interface signals are limited to 1.5 inches from the top of the card edge connector to the PCI device.
- The maximum trace lengths for the PCI CLK signal is limited to 2.5 inches from the top of the card edge connector to the PCI device. (+/- 0.1 inches)

The following highlights the way signal traces will be routed to follow the PCI specification 2.1.

- First choose to route over either the 5v plane or the 3.3v plane
- If a trace would have to cross over 5v and 3.3v islands then route the trace on the secondary side with a reference to the ground plane.
- If this is not possible then decouple the 5v to the 3.3v with a 0.01 microFarad cap. The capacitor will be placed within 0.25 inches from the point the signal crosses the split. One capacitor for each four PCI signal lines will be used.

PCI Signal Trace Width

- Characteristic impedance for signal traces is designated in the PCI Specification to be between 60 and 100 Ohms (Zo).

- The following approximation formula may be used for four layer boards (EQ1):

$$Z0 = \frac{87}{\sqrt{Er + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 + t}\right)$$

Er is the dielectric permittivity
h is the dielectric thickness between the trace and the next plane down.
t is the copper thickness determined by the weight. (2oz ~ 2.88 mil)
w is the trace width

Here is an example that uses 1-oz copper.
Given:
Zo = 72
Er = 4.6
h = 0.010 inches (10 mil)
t = 0.00144 inches (1.44 mil)
Results:
w ~ 8 mil trace width

- The following approximation formula may be used for traces on inner layers between two power planes:
(EQ2):

$$Z0 = \frac{60}{\sqrt{Er}} \times \ln\left(\frac{1.9 \times b}{0.8 \times w + t}\right)$$

Er is the dielectric permittivity
b is the separation between grounds
t is the copper thickness determined by the weight. (2oz ~ 2.88 mil)
w is the trace width

Board Dielectric Permittivity

- The estimation of the dielectric relative permittivity leads to a range of 3.13 to 5.0 when traces are on the inner or outer layers. (Estimate based on propagation delay.) The FR-4 material used in this design uses a value of 4.6.

24 Port Switch PCB Parameters

- This reference design uses an eight layer Printed Circuit Board with 8 mil traces and 7 mil spacing. The power routes use 20 mil trace width. Trace apertures were changed during board fabrication in some cases. The following table gives the parameters chosen during PCB fabrication.

Between Layers	Layer Thickness	Copper Thickness	Finishing Trace Width	Impedance Estimate
1-2 (prepreg)	5 mils	Finishes at 2 mils	7 mils	89 Ohms (EQ1)
2-3 (core)	5 mils	1.44 mils	6 mils	83 Ohms (EQ1)
3-4 (prepreg)	6 mils	1.44 mils	5 mils	67 Ohms (EQ1)
4-5 (core)	30 mils	1.44 mils	NA	NA
5-6 (prepreg)	6 mils	1.44 mils	5 mils	67 Ohms (EQ1)
6-7 (core)	5 mils	1.44 mils	6 mils	83 Ohms (EQ1)
7-8 (prepreg)	5 mils	Finishes at 2 mils	7 mils	89 Ohms (EQ1)

Component Selection

RJ45 Connector

8-pin 8 position octal RJ45 modular jacks are used in this reference design. In general, there are three types of modular jacks:

- non-filtered and non-shielded
- shielded and non-filtered
- shielded and filtered (capacitive filtering or inductive filtering)

Shielding is recommended for EMI considerations. In order for the shielding to be effective, the shield should be electrically connected to the chassis ground via a low impedance connection (i.e. using copper finger stocks or firm mechanical contact with the mounting bracket). Typically, the shielded portion of the jack will extend through the opening in the mounting bracket and make firm mechanical contact with the bracket on all sides.

The following vendors carry RJ45 connectors:

- Stewart Connectors Tel: 717-235-7512
- AMP Tel: 800-522-6752
- Kycon Tel: 800-544-6941
- Power Dynamics Tel: 201-736-5722

Transformer

The transformer used in this reference design is Halo T646-1406NX, a quad-transformer with filtering. Single transformers can also be used if it is more cost-effective.

The following vendors also carries 10-BASE-T transformers (they are not necessarily footprint compatible):

- Valor Tel: 800-318-2567
- Pulse Engineering Tel: 619-674-8100
- Microlinear Tel: 408-433-5200

Oscillator

The on-board oscillators provide a timing reference for the PM3350 device, the Level One LXT944, and the PCI bus interface. The oscillator should be +/-100ppm or better. The stability figure of an oscillator should include any variation due to calibration, temperature, voltage, load, aging, shock, and vibration, and is specified over the lift time of the oscillator.

Either CMOS or TTL oscillator can be used. The following is a list of vendors that provide these oscillators:

- Motron Industries Tel: 605-665-9321
- Connor Winfield Tel: 708-851-4722
- Champion Tel: 708-451-1000
- Oak Frequency Control Group Tel: 717-486-3411
- Ecliptek Tel: 714-433-1200

APPENDIX B: BILL OF MATERIALS

This table lists the components used in this reference design. Note that compatible components can be substituted, but this is not guaranteed. Please refer to the Component Selection section in Appendix A for suggestions on alternative sources for some of the major components.

PM3350 24 Port Reference Design Schematic - Top Revised: Thursday, October 16, 1997
TBD Revision: 1.1

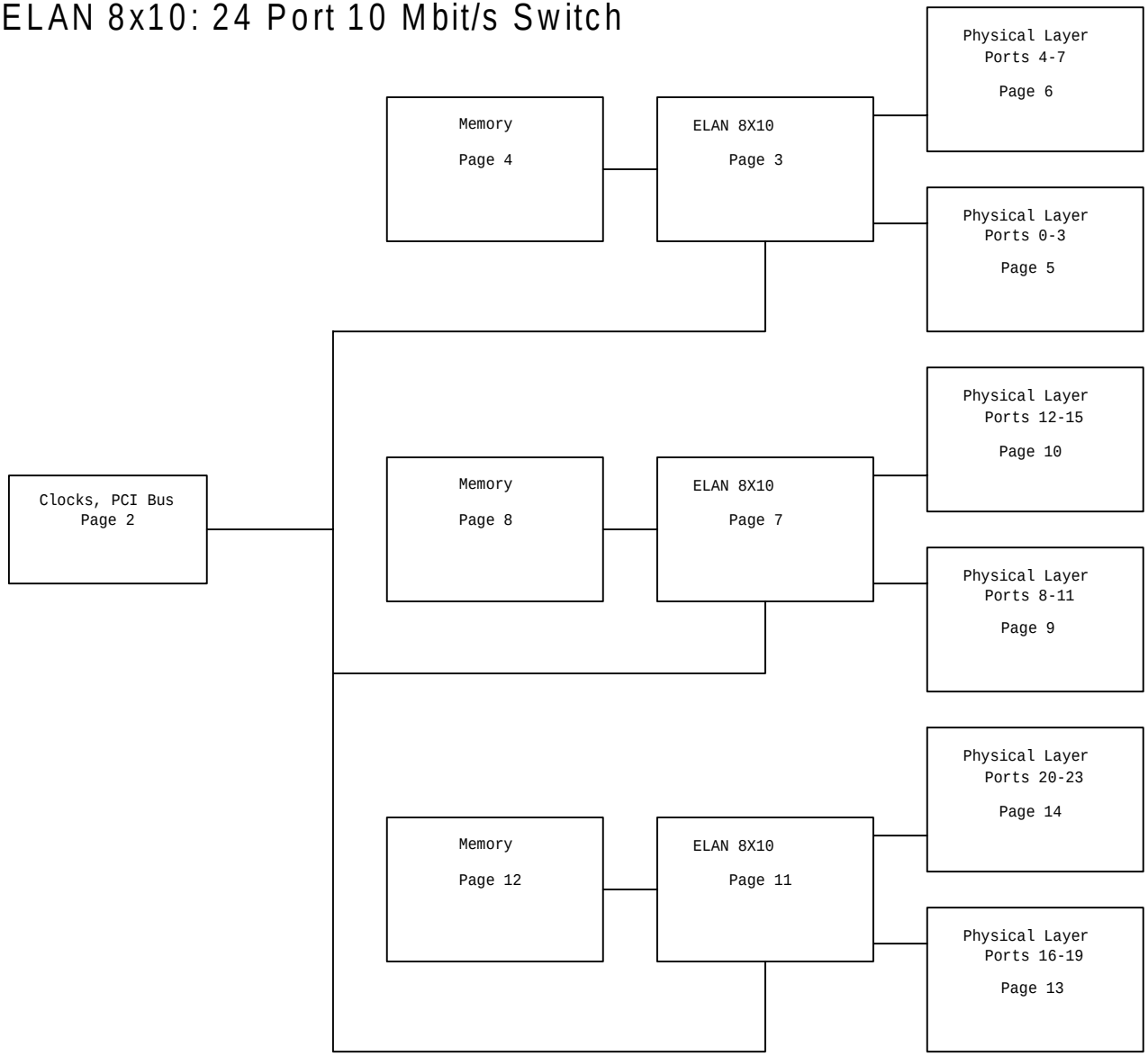
Bill Of Materials November 5, 1997 12:21:02 Page1

Item	Quantity	Reference	Part	PCB Footprint
1	18	C1, C4, C19, C25, C27, C30, C32, C39, C40, C41, C42, C44, C47, C48, C50, C51, C57, C59	22UF	SC/C
2	140	C2, C3, C7, C8, C10, C11, C12, C13, C15, C16, C17, C21, C22, C29, C31, C33, C34, C36, C38, C46, C49, C53, C54, C55, C56, C60, C62, C66, C68, C69, C70, C72, C73, C74, C79, C81, C82, C83, C84, C86, C87, C89, C92, C93, C96, C101, C102, C103, C104, C106, C110, C112, C113, C114, C116, C117, C119, C123, C125, C126, C127, C128, C130, C131, C133, C137, C138, C139, C141, C145, C146, C147, C149, C150, C151, C152, C153, C154, C155, C158, C159, C160, C161, C162, C163, C166, C167, C168, C169, C170, C171, C172, C173, C174, C176, C180, C181, C182, C183, C184, C186, C187, C188, C189, C190, C193, C194, C195, C197, C199, C201, C202, C203, C206, C208, C209, C210, C211, C212, C214, C215, C216, C217, C219, C220, C221, C222, C223, C224, C225, C227, C229, C230, C231, C236, C237, C238, C241, C244, C246	.1uF	SC0805
3	60	C5, C18, C20, C23, C24, C26, C28, C35, C37, C43, C45, C52, C67, C71, C80, C85, C88, C94, C95, C100, C105, C111, C115, C118, C124, C129, C132, C140, C144, C148, C156, C157, C164, C165, C175, C177, C178, C179, C185, C191, C192, C196, C198, C200, C204, C205, C207, C213, C218, C226, C228, C232, C233, C234, C235, C239, C240, C242, C243, C245	.01uF	SC0805
4	2	C6, C14	33uF	SC/C

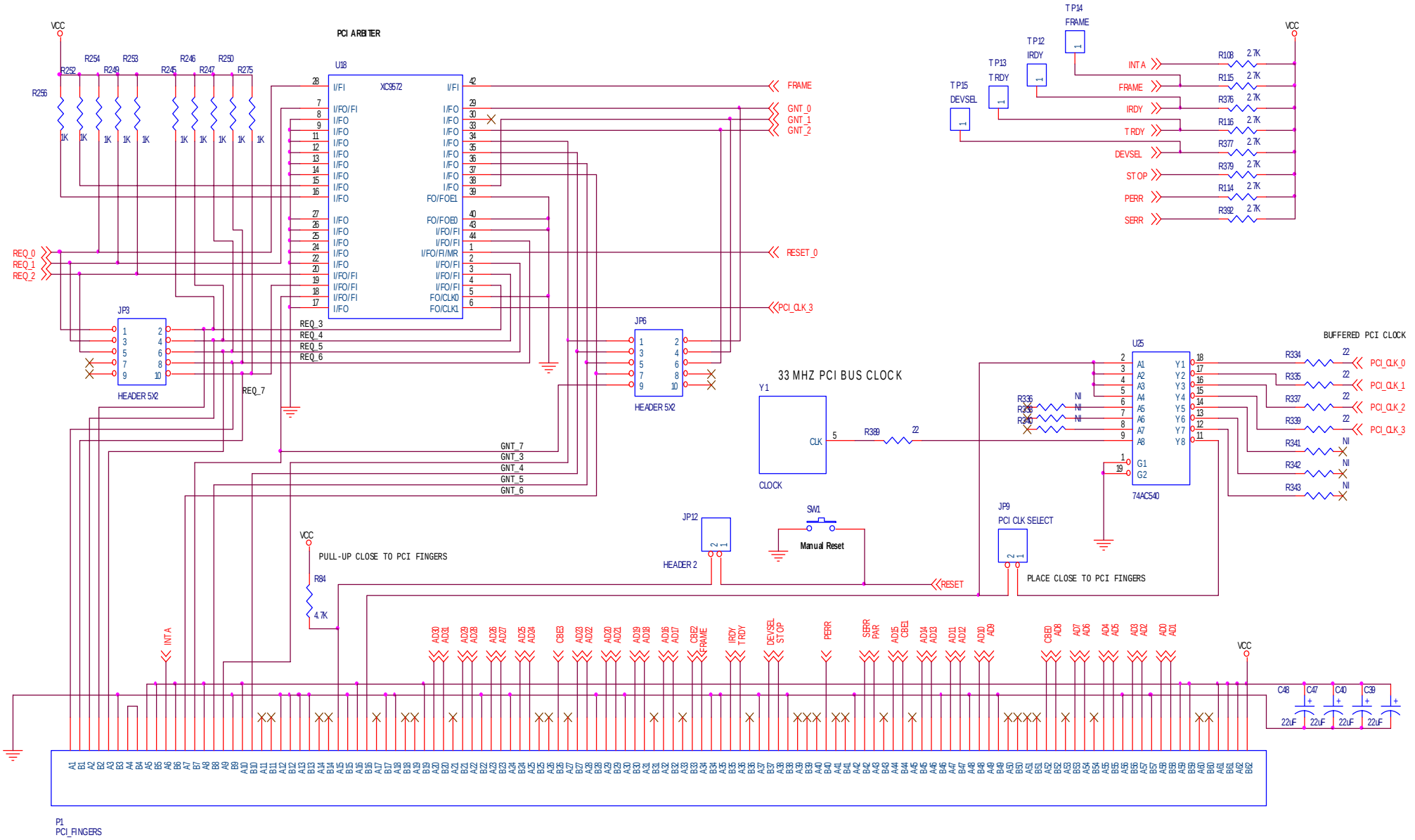
5	1	C9	560PF	SC0805
6	1	C58	330uF 50V	CAP/RADIAL/200 MILS
7	24	C61, C63, C64, C65, C75, C76, C77, C78, C90, C91, C97, C98, C99, C107, C108, C109, C120, C121, C122, C134, C135, C136, C142, C143	120pF	SC0805
9	6	D2, D3, D4, D5, D6, D7	QUAD_LED	LEDX4
10	1	D26	1N4001	DIODE/THROUGH HOLE
11	1	JK1	GND	PAD250
12	1	JK2	VCC	PAD250
13	7	JP1, JP2, JP5, JP10, JP12, JP8, JP9	HEADER 2	HD002
14	2	JP3, JP6	HEADER 5X2	HD016
18	3	J1, J2, J3	RJ45X8	PHONEJ/8X
20	24	R1, R2, R6, R7, R13, R14, R19, R20, R25, R26, R34, R35, R124, R125, R134, R146, R153, R154, R169, R170, R190, R191, R199, R200	100	SR0805
22	30	R5, R8, R9, R15, R16, R17, R18, R21, R27, R29, R30, R33, R36, R37, R41, R42, R53, R60, R98, R99, R155, R259, R260, R272, R307, R314, R317, R319, R366, R370	4.7K	SR0805\3P
23	48	R44, R45, R46, R47, R48, R49, R50, R51, R52, R54, R55, R56, R57, R58, R117, R118, R119, R120, R121, R122, R138, R205, R206, R207, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R233, R238, R242, R244, R248, R251, R255, R257	390	SR0805
24	17	R59, R61, R94, R108, R114, R115, R116, R156, R258, R267, R302, R303, R362, R376, R377, R379, R392	2.7K	SR0805
25	81	R62, R63, R64, R65, R73, R74, R75, R84, R95, R96, R97, R109, R110, R111, R112, R231, R232, R234, R235, R236, R237, R239, R240, R241, R243, R261, R262, R263, R264, R265, R266, R268, R269, R270, R271, R273, R274, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R304, R305, R306, R308, R309, R310, R311, R312, R313, R344, R345, R346, R360, R361, R363, R364, R365, R367, R368, R369, R371, R380, R381, R382, R383, R384, R385, R386, R387	4.7K	SR0805
26	77	R66, R67, R68, R69, R70, R71, R72, R76, R77, R78, R79, R80, R81, R82, R85, R86, R87, R88, R89, R90, R91, R93, R100, R101, R102, R103, R104, R105, R106, R113, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R315, R316, R318, R320,	22	SR0805

		R321, R322, R323, R324, R325, R327, R328, R329, R330, R331, R332, R334, R335, R337, R339, R347, R348, R349, R350, R351, R352, R353, R354, R356, R357, R372, R373, R374, R375, R389, R390, R391		
27	14	R83, R92, R107, R245, R246, R247, R249, R250, R252, R253, R254, R256, R275, R393	1K	SR0805
28	48	R123, R127, R128, R129, R130, R131, R132, R133, R139, R140, R141, R142, R143, R144, R145, R148, R149, R150, R151, R152, R163, R164, R165, R166, R167, R168, R175, R176, R177, R178, R179, R180, R184, R185, R186, R187, R188, R189, R193, R194, R195, R196, R197, R198, R208, R209, R210, R211	24.9	SR0805
29	5	R135, R171, R181, R201, R212	4.5K	SR0805
30	6	R136, R157, R172, R182, R202, R213	7.5K	SR0805
31	1	SW1	SW PUSHBUTTON	HD003
41	6	U1, U3, U5, U7, U9, U11	TG45-1406NX	SOL40
42	6	U2, U4, U6, U8, U10, U12	LXT944QC	PQFP100_0.026PITCH
44	6	U14, U17, U21, U22, U27, U29	MT4C16270DL-6	SOJ40
45	1	U15	27C020	U32S6
46	1	U18	XC9572	PLCC44
48	3	U23, U24, U28	PM3350	BGA256
49	2	U25, U26	74F540	
50	1	U30	LT1585CT-3.3-ND	TO220
51	1	U31	DS1233	SOT-223/PMC
53	2	Y1, Y2	CLOCK	Y005
54	2	Y1, Y2	SOCKET	Y005
55	1	U15	SOCKET	U32S6
56	1	U18	SOCKET	PLCC44

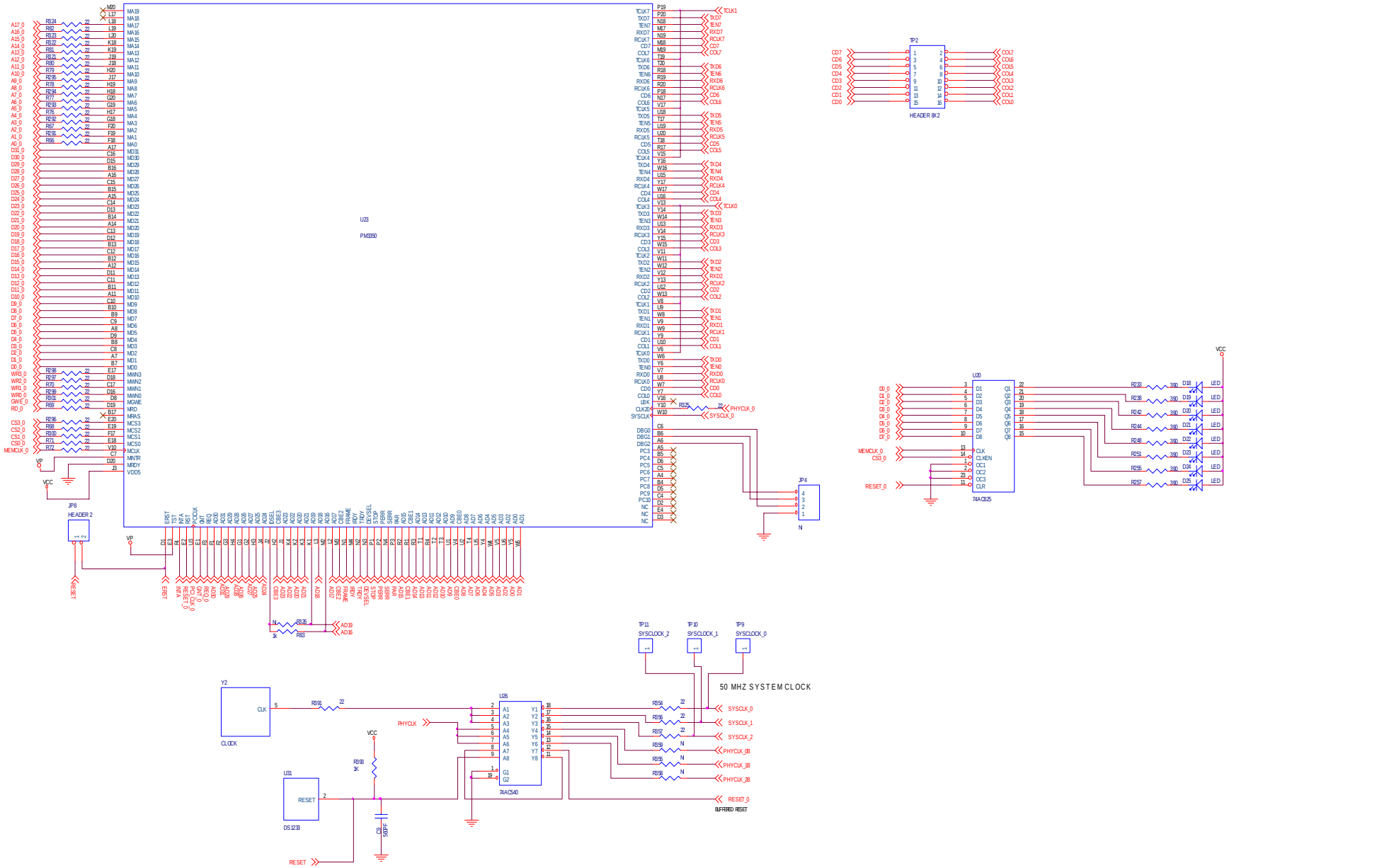
ELAN 8x10: 24 Port 10 Mbit/s Switch



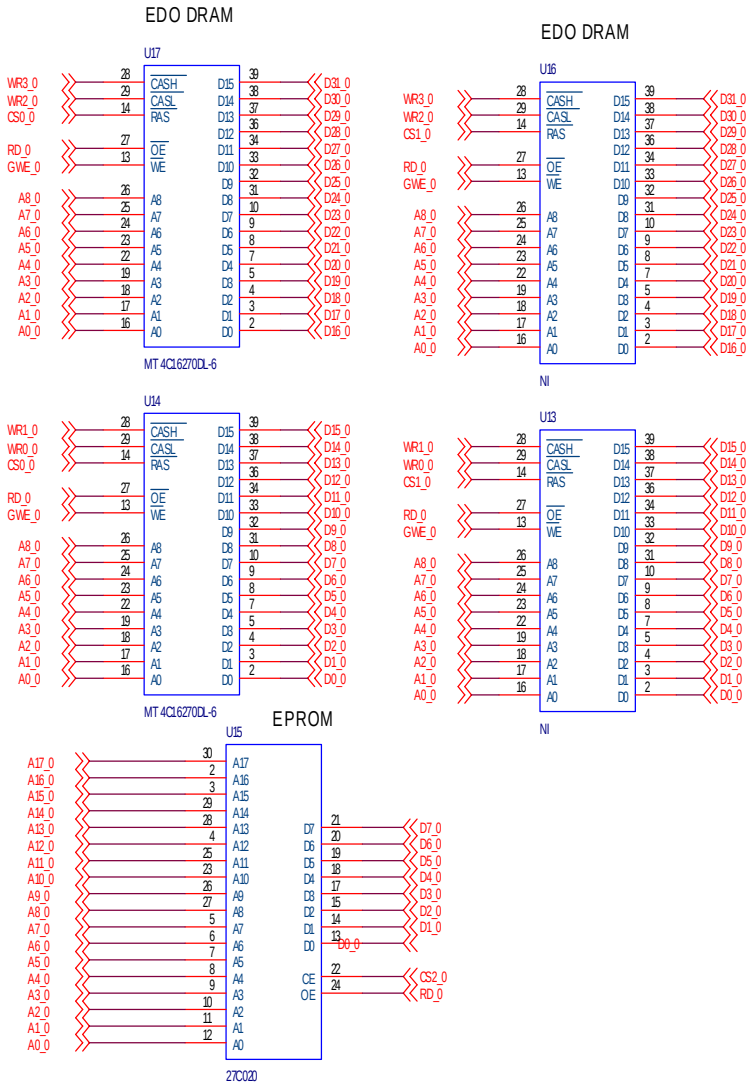
PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - Top		
Size: A	Document Number: TBD	Rev: 1.1
Date: Thursday, October 16, 1997	Sheet 1 of 15	

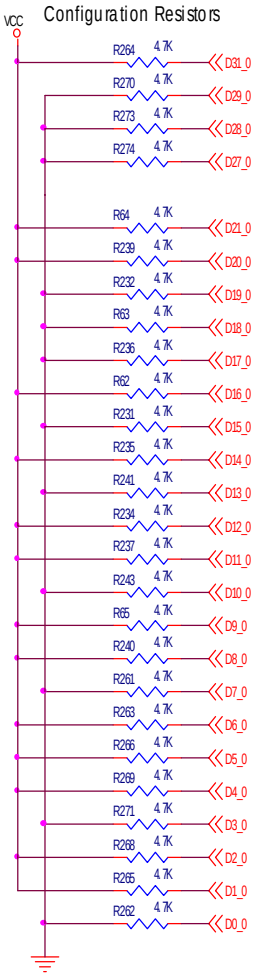


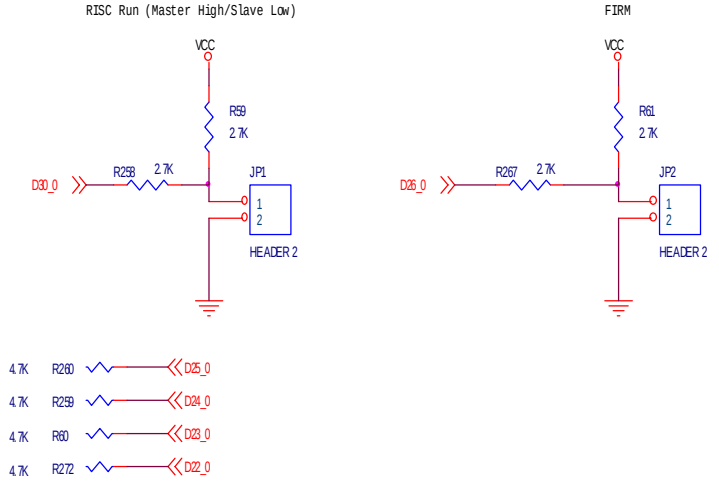
PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - Bus		
Size: B	Document Number: TBD	Rev: 1.1
Date: Wednesday, November 05, 1997	Sheet 2 of 15	



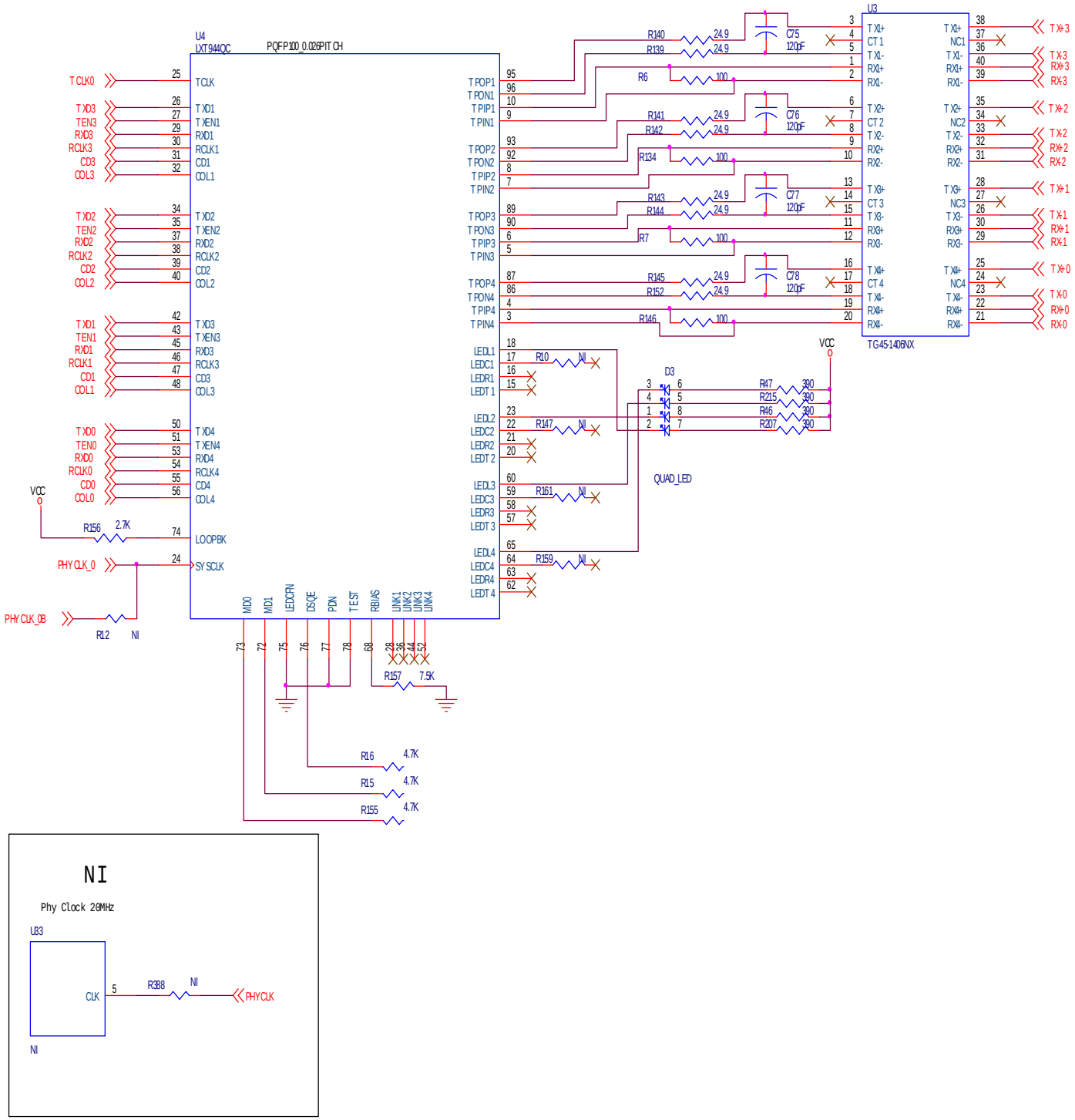
PMC-Sierra, Inc.	Ethernet Products		Portland, Oregon, USA
Title	PM3350 24 Port Reference Design Schematic ED0		
Size: C	Document Number: TBD		Rev: .11
Date: Wednesday, November 05, 1997		Sheet: 3 of: 15	







PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - Memory0		
Size: B	Document Number: TBD	Rev: 1.1
Date: Wednesday, November 05, 1997	Sheet 4 of 15	



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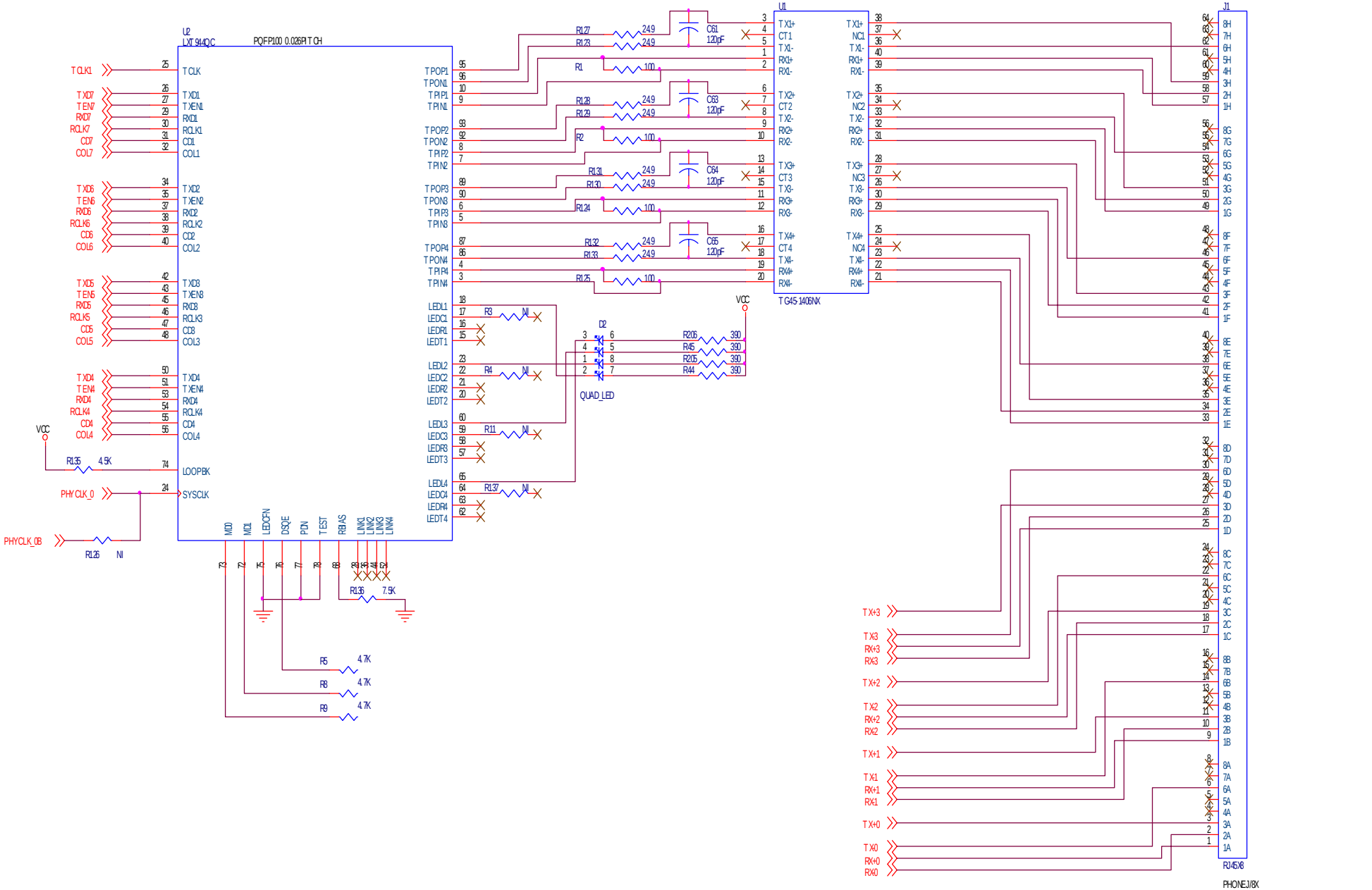
Title

PM3350 24 Port Reference Design Schematic - Phy0-3

Size	Document Number	Rev
B	TBD	1.1

Date: Wednesday, November 05, 1997 Sheet 5 of 15

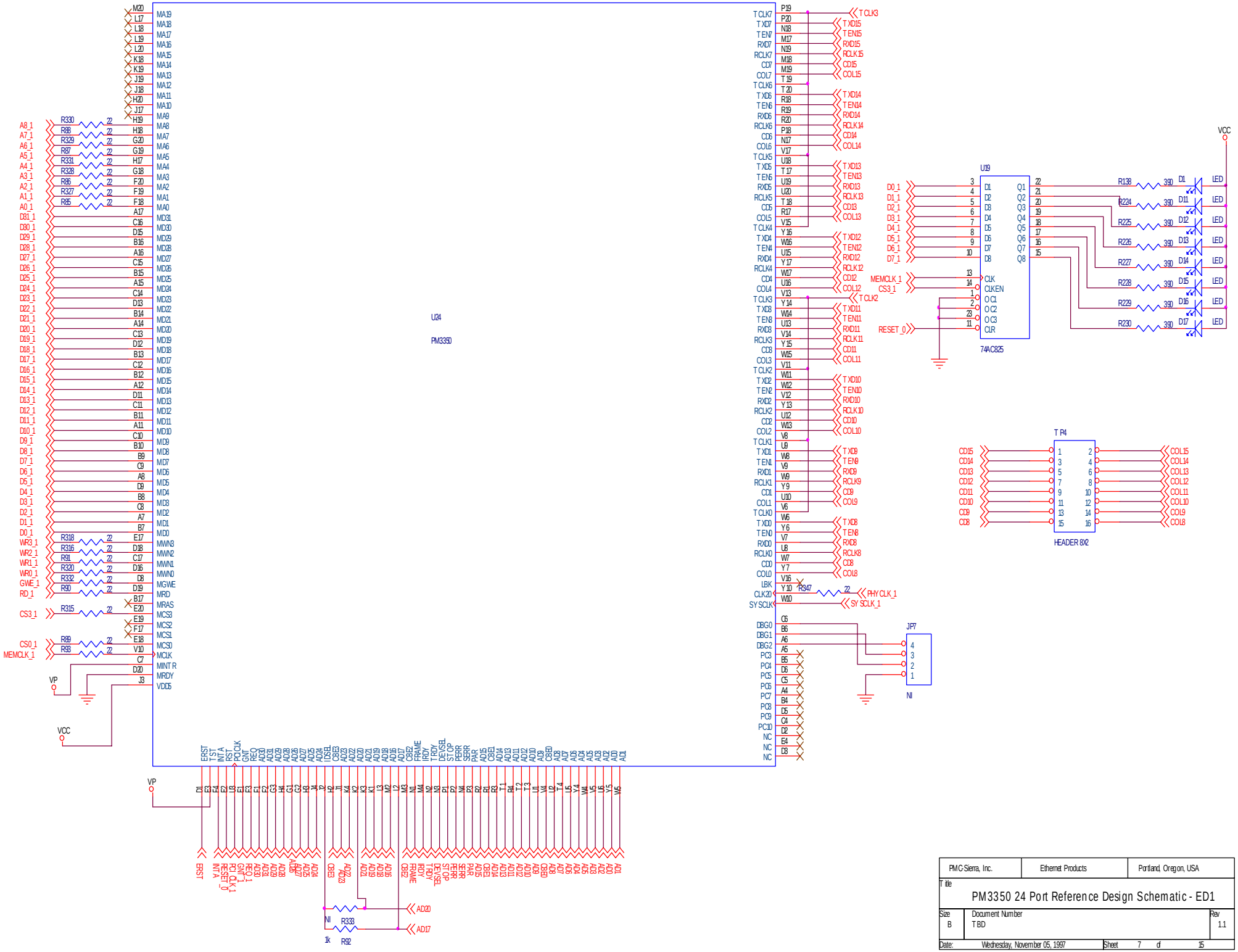


PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA

Title: PM3350 24 Port Reference Design Schematic - Phy4-7

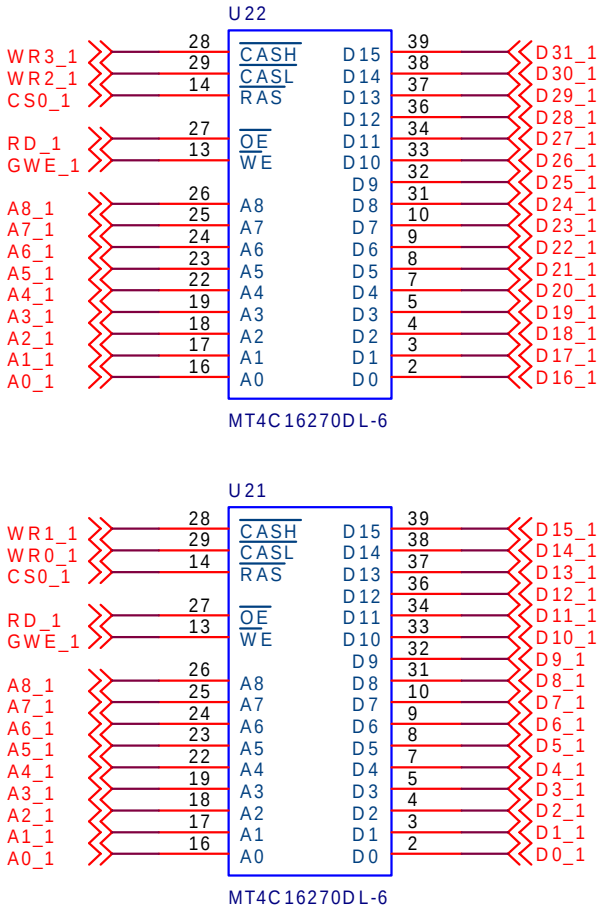
Size	Document Number	Rev
B	TBD	1.1

Date: Wednesday, November 05, 1997 Sheet 6 of 15

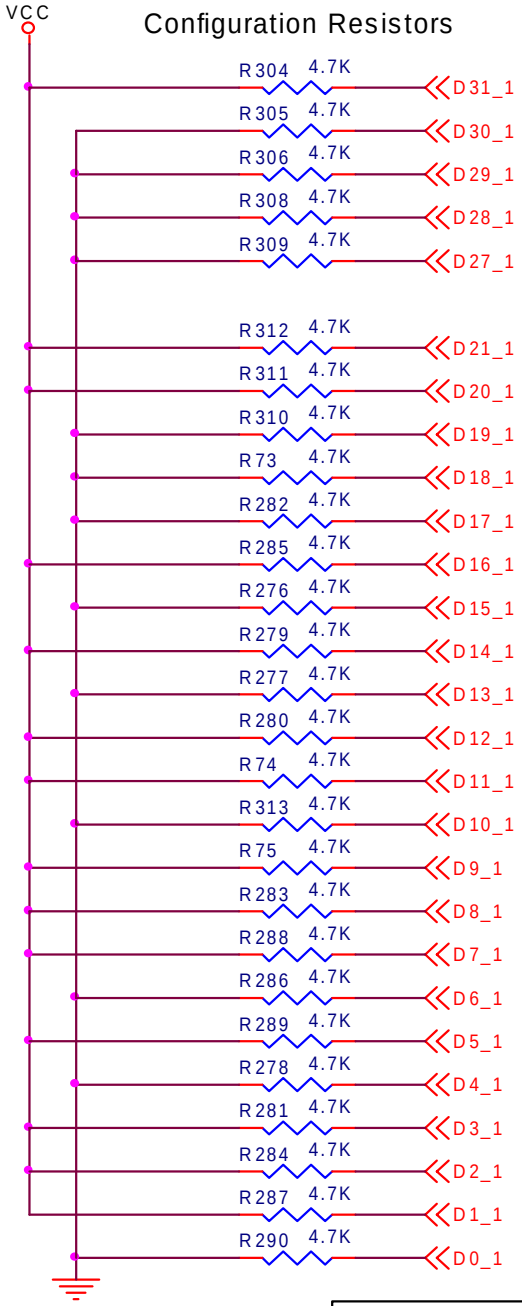


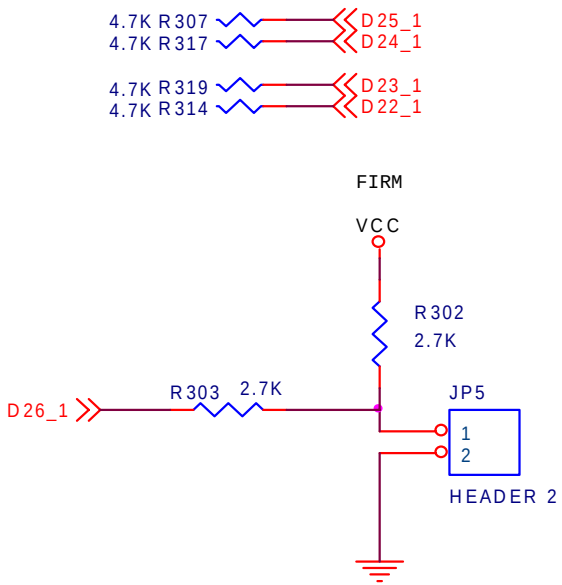
PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - ED1		
Size: B	Document Number: TBD	Rev: 1.1
Date: Wednesday, November 05, 1997	Sheet 7 of 15	

EDO DRAM



Configuration Resistors





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Title

PM3350 24 Port Reference Design Schematic - Memory1

Size	Document Number	Rev
A	TBD	1.1

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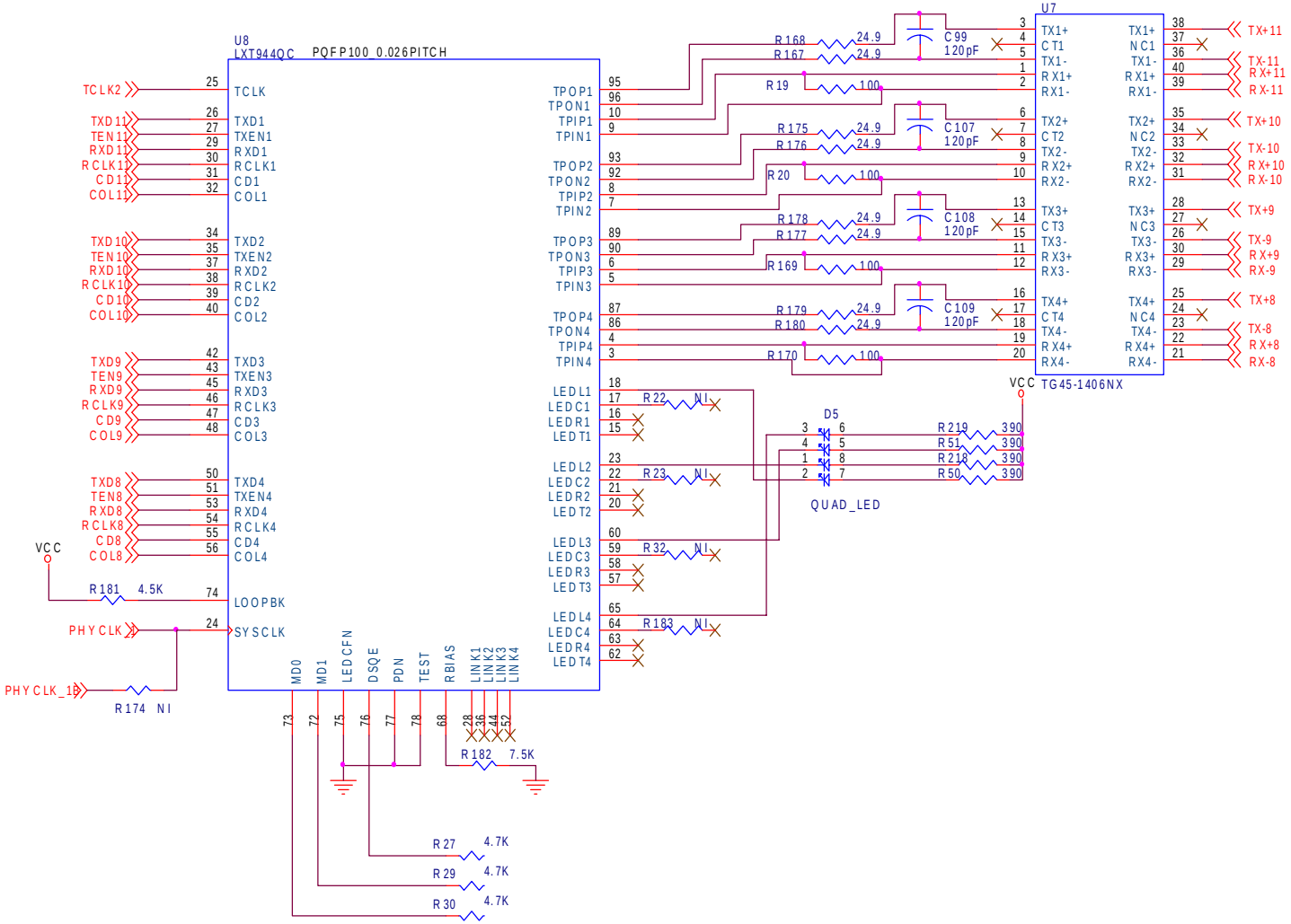

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Title
PM3350 24 Port Reference Design Schematic-Phy8-11

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B	TBD	1.1

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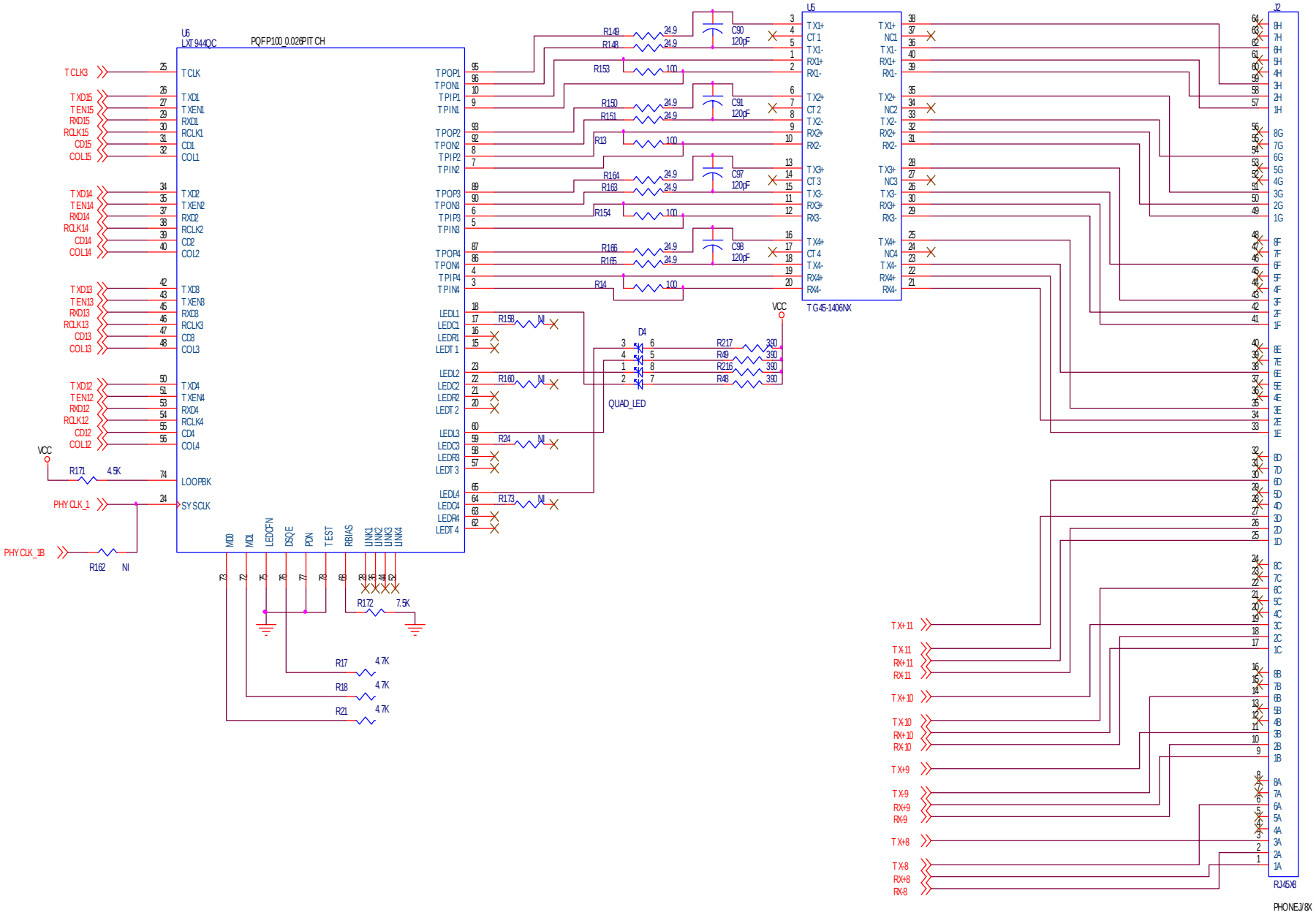

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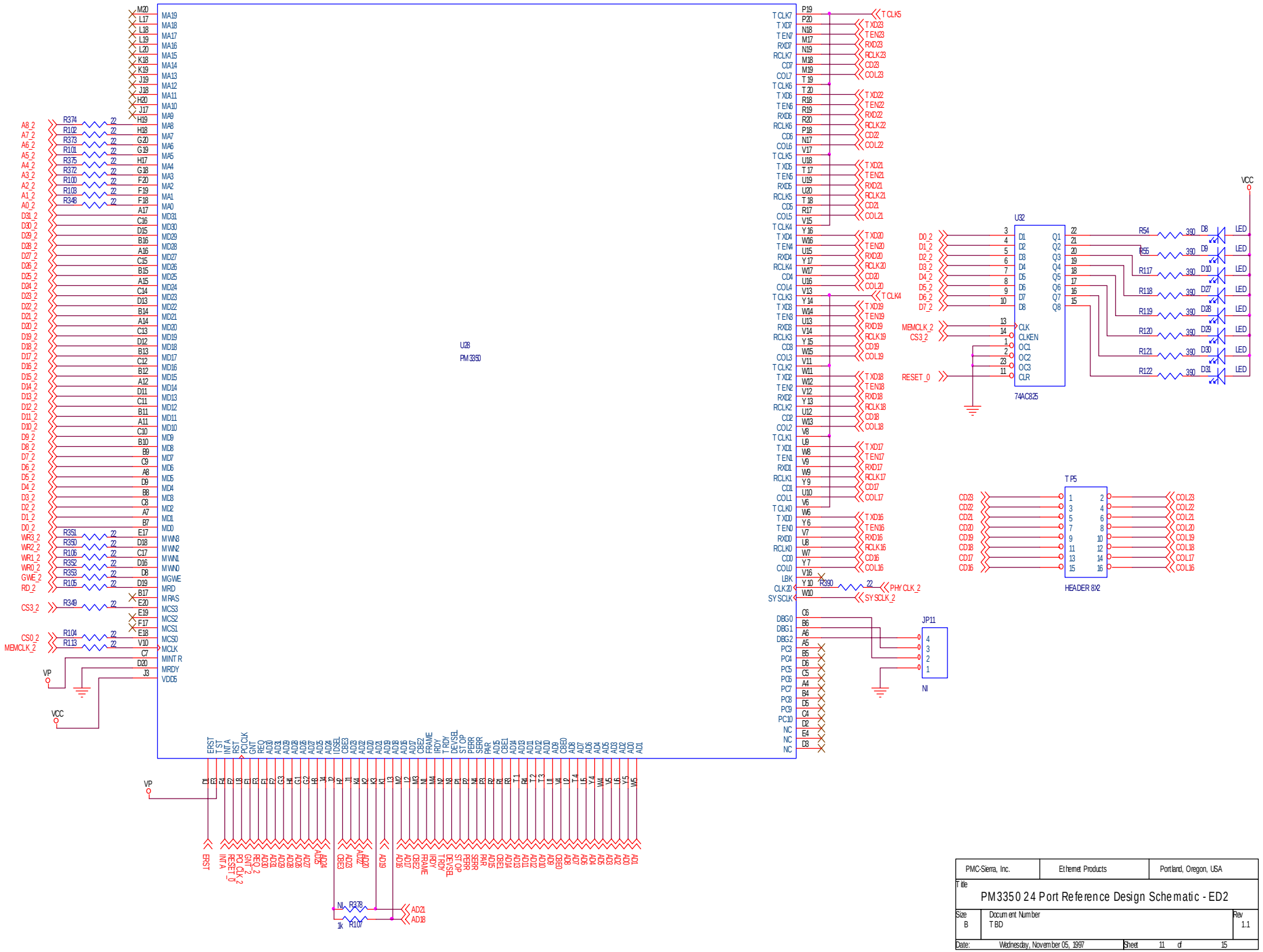
Title
PM3350 24 Port Reference Design Schematic - Phy12-15

Size	Document Number	Rev
B	TBD	1.1

Date: Wednesday, November 05, 1997 Sheet 10 of 15



PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - ED2		
Size: B	Document Number: TBD	Rev: 1.1
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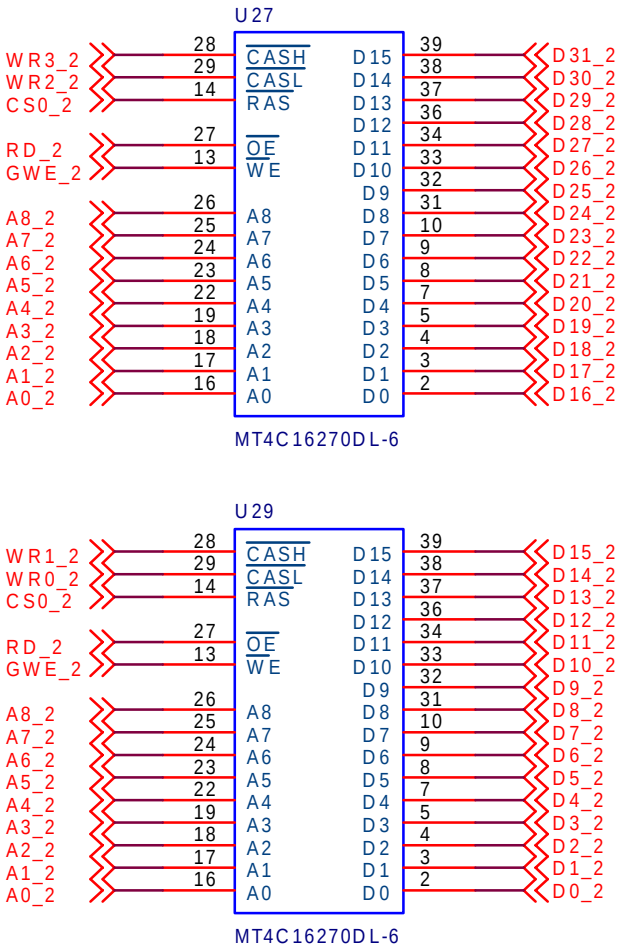
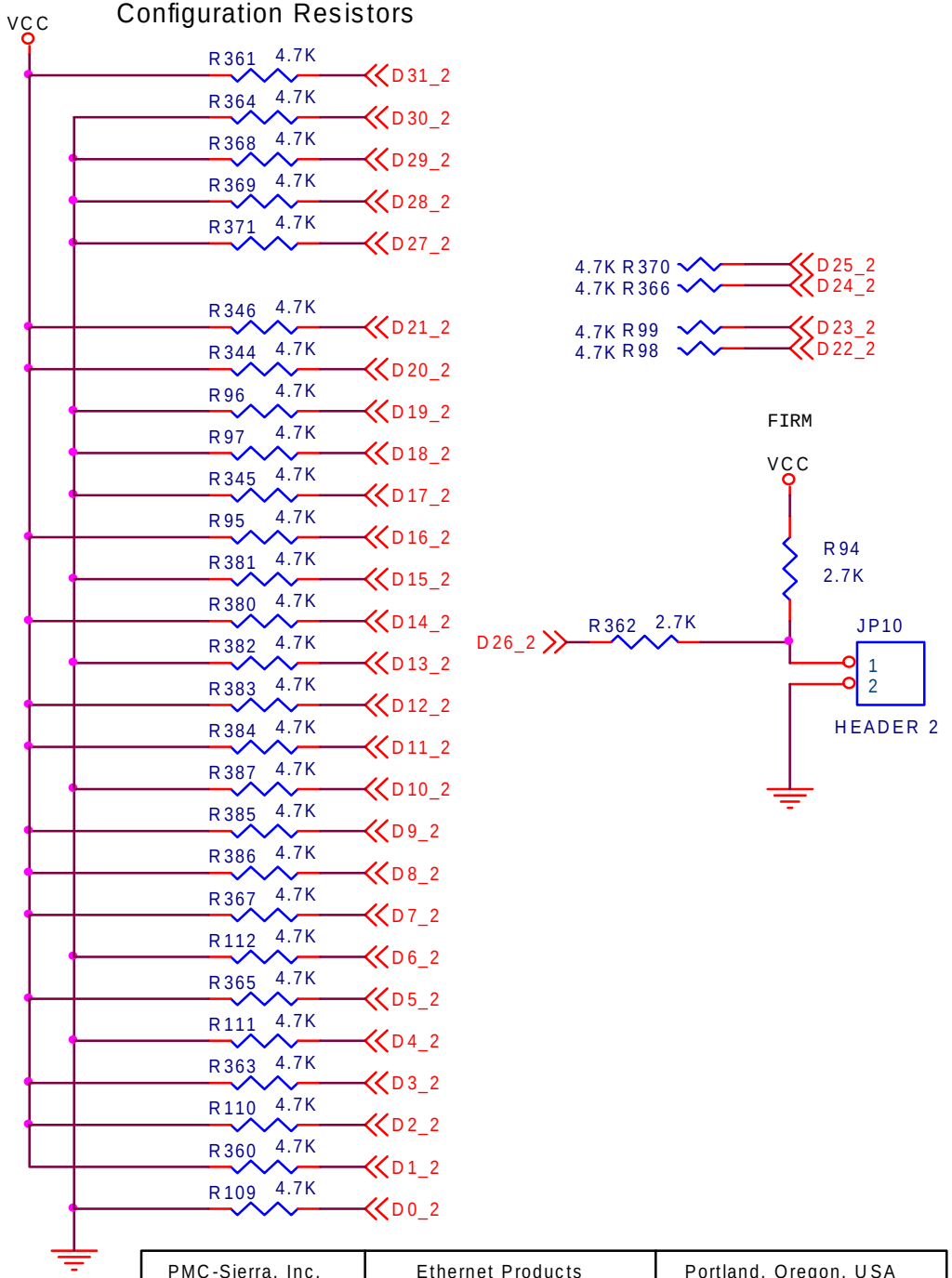
EDO DRAM



Configuration Resistors



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PM3350 24 Port Reference Design Schematic - Memory2

Size	Document Number	Rev
A	TBD	1.1

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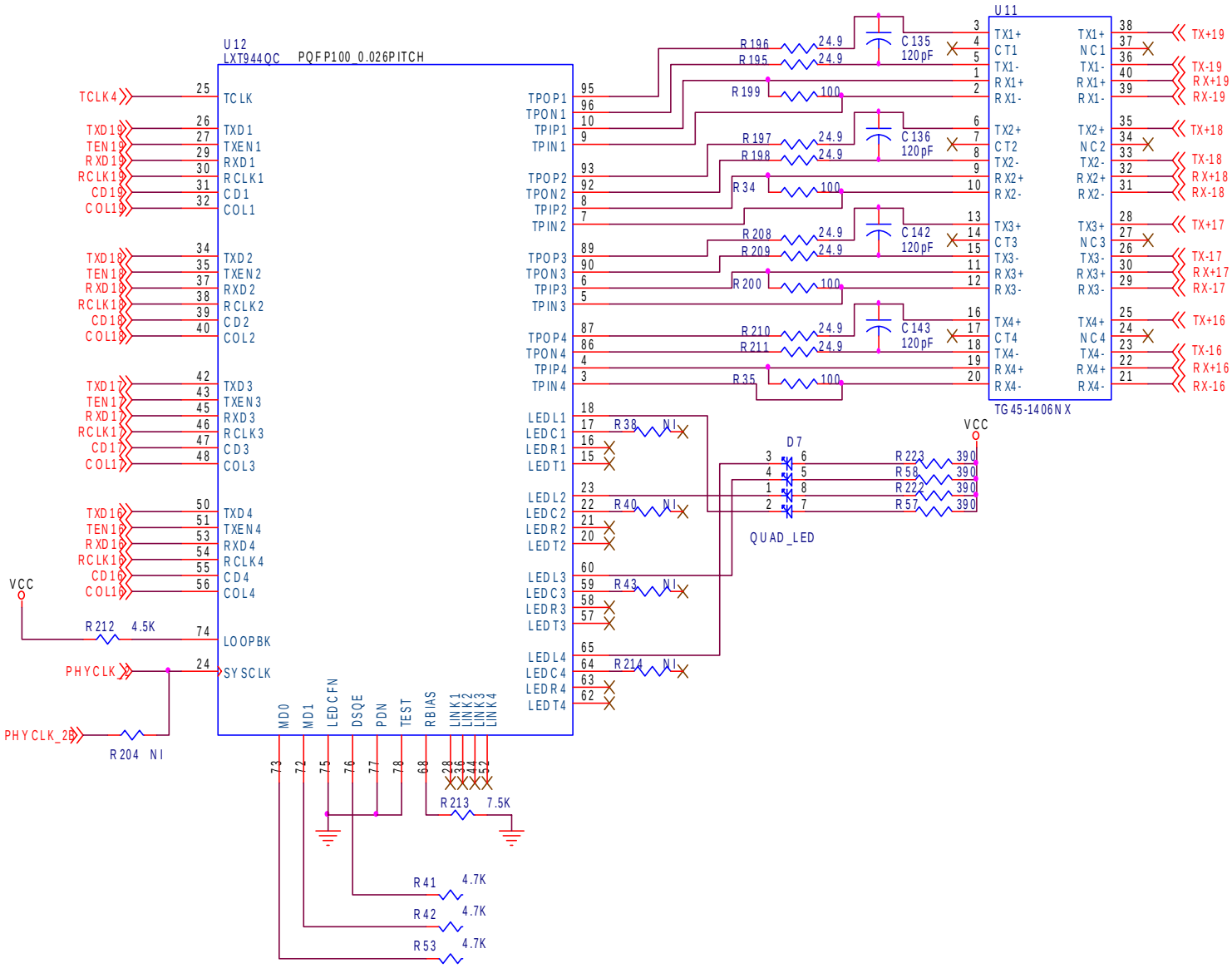
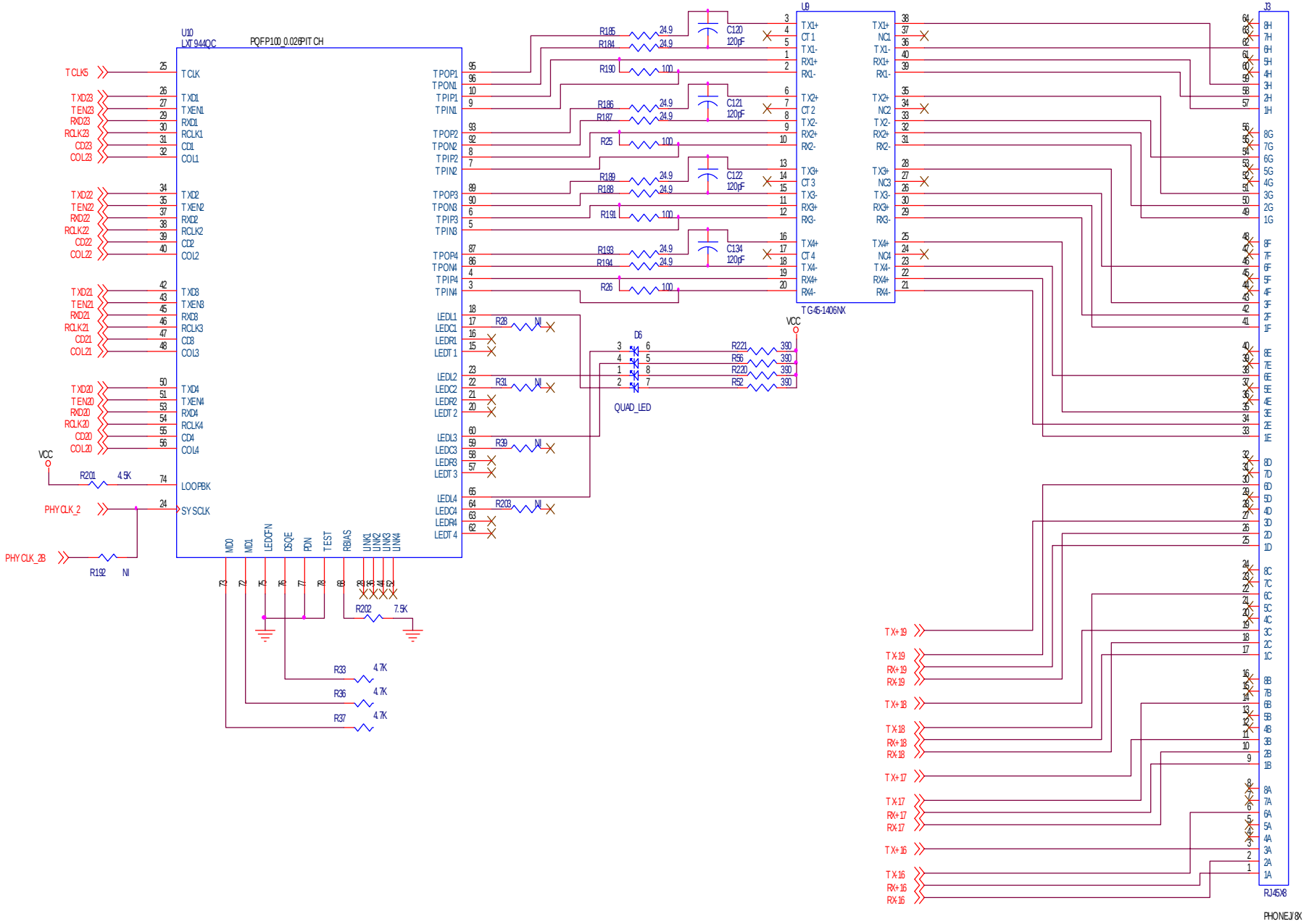


PMC-Sierra, Inc.	Ethernet Products	Portland, Oregon, USA
Title: PM3350 24 Port Reference Design Schematic - Phy16-19		
Size: B	Document Number: TBD	Rev: 1.1
Date: Wednesday, November 05, 199	Sheet 13 of 15	



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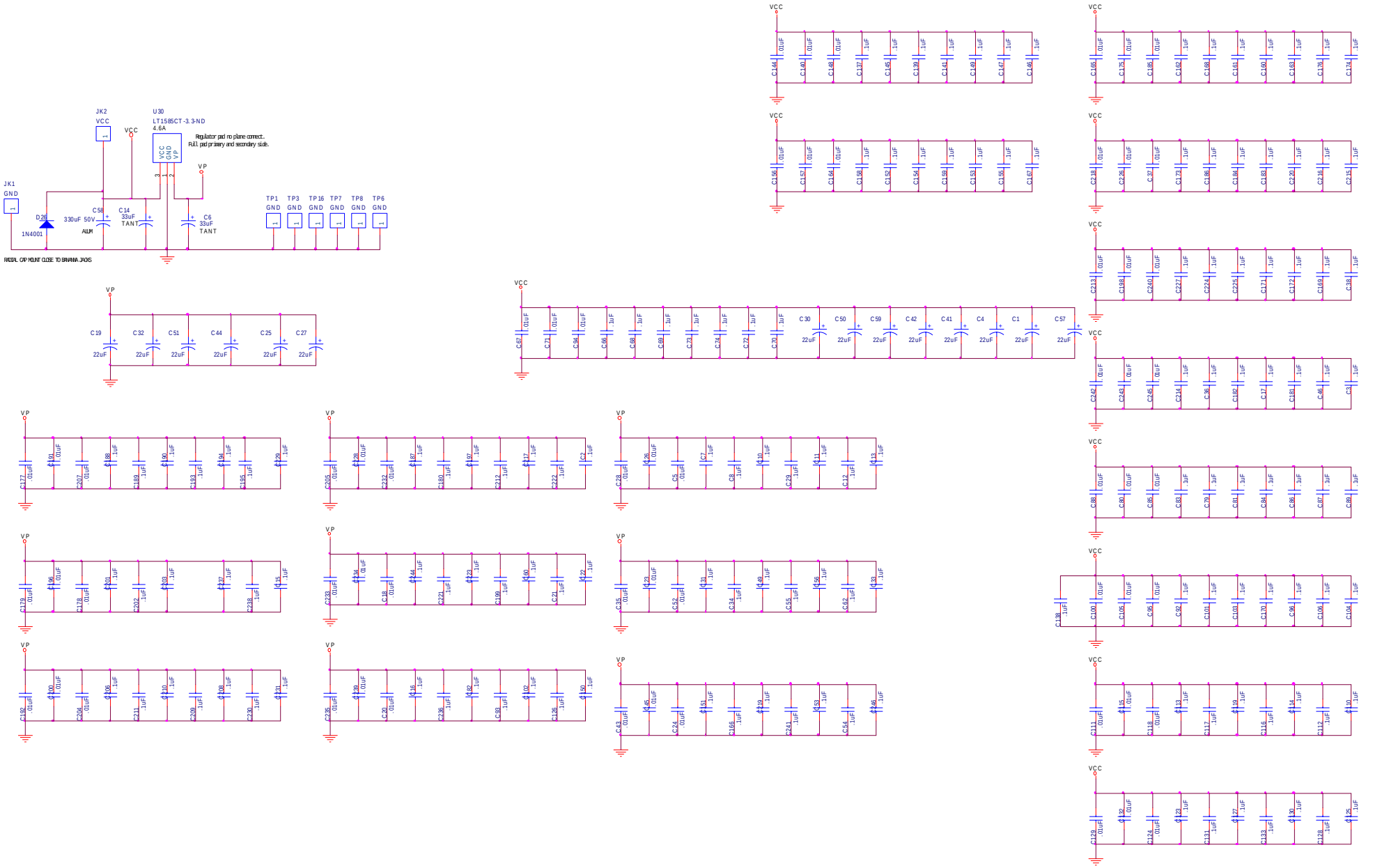
Title

PM3350 24 Port Reference Design Schematic - Phy20-23

Size	Document Number	Rev
B	TBD	1.1

Date:	Wednesday, November 05, 1997	Sheet	14	of	15



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C	TBD	1.1

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CONTACTING PMC-SIERRA

PMC-Sierra, Inc.
Ethernet Products Division
9400 SW Gemini Dr.
Beaverton, OR 97008

Telephone: 503 520-1800
Facsimile: 503 520-1700

Document Information: document@pmc-sierra.com
Product Information: info@pmc-sierra.com
Applications information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

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